FUJITSU SEMICONDUCTOR
DATA SHEET

DS405-00007-1v0-E

ASSP for Power Management Applications

2ch DC/DC converter IC with PFM/ PWM synchronous rectification

MB39A214A

■ DESCRIPTION

MB39A214A is a N-ch/ N-ch synchronous rectification type 2ch Buck DC/DC converter IC equipped with a bottom detection comparator for low output voltage ripple. It supports low on-duty operation to allow stable output of low voltages when there is a large difference between input and output voltages. It also allows the high switching frequency setting, enabling the downsized peripheral circuits and low-cost configuration. MB39A214A realizes ultra-rapid response and high efficiency with built-in enhanced protection features. It is most suitable for the power supply for ASIC or FPGA core, input/output devices, or memory.

■ FEATURES

- High efficiency
- Frequency setting by internal preset function : 310 kHz, 620 kHz, 1 MHz
- High accuracy reference voltage : ± 0.7% (Ta = + 25 °C)
- V_{IN} Input voltage range : 6 V to 28 V
- Output voltage setting range : 0.7 V to 5.3 V
- Possible to select the automatic PFM/PWM selection mode or PWM-fixed mode
- PAF frequency limitation function (Prohibit Audio Frequency) : > 30 kHz (Min)
- Built-in boost diode, external fly-back diode not required
- Built-in discharge FET
- Built-in over voltage protection function
- Built-in under voltage protection function
- Built-in over temperature protection function
- Built-in over current limitation function
- Soft-start circuit without load dependence
- Current sense resistor not required
- Built-in synchronous rectification type output steps for N-ch MOS FET
- Standby current : 0 µA (Typ)
- Package : TSSOP24 (4.4 mm×6.5 mm×1.2 mm [Max])

■ APPLICATIONS

- Digital TV
- Photocopiers
- STB
- BD, DVD players/recorders
- Projectors etc.

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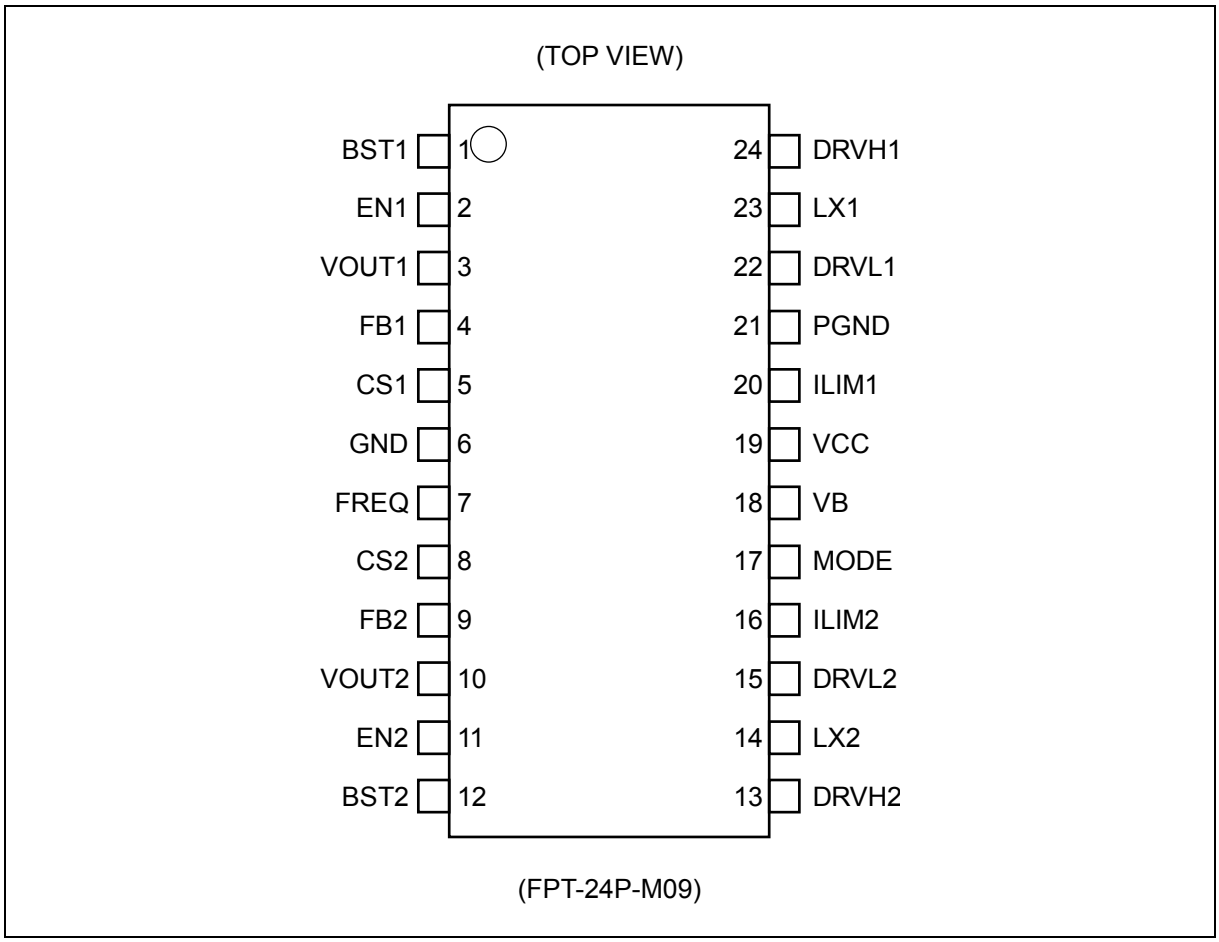
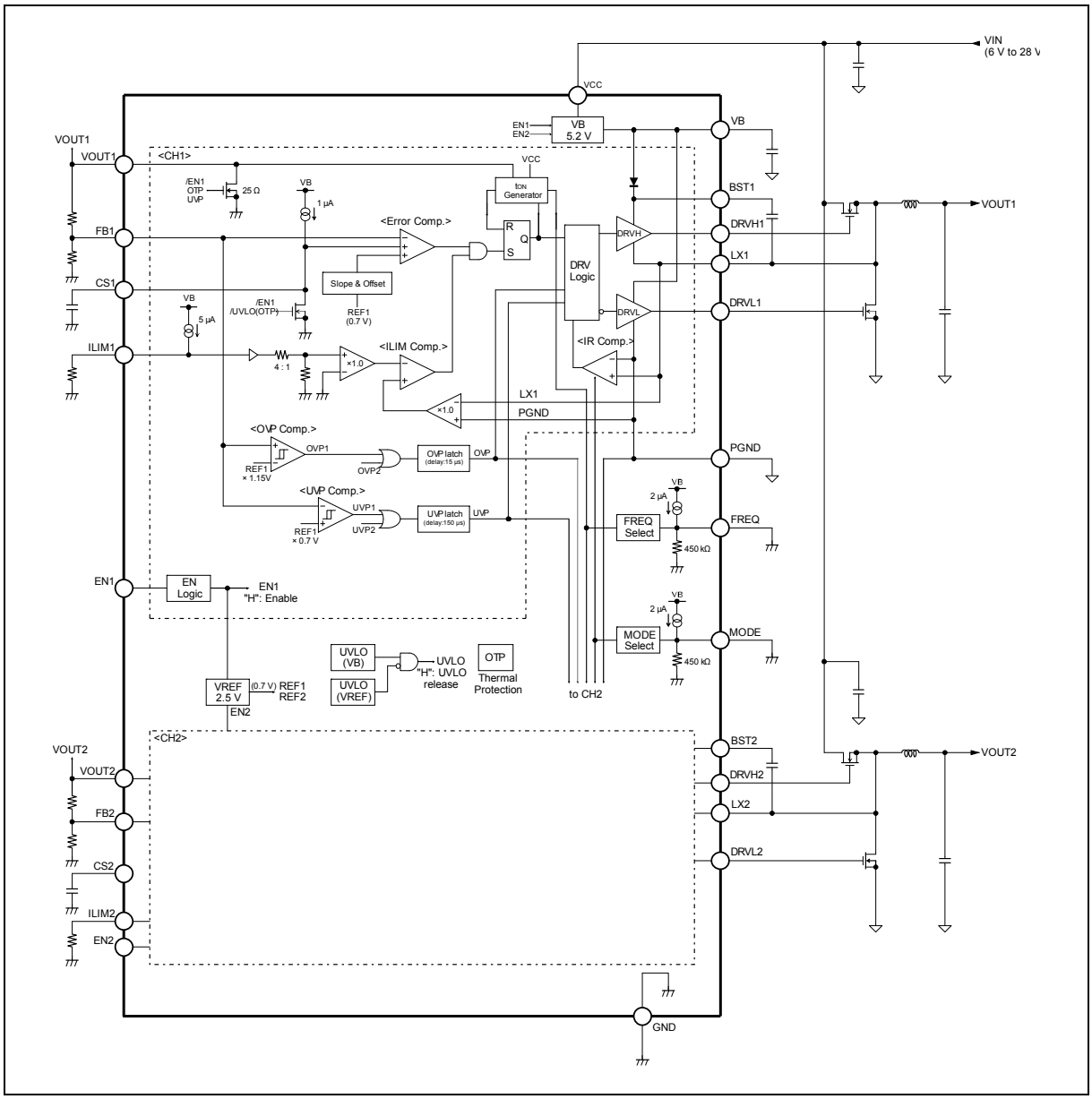
■ PIN ASSIGNMENT



■PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	BST1	—	CH1 boost capacitor connection pin.
2	EN1	I	CH1 enable pin.
3	VOUT1	I	CH1 input pin for DC/DC output voltage.
4	FB1	I	CH1 input pin for feedback voltage.
5	CS1	I	CH1 soft-start time setting capacitor connection pin.
6	GND	—	Ground pin.
7	FREQ	I	Frequency switching signal input pin. FREQ : GND Short Switching frequency 310 kHz FREQ : Open Switching frequency 620 kHz FREQ : VB Short Switching frequency 1 MHz
8	CS2	I	CH2 soft-start time setting capacitor connection pin.
9	FB2	I	CH2 input pin for feedback voltage.
10	VOUT2	I	CH2 input pin for DC/DC output voltage.
11	EN2	I	CH2 enable pin.
12	BST2	—	CH2 boost capacitor connection pin.
13	DRVH2	O	CH2 output pin for external high-side FET gate drive.
14	LX2	—	CH2 inductor and external high-side FET source connection pin.
15	DRVL2	—	CH2 output pin for external low-side FET gate drive.
16	ILIM2	I	CH2 over current detection level setting voltage input pin.
17	MODE	I	DC/DC control mode switching signal input pin. MODE : GND Short PFM/PWM MODE : Open PFM/PWM, PAF MODE : VB Short PWM fixed
18	VB	O	Internal circuit bias output pin.
19	VCC	I	Power input pin for control and output circuits.
20	ILIM1	I	CH1 over current detection level setting voltage input pin.
21	PGND	—	Ground pin for output circuit.
22	DRVL1	O	CH1 output pin for external low-side FET gate drive.
23	LX1	—	CH1 inductor and external high-side FET source connection pin.
24	DRVH1	O	CH1 output pin for external high-side FET gate drive.

■BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
VCC pin input voltage	V_{VCC}	VCC pin	− 0.3	+ 30	V
BST pin input voltage	V_{BST}	BST1, BST2 pins	− 0.3	+ 36	V
LX pin input voltage	V_{LX}	LX1, LX2 pins	− 1	+ 30	V
Voltage between BST and LX	V_{BST-LX}	—	− 0.3	+ 7	V
EN pin input voltage	V_{EN}	EN1, EN2 pins	− 0.3	+ 30	V
Input voltage	V_{FB}	FB1, FB2 pins	− 0.3	VB + 0.3	V
	V_{VOUT}	VOUT1, VOUT2 pins	− 0.3	+ 7	V
	V_{ILIM}	ILIM1, ILIM2 pins	− 0.3	VB + 0.3	V
	V_{CS}	CS1, CS2 pins	− 0.3	VB + 0.3	V
	V_{FREQ}	FREQ pin	− 0.3	VB + 0.3	V
	V_{MODE}	MODE pin	− 0.3	VB + 0.3	V
Output current	I_{OUT}	DRVH1, DRVH2 pins, DRVL1, DRVL2 pins	—	60	mA
Power dissipation	P_D	Ta ≤ + 25°C	—	+ 1282	mW
Storage temperature	T_{STG}	—	− 55	+ 125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
VCC pin input voltage	V_{VCC}	VCC pin	6	—	28	V
BST pin input voltage	V_{BST}	BST1, BST2 pins	—	—	34	V
EN pin input voltage	V_{EN}	EN1, EN2 pins	0	—	28	V
Input voltage	V_{FB}	FB1, FB2 pins	0	—	VB	V
	V_{VOUT}	VOUT1, VOUT2 pins	0	—	5.5	V
	V_{ILIM}	ILIM1, ILIM2 pins	0	—	2	V
	V_{FREQ}	FREQ pin	0	—	VB	V
	V_{MODE}	MODE pin	0	—	VB	V
Peak output current	I_{OUT}	DRVH1, DRVH2 pins, DRVL1, DRVL2 pins Duty ≤ 5% ($t = 1/f_{OSC} \times Duty$)	− 1200	—	+ 1200	mA
Operating ambient temperature	Ta	—	− 30	+ 25	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = +25°C, VCC = 12 V, EN1, EN2 = 5 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Bias Voltage Block [VB Reg.]	Output voltage	V_{VB}	18	VB = 0 A	5.04	5.20	5.36	V
	Input stability	LINE	18	VCC = 6 V to 28 V	—	10	100	mV
	Load stability	LOAD	18	VB = 0 A to − 1 mA	—	10	100	mV
	Short-circuit output current	I_{OS}	18	VB = 0 V	− 145	− 100	− 75	mA
Under voltage Lockout Protection Circuit Block [UVLO]	Threshold voltage	V_{TLH}	18	VB pin	4.0	4.3	4.6	V
		V_{THL}	18	VB pin	3.7	4.0	4.3	V
	Hysteresis width	V_H	18	VB pin	—	0.3*	—	V
Soft-Start/ Discharge Block [Soft Start, Discharge]	Charge current	I_{CS}	5,8	CS1, CS2 = 0 V	− 1.5	−1.0	− 0.75	µA
	Electrical discharge resistance	R_D	3,10	EN1, EN2 = 0 V, VOUT1, VOUT2 ≥ 0.15 V	—	25*	—	Ω
	Discharge end voltage	V_{VOVTH}	3,10	EN1, EN2 = 0 V, VOUT1, VOUT2 pins	—	0.2*	—	V
ON/OFF Time Generator Block [t_{ON} Generator]	ON time (Preset value 1)	t_{ON11}	24	FREQ pin GND connection VCC = 12 V, VOUT1 = 1.5 V	430	538	646	ns
		t_{ON21}	13	FREQ pin GND connection VCC = 12 V, VOUT2 = 1.5V	320	400	480	ns
	ON time (Preset value 2)	t_{ON12}	24	FREQ pin OPEN VCC = 12 V, VOUT1 = 1.5 V	210	263	316	ns
		t_{ON22}	13	FREQ pin OPEN VCC = 12 V, VOUT2 = 1.5 V	160	200	240	ns
	ON time (Preset value 3)	t_{ON13}	24	FREQ pin VB connection VCC = 12 V, VOUT1 = 1.5 V	130	163	196	ns
		t_{ON23}	13	FREQ pin VB connection VCC = 12 V, VOUT2 = 1.5 V	100	125	150	ns
	Minimum ON time (Preset value 1)	$t_{ONMIN11}$	24	FREQ pin GND connection VCC = 12 V, VOUT1 = 0V	—	136	191	ns
		$t_{ONMIN21}$	13	FREQ pin GND connection VCC = 12 V, VOUT2 = 0V	—	103	145	ns
	Minimum ON time (Preset value 2)	$t_{ONMIN12}$	24	FREQ pin OPEN VCC = 12 V, VOUT1 = 0V	—	77	108	ns
		$t_{ONMIN22}$	13	FREQ pin OPEN VCC = 12 V, VOUT2 = 0V	—	58	82	ns
	Minimum ON time (Preset value 3)	$t_{ONMIN13}$	24	FREQ pin VB connection VCC = 12V, VOUT1 = 0V	—	55	77	ns
		$t_{ONMIN23}$	13	FREQ pin VB connection VCC = 12 V, VOUT2 = 0V	—	43	61	ns
	Minimum OFF time	t_{OFFMIN}	24, 13	—	—	410	535	ns

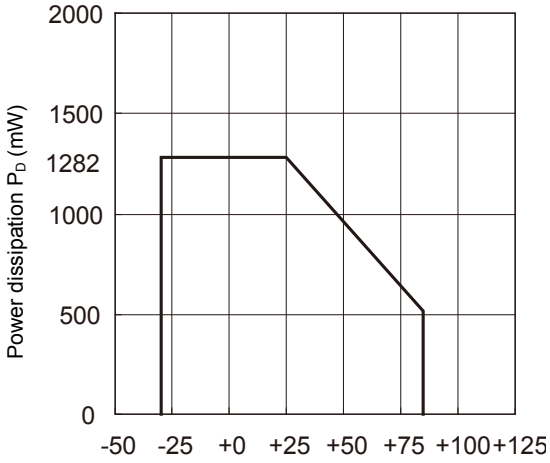
Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Error Comparison Block [Error Comp.]	Threshold voltage	V_{TH}	4, 9	Ta = +25°C	0.695	0.700	0.705	V
	FB pin input current	I_{FB}	4, 9	FB1, FB2 = 0.7 V	− 0.1	0	+0.1	µA
	VOUT pin input current	I_{VO}	3,10	VOUT1, VOUT2 = 1.5 V	—	6.0	8.6	µA
Over Current Detection Block [ILIM Comp.]	Over current detection offset voltage	$V_{OFFILIM}$	21 to 23 21 to 14	PGND − LX1, LX2 ILIM1, ILIM2 = 500 mV	− 30	0	+30	mV
	ILIM pin current	I_{ILIM}	20,16	ILIM1, ILIM2 = 0 V	− 6	− 5	− 4	µA
	ILIM pin current Temperature slope	T_{ILIM}	20,16	Ta = +25°C	—	4500*	—	ppm/°C
Over-voltage Protection Circuit Block [OVP Comp.]	Over-voltage detecting voltage	V_{OVP}	4, 9	For REF1, REF2 voltage	110	115	120	%
	Hysteresis width	V_{HOVP}	4, 9	—	—	5*	—	%
	Detection delay time	t_{OVP}	—	—	10	15	20	µs
Under-voltage Protection Circuit Block [UVP Comp.]	Under-voltage detecting voltage	V_{UVP}	4, 9	For REF1, REF2 voltage	65	70	75	%
	Hysteresis width	V_{HUVP}	4, 9	—	—	10*	—	%
	Detection delay time	t_{UVP}	—	—	100	150	200	µs
Over-temperature Protection Circuit Block [OTP]	Protection temperature	T_{OTPH}	—	—	—	150*	—	°C
		T_{OTPL}	—	—	—	125*	—	°C
Output Block [DRV]	High-side output on-resistance	R_{OH}	24,13	DRVH1, DRVH2 = − 100 mA	—	4	6	Ω
		R_{OL}	24,13	DRVH1, DRVH2 = 100 mA	—	1	1.5	Ω
	Low-side output on-resistance	R_{OH}	22,15	DRVL1, DRVL2 = − 100 mA	—	4	6	Ω
		R_{OL}	22,15	DRVL1, DRVL2 = 100 mA	—	1	1.5	Ω
	Output source current	I_{SOURCE}	24,13 22,15	LX1, LX2 = 0 V, BST1, BST2 = VB DRVH1, DRVH2 = 2.5 V Duty ≤ 5%	—	− 0.5*	—	A
	Output sink current	I_{SINK}	24,13 22,15	LX1, LX2 = 0 V, BST1, BST2 = VB DRVH1, DRVH2 = 2.5 V Duty ≤ 5%	—	0.9*	—	A
	Dead time	t_D	24 to 22 13 to 15	LX1, LX2 = 0 V, BST1, BST2 = VB DRVL1, DRVL2-low to DRVH1, DRVH2-on	15	25	35	ns
				LX1, LX2 = 0 V, BST1, BST2 = VB DRVH1, DRVH2-low to DRVL1, DRVL2-on	35	50	65	ns

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Output Block [DRV]	BST diode voltage	V_F	1,12	I_F = 10 mA	0.75	0.85	0.95	V
	Bias current	I_{BST}	1,12	LX1, LX2 = 0 V, BST1, BST2 = 5.2 V	11	15	22	µA
Switching Frequency Control Block [FREQ]	Preset value 1 conditions	V_{FREQ1}	7	FREQ pin: GND connection	0	—	0.2	V
	Preset value 2 conditions	V_{FREQ2}	7	FREQ pin: OPEN	0.6	—	1.2	V
	Preset value 3 conditions	V_{FREQ3}	7	FREQ pin: VB connection	2.4	—	VB	V
	FREQ pin output voltage	V_{FREQ}	7	FREQ = OPEN	0.63	0.9	1.17	V
PFM Control Circuit Block [MODE]	PFM/PWM mode conditions PAF function negate	V_{PFM1}	17	MODE pin: GND connection	0	—	0.2	V
	PFM/PWM mode conditions PAF function assert	V_{PFM2}	17	MODE pin : OPEN	0.6	—	1.2	V
	PWM-fixed mode conditions	V_{PWM}	17	MODE pin : VB connection	4.6	—	VB	V
	PAF frequency	f_{PAF}	—	Ta = − 30°C to +85°C	30	45	—	kHz
	MODE pin voltage	V_{MODE}	17	MODE = OPEN	0.63	0.9	1.17	V
Enable Block [EN1 , EN2]	ON condition	V_{ON}	2, 11	EN1, EN2 pins	2.64	—	—	V
	OFF condition	V_{OFF}	2, 11	EN1, EN2 pins	—	—	0.66	V
	Hysteresis width	V_H	2, 11	EN1, EN2 pins	—	0.4*	—	V
	Input current	I_{EN}	2, 11	EN1, EN2 = 5V	11	15	22	µA
Power Supply Current	Standby current	I_{CCS}	19	EN1, EN2 = 0V	—	0	10	µA
	Power supply current during idle period	I_{CC1}	19	LX1, LX2 = 0 V BST1, BST2 : VB connection FB1, FB2 = 0.75 V	—	600	860	µA
	Power supply current during operation	I_{CC2}	19	LX1, LX2 = 0V BST1, BST2 : VB connection FB1, FB2 = 0.6 V	—	1200	1700	µA

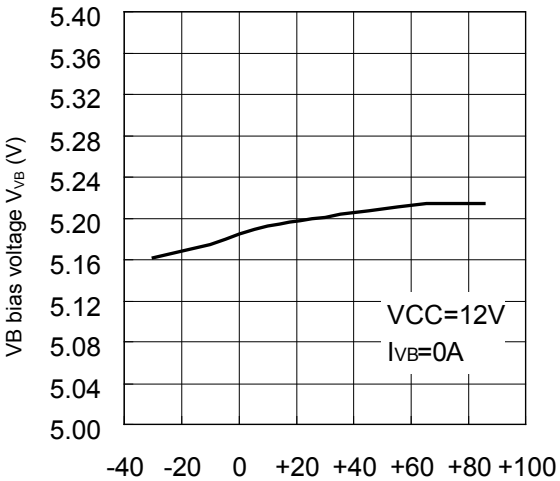
*: This parameter is not be specified. This should be used as a reference to support designing the circuits.

■ TYPICAL CHARACTERISTICS

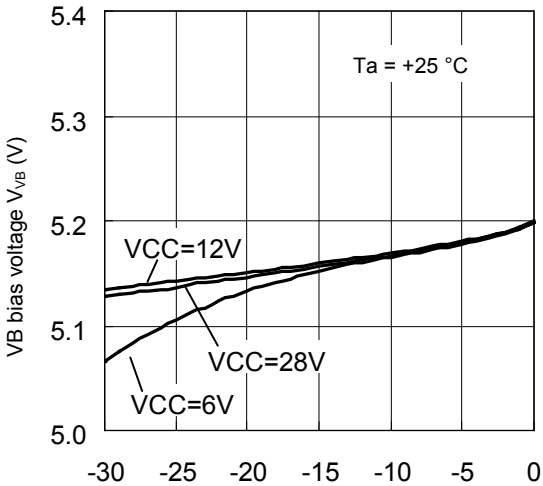
Power dissipation vs. Operating ambient temperature



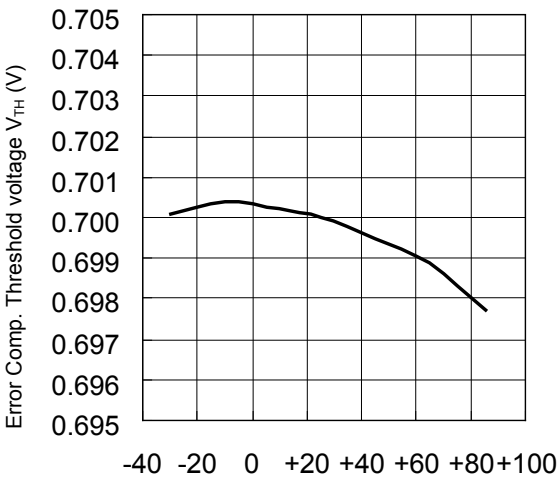
VB bias voltage vs. Operating ambient temperature



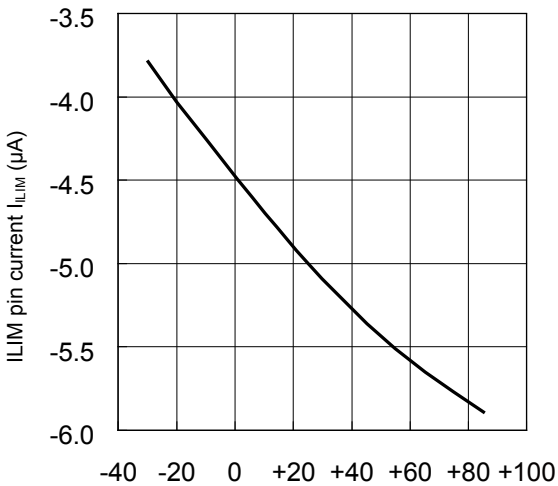
VB bias voltage vs. VB bias output current



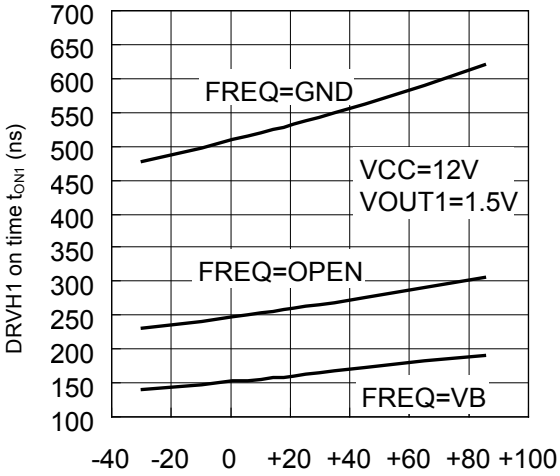
Error Comp. Threshold voltage vs. Operating ambient temperature



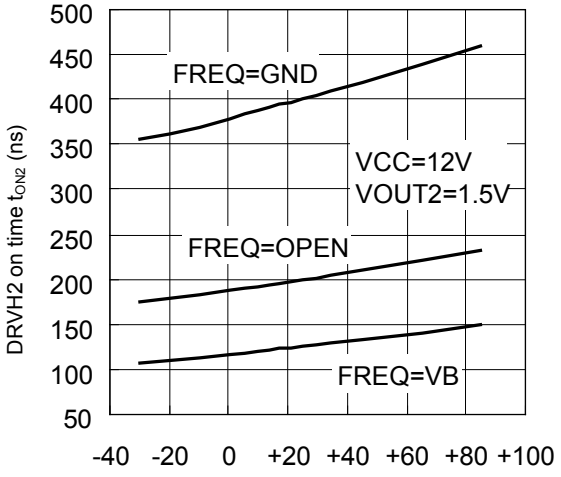
ILIM pin current vs. Operating ambient temperature



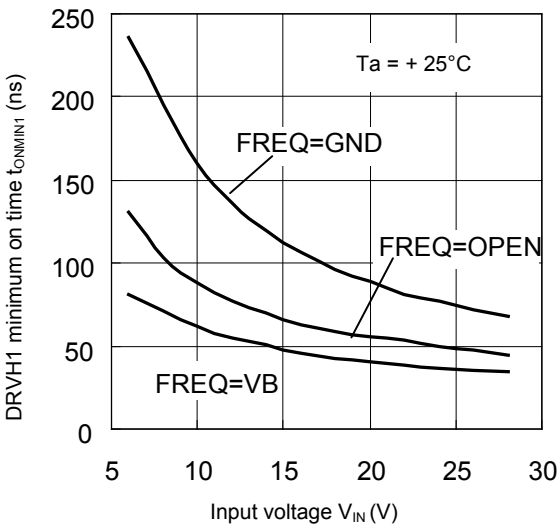
DRVH1 on time vs. Operating ambient temperature



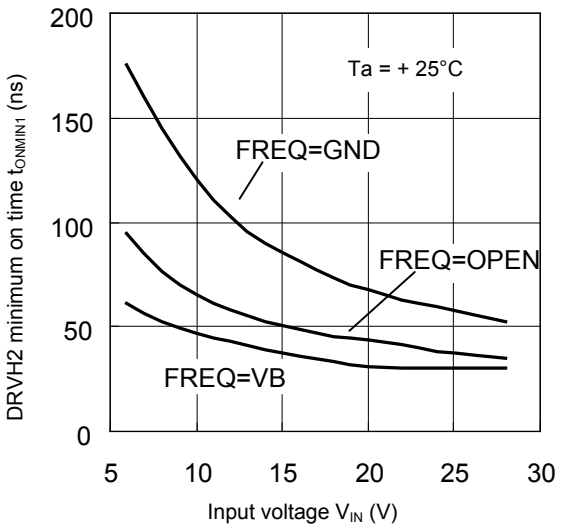
DRVH2 on time vs. Operating ambient temperature



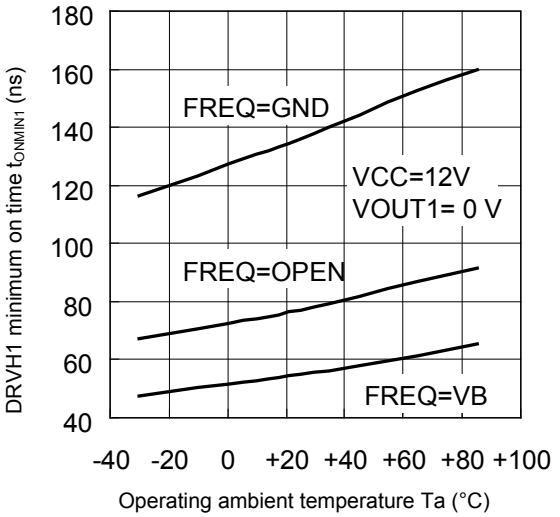
DRVH1 minimum on time vs. Input voltage



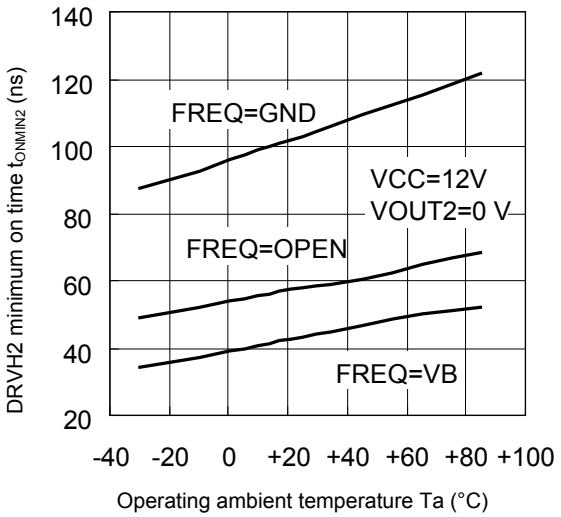
DRVH2 minimum on time vs. Input voltage



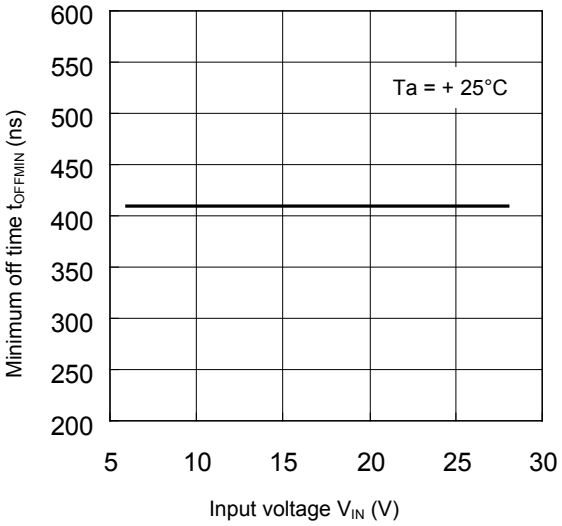
DRVH1 minimum on time vs.
Operating ambient temperature



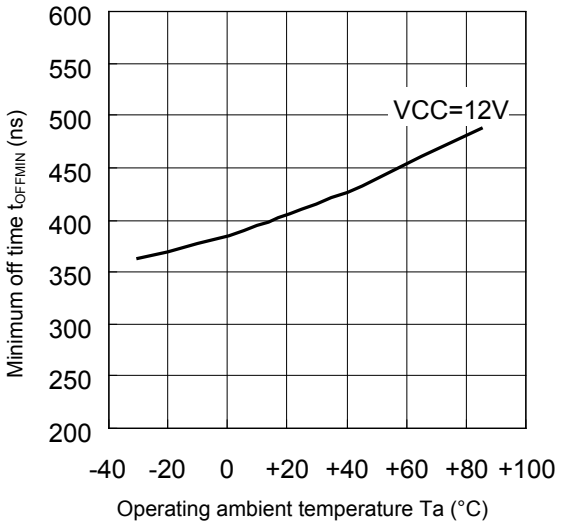
DRVH2 minimum on time vs.
Operating ambient temperature



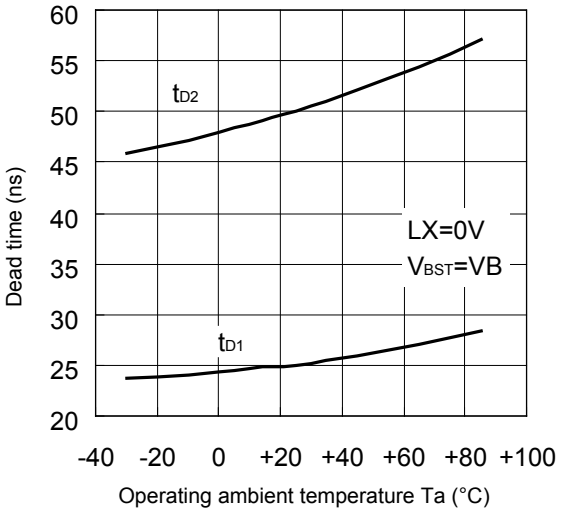
Minimum off time vs. Input voltage



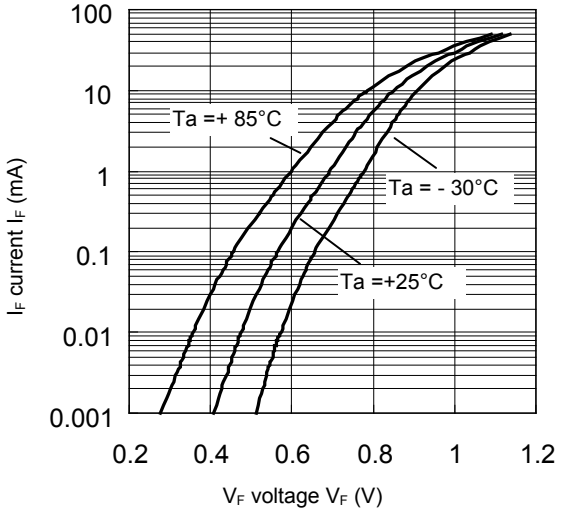
Minimum off time vs.
Operating ambient temperature



Dead time vs. Operating ambient temperature



Bootstrap diode I_F vs. V_F



t_{D1} : Period from DRVL off to DRVH on
t_{D2} : Period from DRVH off to DRVL on

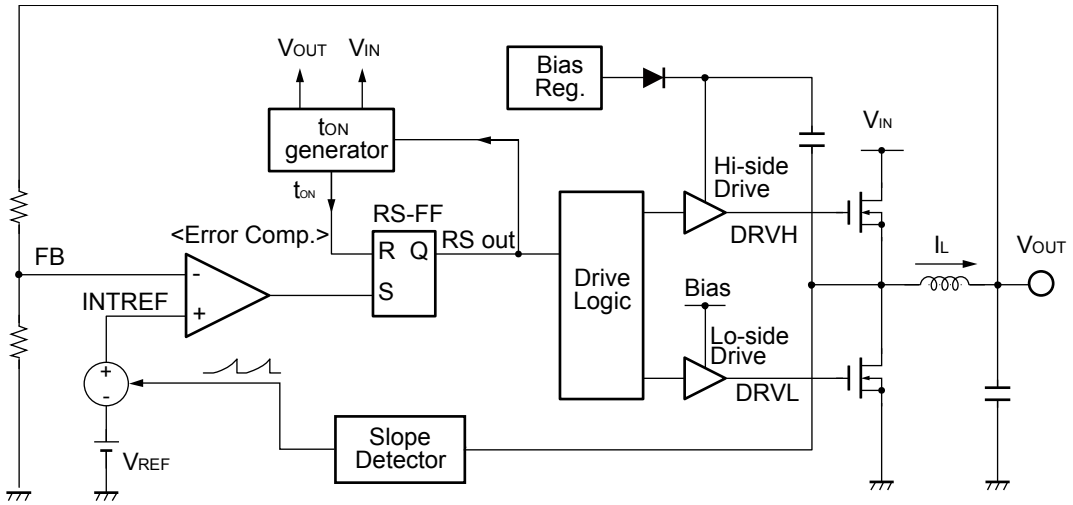
■ FUNCTION

Bottom detection comparator system for low output voltage ripple

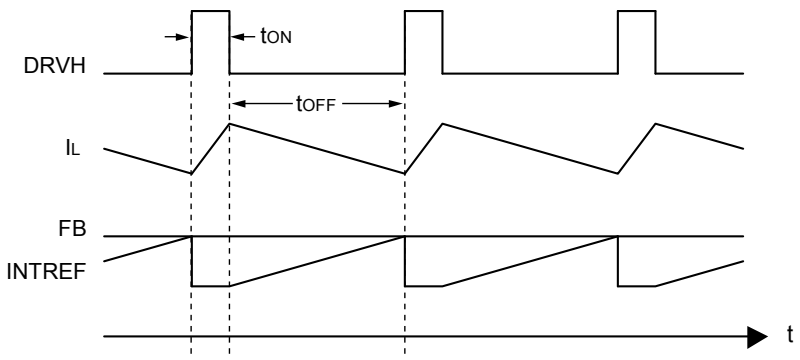
The bottom detection comparator system for low output voltage ripple determines the ON time (t_{ON}) using the input voltage (V_{IN}) and output voltage (V_{OUT}) to hold the ON state to a specified period. During the OFF period, the reference voltage (INTREF) is compared with the feedback voltage (FB) using the error comparator (Error Comp.). When the feedback voltage (FB) is below the reference voltage (INTREF) , RS-FF is set and the ON period starts again. Switching is repeated as described above. Error Comp. is used to compare the reference voltage (INTREF) with the feedback voltage (FB) to control the off-duty condition in order to stabilize the output voltage.

This system adds the inductor current slope detected during the synchronous rectification period (t_{OFF}) to the reference voltage (INTREF) , and generates an output voltage slope during the OFF period, which is essential for the bottom detection comparator system, in the IC. This enables the stable control operations under the low output voltage ripple conditions.

- Circuit diagram



- Waveforms



(1) Bias Voltage Block (VB Reg.)

The 5.2 V (Typ) bias voltage is generated from the VCC pin voltage for the control, output, and boost circuits. When either or both of the EN1 pin (pin 2) and EN2 pin (pin 11) are set to the “H” level, the system is restored from the standby state to supply the bias voltage from the VB pin (pin 18).

(2) ON/OFF Time Generator Block (t_{ON} Generator)

This block contains a capacitor for timing setting and a resistor for timing setting and generates ON time (t_{ON}) which depends on input voltage and output voltage. The switching frequency can be switched by setting the FREQ pin (pin 7) to any one of GND connection, OPEN, and VB connection. ON time for each CH is obtained from the following formula.

<FREQ pin : GND connection>

$$t_{ON1}\ (ns) = \frac{V_{VOUT1}}{V_{VIN}} \times 4300 \quad (f_{OSC1} \fallingdotseq 230\ kHz)$$

$$t_{ON2}\ (ns) = \frac{V_{VOUT2}}{V_{VIN}} \times 3200 \quad (f_{OSC2} \fallingdotseq 310\ kHz)$$

<FREQ pin : OPEN>

$$t_{ON1}\ (ns) = \frac{V_{VOUT1}}{V_{VIN}} \times 2100 \quad (f_{OSC1} \fallingdotseq 460\ kHz)$$

$$t_{ON2}\ (ns) = \frac{V_{VOUT2}}{V_{VIN}} \times 1600 \quad (f_{OSC2} \fallingdotseq 620\ kHz)$$

<FREQ pin : VB connection>

$$t_{ON1}\ (ns) = \frac{V_{VOUT1}}{V_{VIN}} \times 1300 \quad (f_{OSC1} \fallingdotseq 750\ kHz)$$

$$t_{ON2}\ (ns) = \frac{V_{VOUT2}}{V_{VIN}} \times 1000 \quad (f_{OSC2} \fallingdotseq 1000\ kHz)$$

The switching frequency of CH2 is set to 1.33 times that of CH1 to prevent the beat by the frequency difference of channel to channel.

(3) Output Block (DRV1, DRV2)

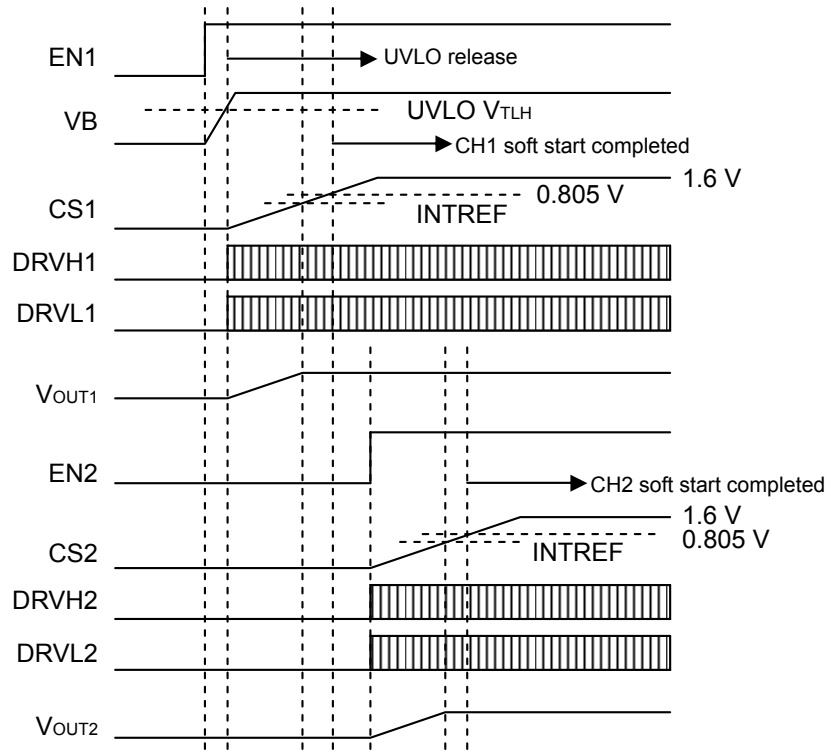
The output circuit is configured in CMOS type for both of the high-side and the low-side. It provides the 0.5 A (Typ) source current and 0.9 A (Typ) sink current, drive the external N-ch MOS FET. The output circuit of the high-side FET supplies the power from the boost circuit including the built-in boost diode. The output circuit of the low-side FET supplies the power from the VB pin. This circuit monitors the gate voltages of the high-side and low-side FETs. Until either FET is turned off, this circuit controls the ON timing of another FET, preventing the shoot-through current. The sink ON resistance of the output circuit is low 1 Ω (Typ), improve the self turn on margin of low-side FET.

(4) Starting sequence

When the EN1 pin (pin 2) or EN2 pin (pin 11) is set to the “H” level, the bias voltage is supplied from the VB pin. If the voltage of the VB pin exceeds the UVLO threshold voltage, the DC/DC converter starts operations and carries out the soft start. The soft start is a function used to prevent a rush current when the power is started.

Activating the soft start initiates charging of the capacitor connected to the CS1 pin (pin 5) and CS2 pin (pin 8) and inputs the lamp voltage to the error comparator (Error Comp.) of each channel. The DC/DC converter generates the output voltage according to that lamp voltage. This results in the soft start operation that does not depend on the output load. The over voltage protection (OVP) and under voltage protection (UVP) functions are disabled while the soft start is active.

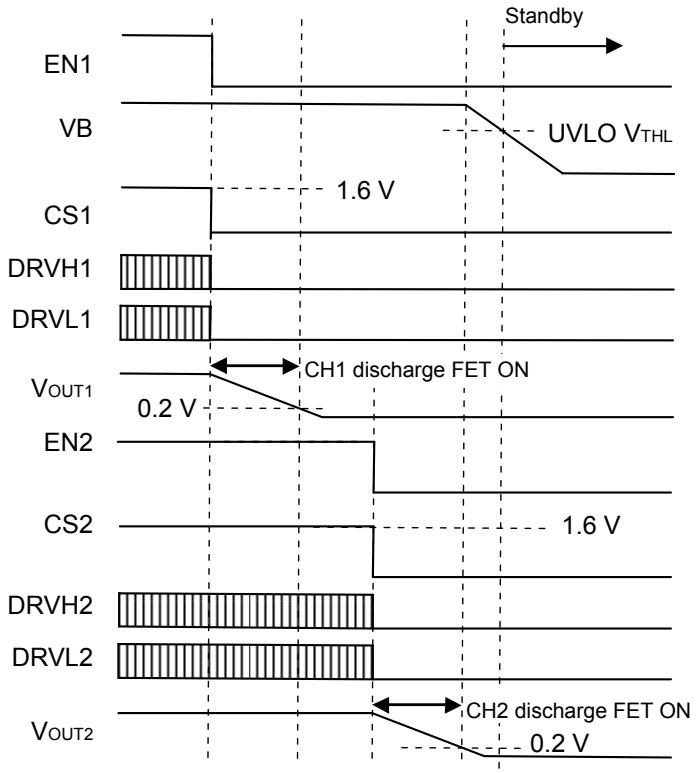
<Timing chart>



(5) DC/DC converter stop sequence (Discharge, standby)

When the EN1 pin (pin 2) or EN2 pin (pin 11) is set to the “L” level, the output capacitor is discharged using the discharge FET (R_{ON} ≒ 25 Ω) in the IC. If the voltage of the VOUT1 pin (pin 3) and VOUT2 pin (pin 10) is below 0.2 V (Typ) by discharging the output capacitor, the IC stops discharge operation. Further, if both the EN1 and EN2 pins are set to the “L” level, the IC also stops the output of the VB pin and enters the standby state after detecting UVLO. The current of the VCC pin (I_{VCC}) is then 10 µA (Max).

<Timing chart>



(6) Under Voltage Lockout Protection (UVLO)

The under voltage lockout protection (UVLO) protects ICs from malfunction and protects the system from destruction/deterioration, according to the reasons mentioned below.

- Transitional state when the bias voltage (VB) or the reference voltage (VREF) starts.
- Momentary decrease

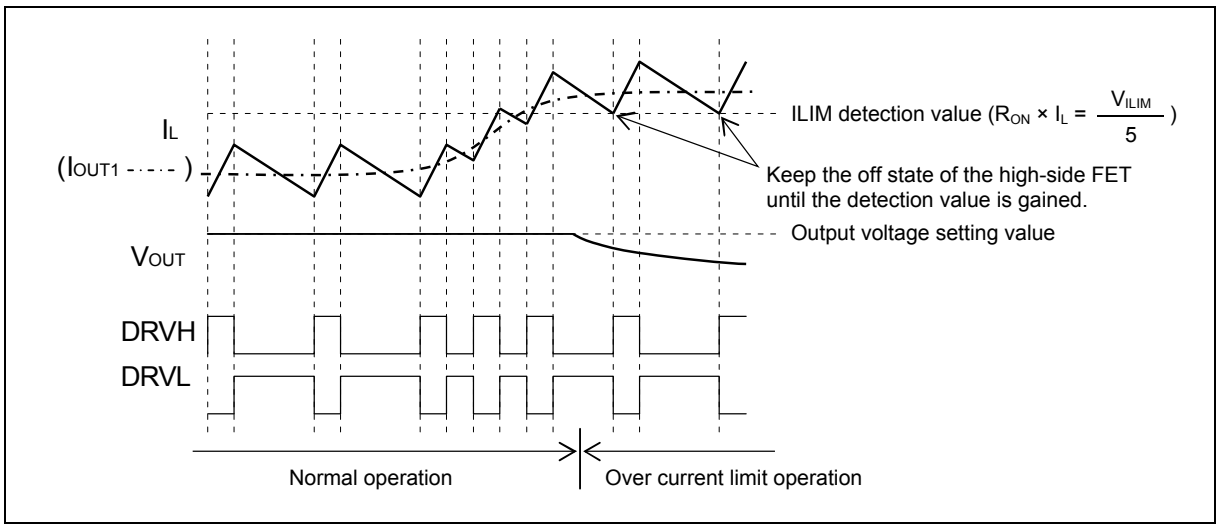
To prevent such a malfunction, this function detects a voltage drop of the VB pin (pin 18) using the comparator (UVLO Comp.), and stops IC operations.

When the VB pin exceeds the threshold voltage of the under voltage lockout protection circuit, the system is restored.

(7) Over Current Limitation (ILIM)

This function limits the output current when it has increased, and protects devices connected to the output. This function detects the inductor current I_L from the electromotive force of the low-side FET on-resistance R_{ON}, and compares this voltage with the 1/5-time value of the voltage V_{ILIM} of the ILIM1 pin (pin 20) and ILIM2 pin (pin 16) on a cyclically, using ILIM Comp. Until this voltage falls below the over current limit value, the high-side FET is held in the off state. After the voltage has fallen below the limit value, the high-side FET is placed into the on state. This limits the lower bound of the inductor current and also restricts the over current. As a result, it becomes operation that the output voltage droops.

The over current limit value is set by connecting the resistor to the ILIM pin. The ILIM pin supplies the constant current of 5 µA (Typ) . However, the current value has a temperature slope up to 4500 ppm/°C to compensate the temperature dependence characteristics of the low-side FET on-resistance.



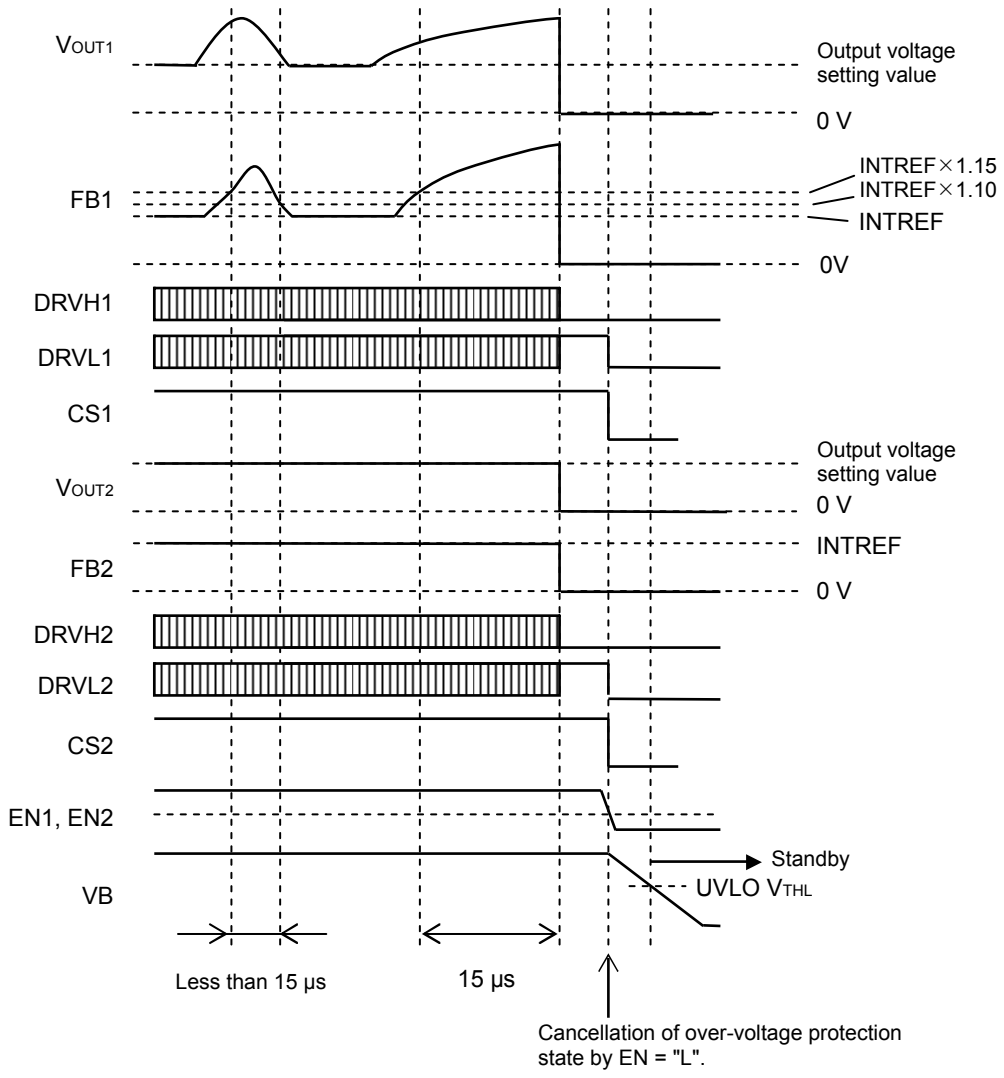
(8) Over Voltage Protection (OVP)

This function stops the output voltage when the output voltage has increased, and protects devices connected to the output.

1. Using OVP Comp, this function makes a comparison between the voltage which is 1.15 times (Typ) of the internal reference voltage INTREF1 and INTREF2 (0.7 V), and the feedback voltage for the FB1 pin (pin 4) and the FB2 pin (pin 9).
2. If the feedback voltage mentioned in 1 detects the higher state by 15µs (Typ) or more, the operations below will be performed.
   - Set the RS latch.
   - Set the DRVH1 pin (pin 24) and the DRVH2 pin (pin 13) to the “L” level.
   - Set the DRVL1 pin (pin 22) and the DRVL2 pin (pin 15) to the “H” level.

These operations fix the high-side FET to the off state and the low-side FET to the on state for both channels of the DC/DC converter, and stops switching (latch stop).The over-voltage protection state can be cancelled by setting both the EN1pin (pin 2) and EN2 pin (pin 11) to the “L” level or reducing the VCC power once until the bias voltage (VB) falls below V_{THL} of UVLO.

<Timing chart>



(9) Under Voltage Protection (UVP)

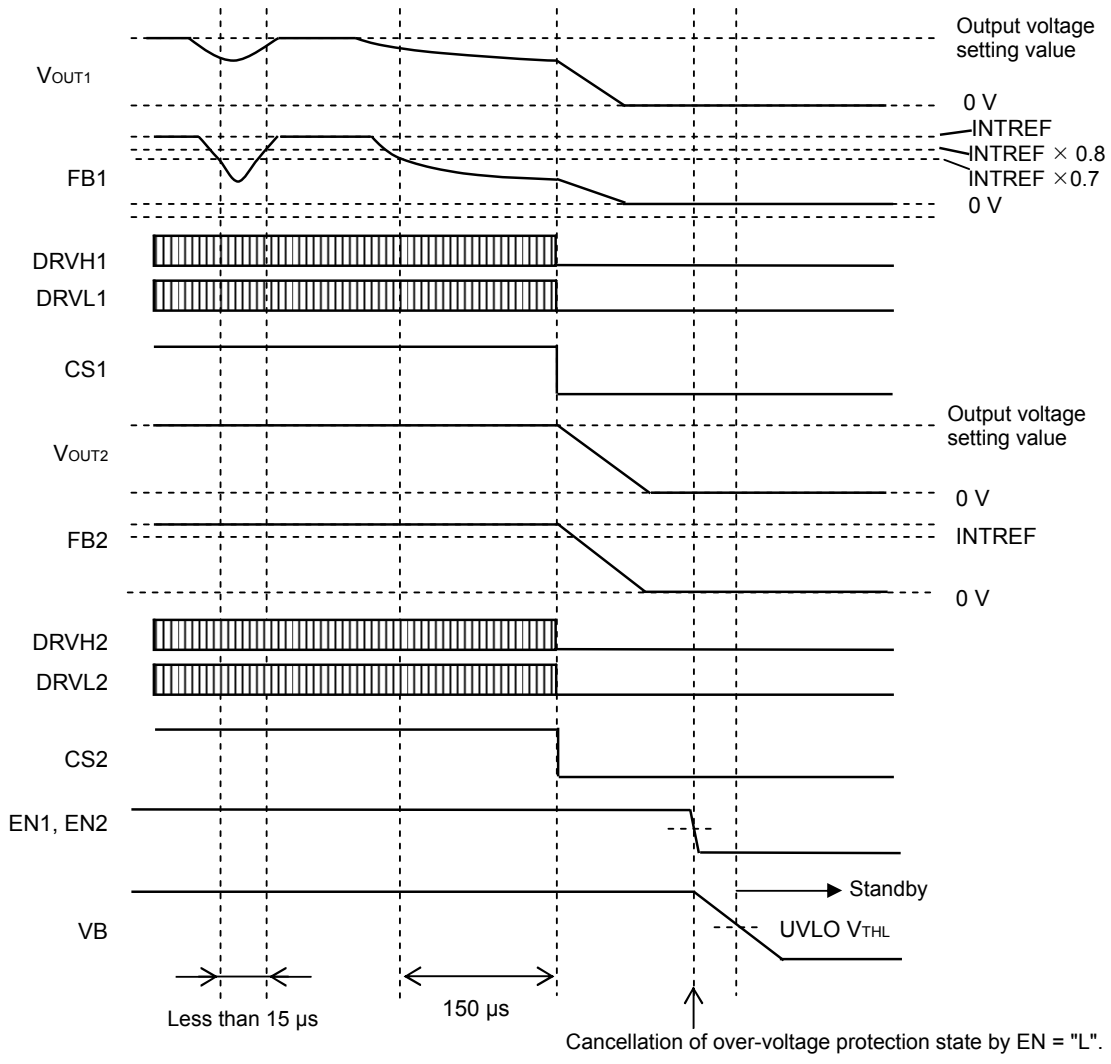
This function stops the output voltage when the output voltage has lowered, and protects devices connected to the output.

1. Using UVP Comp, this function makes a comparison between the voltage which is 0.7 times (Typ) of the internal reference voltage REF1, REF2 (0.7 V), and the feedback voltage for the FB1 pin (pin 4) and the FB2 pin (pin 9).
2. If the feedback voltage mentioned in 1 detects the higher state by 150µs (Typ) or more, the operations below will be performed.
   - Set the RS latch.
   - Set the DRVH1 pin (pin 24) and the DRVH2 pin (pin 13) to the “L” level.
   - Set the DRVL1 pin (pin 22) and the DRVL2 pin (pin 15) to the “L” level.

These operations fix the high-side FET to the off state and the low-side FET to the off state for both channels of the DC/DC converter, and stops switching (latch stop). The discharge operation is then carried out to discharge the output capacitor (The discharge operation continues until the state of the under-voltage protection is released).

The under-voltage protection state can be cancelled by setting both the EN1 pin (pin 2) and EN2 pin (pin 11) to the “L” level or reducing the VCC power once until the bias voltage (VB) falls below V_{THL} of UVLO.

<Timing chart>



(10) Over Temperature Protection (OTP)

The over-temperature protection circuit block (OTP) provides a function that prevents the IC from a thermal destruction. If the junction temperature reaches + 150°C, the DRVH1 pin (pin 24) and DRVH2 pin (pin 13) are set to the “L” level, and the DRVL1 pin (pin 22) and DRVL2 pin (pin 15) are set to the “L” level. This fixes the high-side and low-side FETs to the off-state, of both channels in the DC/DC converter, causing switching to be stopped. The discharge operation is then carried out to discharge the output capacitor (The discharge operation continues until the state of the over-temperature protection is released). If the junction temperature drops to + 125°C, the soft start is reactivated. (Restored automatically.)

(11) Operation mode

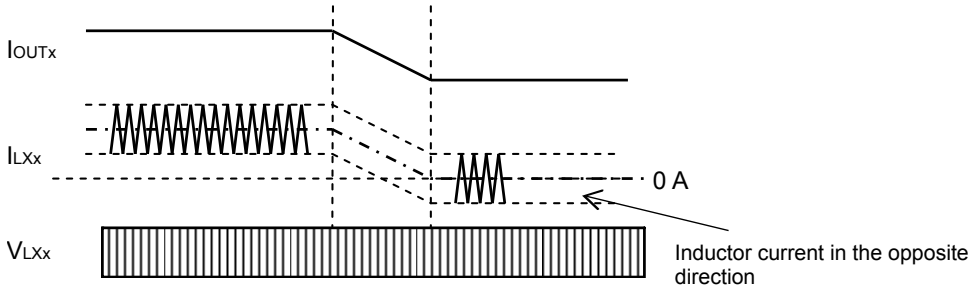
In the PWM-fixed mode, the system acts by the switching frequency specified with the FREQ pin regardless of the load.

In the automatic PFM/PWM selection mode, the switching frequency is reduced at low load, for enhancing the conversion efficiency characteristics. This function detects 0 A of the inductor current from the electromotive force of the low-side FET ON resistance when the low-side FET ON state, and places the low-side FET into the off state. This idle period continued until the output voltage decreased, this results the switching frequency being reduced automatically depending on the load current when the inductor current is below the critical current. The system acts by the switching frequency specified with the FREQ pin, when the inductor current exceeds the critical current.

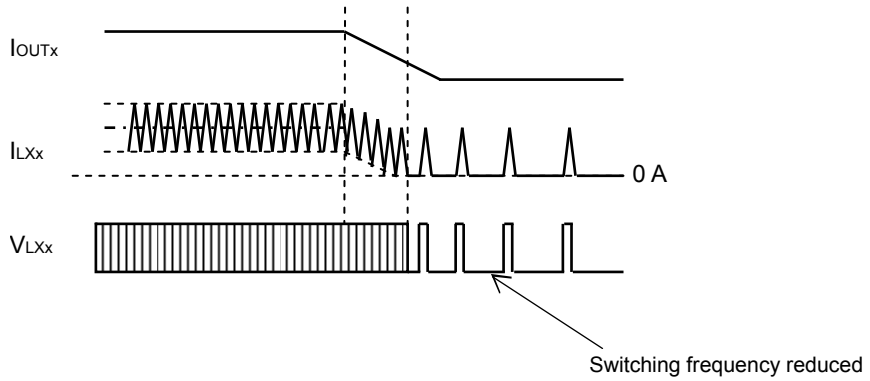
For Automatic PFM/PWM selection mode with PAF function, the switching frequency at low load is held to 30 kHz (Min) or more.

The operation mode can be switched by setting the MODE pin (pin 17) to any one of GND connection, OPEN, and VB connection.

- PWM-fixed mode



- Automatic PFM/PWM selection mode



X : Each channel number

- Enable function table

EN1 pin	EN2 pin	DC/DC converter (CH1)	DC/DC converter (CH2)
L	L	OFF	OFF
H	L	ON	OFF
L	H	OFF	ON
H	H	ON	ON

- DC/DC Control mode function table

MODE pin	DC/DC control
GND connection	Automatic PFM/PWM selection mode
OPEN	Automatic PFM/PWM selection mode with PAF function
VB connection	PWM-fixed mode

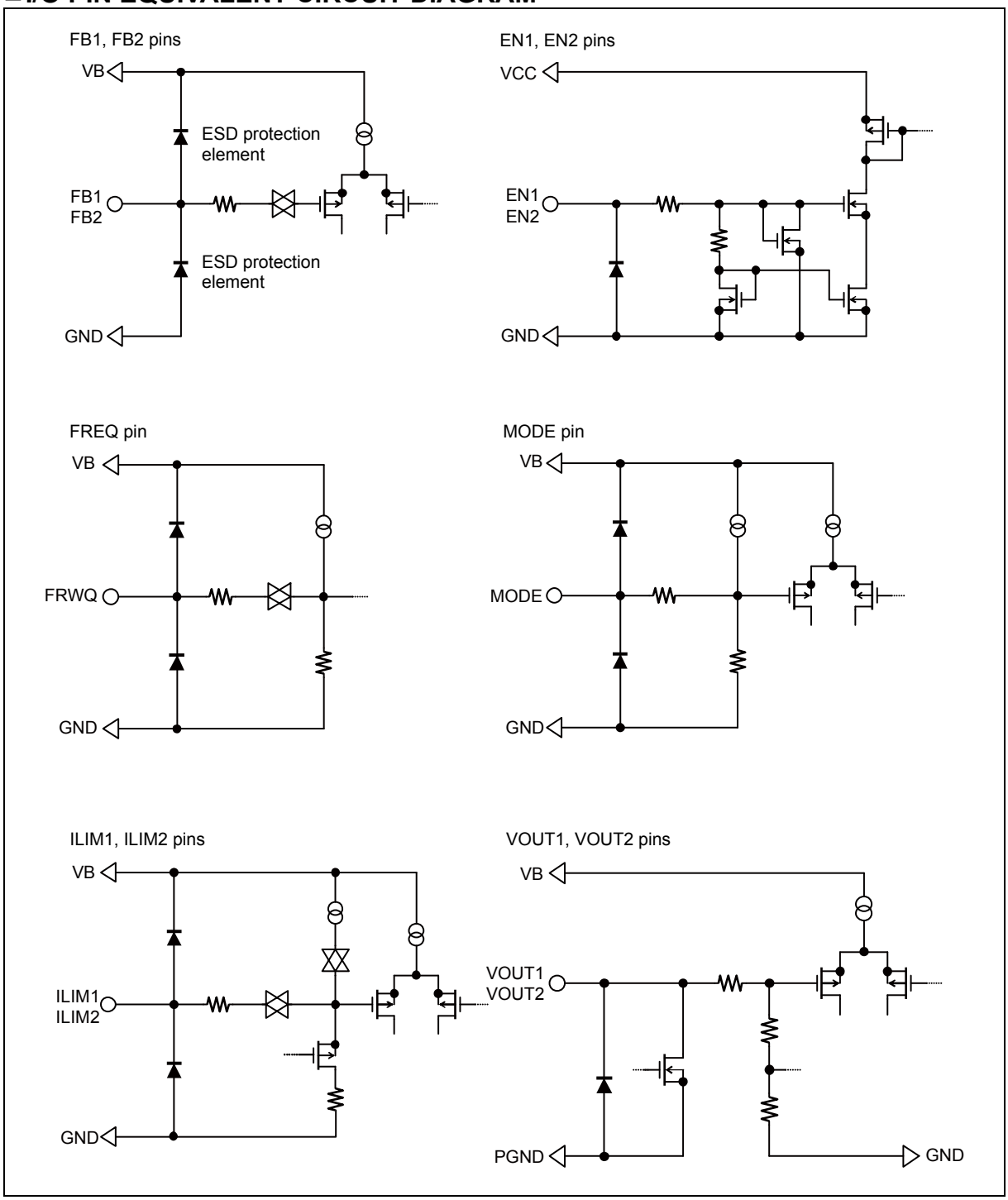
- Switching frequency control function table

FREQ pin	Switching frequency
GND connection	f_{OSC1} ≒ 230 kHz, f_{OSC2} ≒ 310 kHz
OPEN	f_{OSC1} ≒ 460 kHz, f_{OSC2} ≒ 620 kHz
VB connection	f_{OSC1} ≒ 750 kHz, f_{OSC2} ≒ 1000 kHz

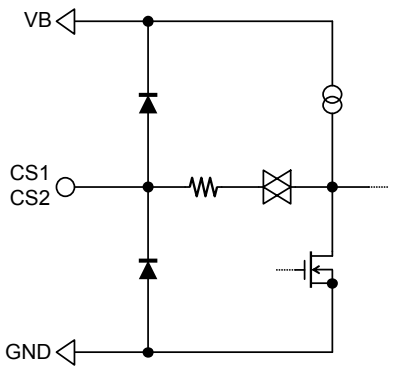
- Protection function table
  The following table shows the state of the VB pin (pin 18), the DRVH1 pin (pin 24), the DRVH2 pin (pin 13), the DRVL1 pin (pin 22), the DRVL2 pin (pin 15) when each protection function operates.

Protection function	Detection condition	Output of each pin after detection			DC/DC output dropping operation
		VB	DRVH1, DRVH2	DRVL1, DRVL2	
Under Voltage Lockout Protection (UVLO)	VB < 4.0 V	—	L	L	Natural electric discharge
Over-current limitation (ILIM)	V_{PGND} - V_{LX1}, V_{LX2} > V_{ILIM1}, V_{ILIM2}	5.2 V	Switching	Switching	The voltage is dropped by the constant current
Over Voltage Protection (OVP)	V_{FB1}, V_{FB2} > INTREF1, INTREF2×1.15 (15 µs or higher)	5.2 V	L	H	0 V clamping
Under Voltage Protection (UVP)	V_{FB1}, V_{FB2} > INTREF1, INTREF2×0.7 (150 µs or higher)	5.2 V	L	L	Electrical discharge by discharge function
Over Temperature Protection (OTP)	Tj > + 150 °C	5.2 V	L	L	Electrical discharge by discharge function
Enable (EN)	EN1, EN2: H → L (V_{OUT1}, V_{OUT2} > 0.2 V)	5.2 V	L	L	Electrical discharge by discharge function

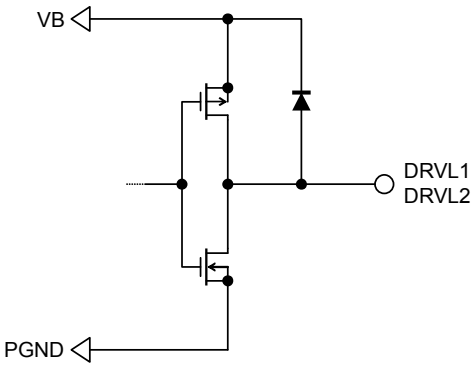
■I/O PIN EQUIVALENT CIRCUIT DIAGRAM



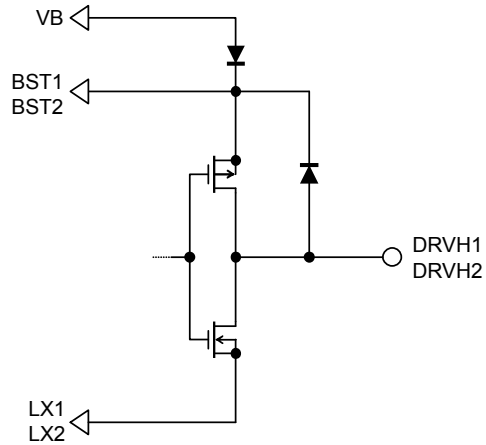
CS pin



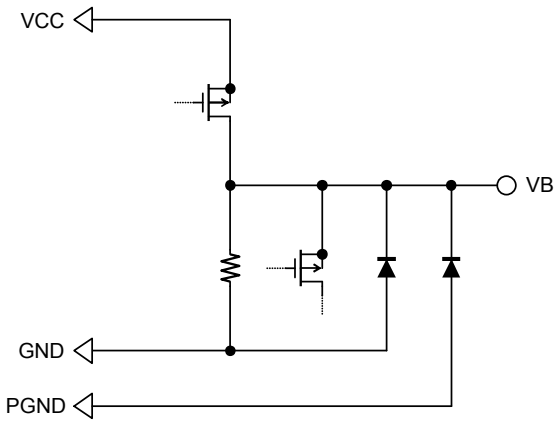
DRVL1, DRVL2 pins



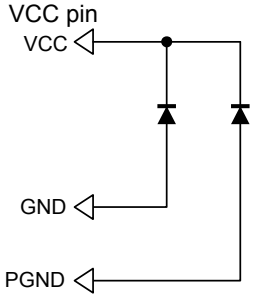
DRVH1, DRVH2, BST1, BST2, LX1, LX2 pins



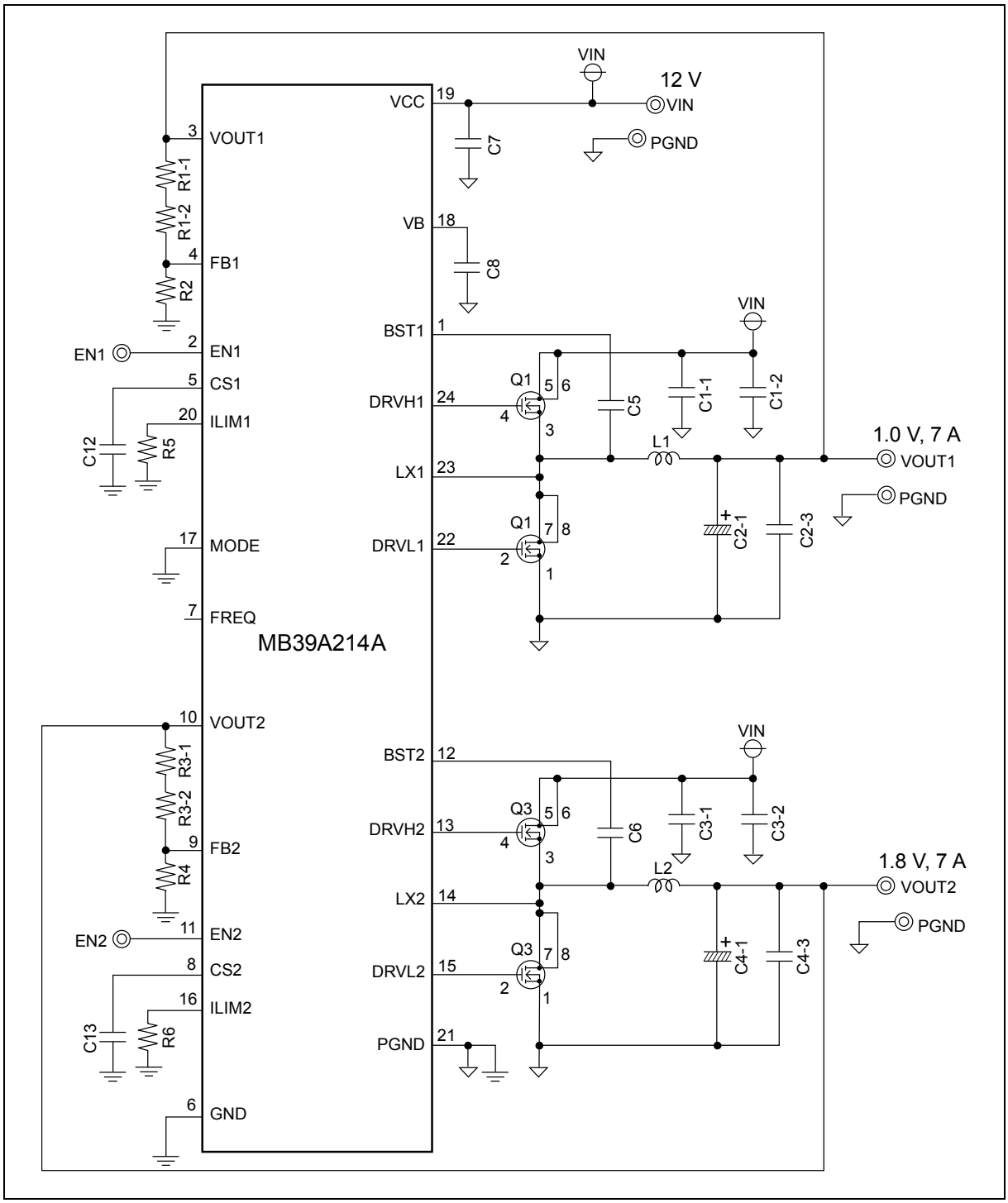
VB pin



VCC pin



■ EXAMPLE APPLICATION CIRCUIT



■PART LIST

Component	Item	Specification	Vendor	Package	Part number	Remarks
Q1	N-ch FET	V_{DS} = 30 V, I_D = 9 A, 5.4 A, R_{ON} = 34 mΩ, 13 mΩ	RENESAS	SOP8	µPA2758	DualType (2elements)
Q3	N-ch FET	V_{DS} = 30 V, I_D = 9 A, 5.4 A, R_{ON} = 34 mΩ, 13 mΩ	RENESAS	SOP8	µPA2758	DualType (2elements)
L1	Inductor	1 µH (18 A)	NEC TOKIN	-	MPC1055L1R0	
L2	Inductor	1.5 µH (12.4 A)	NEC TOKIN	-	MPLC1040L1R5	
C1-1	Ceramic capacitor	10 µF (25 V)	MURATA	3216	GRM31CB31E106K	
C1-2	Ceramic capacitor	10 µF (25 V)	MURATA	3216	GRM31CB31E106K	
C2-1	POSCAP	220 µF (2 V)	SANYO	D case	2TPLF220M6	
C2-3	Ceramic capacitor	1000 pF (50 V)	TDK	1608	C1608JB1H102K	
C3-1	Ceramic capacitor	10 µF (25 V)	MURATA	3216	GRM31CB31E106K	
C3-2	Ceramic capacitor	10 µF (25 V)	MURATA	3216	GRM31CB31E106K	
C4-1	POSCAP	150 µF (6.3 V)	SANYO	D case	6TPL150MU	
C4-3	Ceramic capacitor	1000 pF (50 V)	TDK	1608	C1608JB1H102K	
C5	Ceramic capacitor	0.1 µF (50 V)	TDK	1608	C1608JB1H104K	
C6	Ceramic capacitor	0.1 µF (50 V)	TDK	1608	C1608JB1H104K	
C7	Ceramic capacitor	0.1 µF (50 V)	TDK	1608	C1608JB1H104K	
C8	Ceramic capacitor	4.7 µF (16 V)	TDK	1608	C1608JB1C475K	
C12	Ceramic capacitor	3300 pF (50 V)	TDK	1608	C1608JB1H332K	
C13	Ceramic capacitor	3300 pF (50 V)	TDK	1608	C1608JB1H332K	
R1-1	Resistor	1.6 kΩ	SSM	1608	RR0816P162D	
R1-2	Resistor	27 kΩ	SSM	1608	RR0816P273D	
R2	Resistor	68 kΩ	SSM	1608	RR0816P683D	
R3-1	Resistor	0.047 kΩ	SSM	1608	RR0816P470D	
R3-2	Resistor	56 kΩ	SSM	1608	RR0816P563D	
R4	Resistor	36 kΩ	SSM	1608	RR0816P363D	
R5	Resistor	110 kΩ	SSM	1608	RR0816P114D	
R6	Resistor	120 kΩ	SSM	1608	RR0816P124D	

RENESAS : Renesas Electronics Corporation
SANYO : SANYO Electric Co., Ltd
NEC TOKIN : NEC TOKIN Corporation
TDK : TDK Corporation
MURATA : Murata Manufacturing Co., Ltd.
SSM : SUSUMU Co.,Ltd.

■ APPLICATION NOTE

1. Setting Operating Conditions

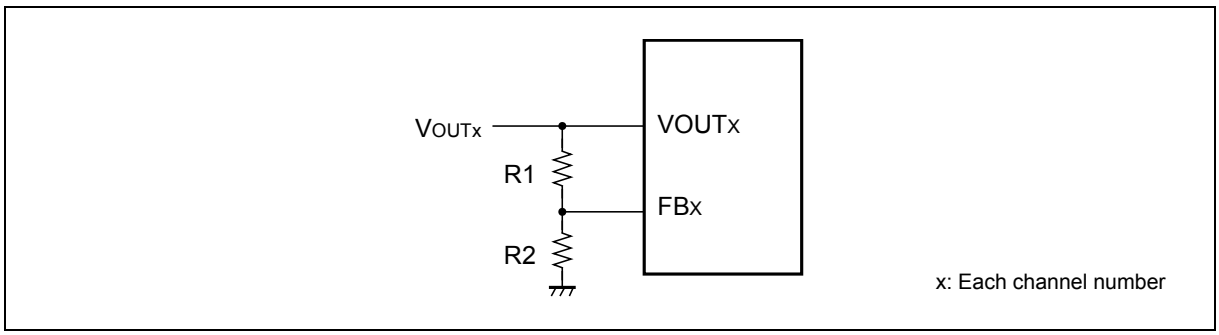
Setting output voltages

The output voltage can be set by adjusting the setting output voltage resistor ratio. Setting output voltage is calculated by the following formula.

$$V_{OUTx} = \frac{R1 + R2}{R2} \times (0.6946 + 0.2667 \times \Delta I_L \times (1 - \frac{2.8 \times 10^{-7}}{t_{OFF}}) \times R_{ON\_Sync}) + \frac{\Delta V_{OUTx}}{2}$$

$$\Delta V_{OUTx} = ESR \times \Delta I_L, \Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN} \times f_{OSC}}, t_{OFF} = \frac{(V_{IN} - V_{OUTx})}{V_{IN} \times f_{OSC}}$$

V_{OUTx}	: Output setting voltage [V]
V_{IN}	: Power supply voltage [V]
ΔV_{OUTX}	: Output ripple voltage value [V]
t_{OFF}	: Off time [s]
R_{ON_Sync}	: ON resistance of low-side FET [Ω]
ΔI_L	: Ripple current peak-to-peak value of inductor [A]
ESR	: Series resistance element of output capacitor [Ω]
L	: Inductor value [H]
f_{OSC}	: Switching frequency [Hz]



The total resistor value (R1+R2) of the setting output resistor should be selected up to 100 kΩ.

Minimum power supply voltage

The maximum on duty is limited by "the minimum off time (t_{OFFMIN}) that an IC holds without fail as a fixed value" and "the on time (t_{ON}) determined by the power voltage value and the output voltage setting value". The ratio between the output voltage and the power voltage must be less than the maximum on duty.

The minimum power supply voltage that is required to sustain the output voltage can be calculated by the following formula.

$$V_{IN\_MIN} = \frac{(V_{OUT} + I_{OUT\_MAX} \times (RDC + R_{ON\_Main})) \times V_{OUT}}{V_{OUT} - (V_{OUT} + I_{OUT\_MAX} \times (RDC + R_{ON\_Sync})) \times t_{OFF\_MIN} \times f_{OSC} \times 1.2}$$

V_{IN_MIN} : Power supply voltage [V]
V_{OUT} : Output setting voltage [V]
I_{OUT_MAX} : Maximum load current value [A]
R_{ON_Main} : ON resistance of high-side FET [Ω]
R_{ON_Sync} : ON resistance of low-side FET [Ω]
RDC : Series resistance of inductor [Ω]
f_{OSC} : Switching frequency setting value [Hz]
t_{OFF_MIN} : Minimum off time (Maximum value) [s]
(For the minimum off time, see “ON/OFF Time [Minimum OFF time] ” in “■ELECTRICAL CHARACTERISTICS”.)

Use the smaller switching frequency setting in order to make the voltage output possible with the lower power voltage.

Slope voltages

It is necessary to sustain the Slope voltage 15 mV or higher in order to obtain the stable switching cycle. The Slope voltage can be calculated by the following formula.

$$V_{Slope} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT} \times R_{ON\_Sync}}{L \times V_{IN} \times f_{OSC}}$$

V_{Slope} : Slope voltage [V]
V_{IN} : Power supply voltage [V]
V_{OUT} : Output setting voltage [V]
f_{OSC} : Switching frequency [Hz]
R_{ON_Sync} : ON resistance of low-side FET [Ω]
L : Inductor value [H]

Setting soft-start time

Calculate the soft-start time by the following formula.

$$t_s = 7 \times 10^5 \times C_{CS}$$

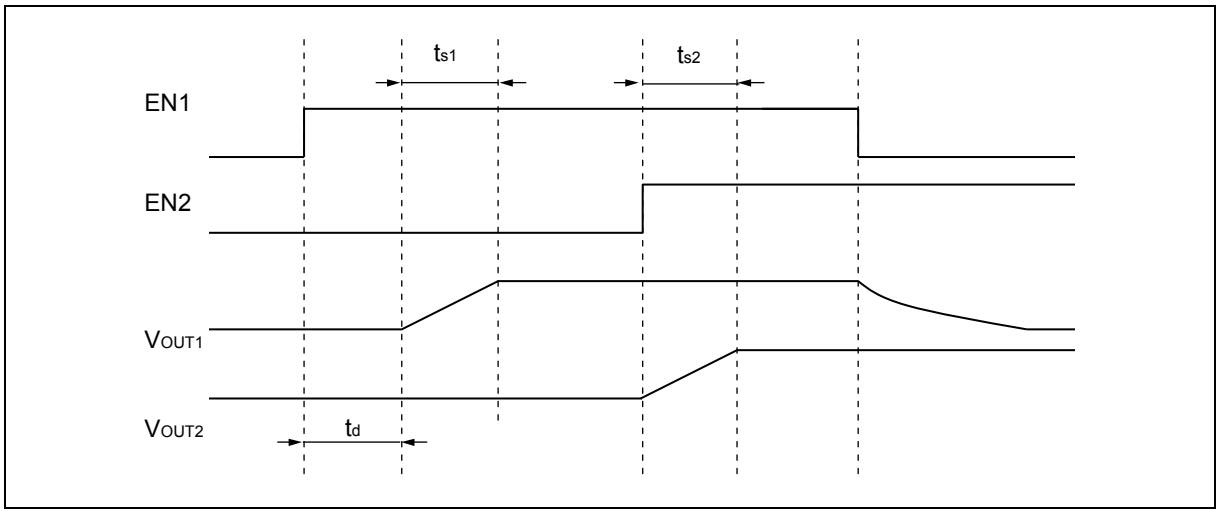
t_s : Soft-start time [s] (time until output reaches 100%)
C_{CS} : CS pin capacitor value [F]

Calculate the delay time until the soft-start activation by the following formula.

$$t_d = 43 \times C_{VB}$$

t_d : VB voltage delay time (at V_{IN} = 12 V) [s]
C_{VB} : VB pin capacitor value [F]

When activating the other in the state where a side channel has already been activated (UVLO release: VB output already), the delay time is hardly generated.



Setting switching frequency

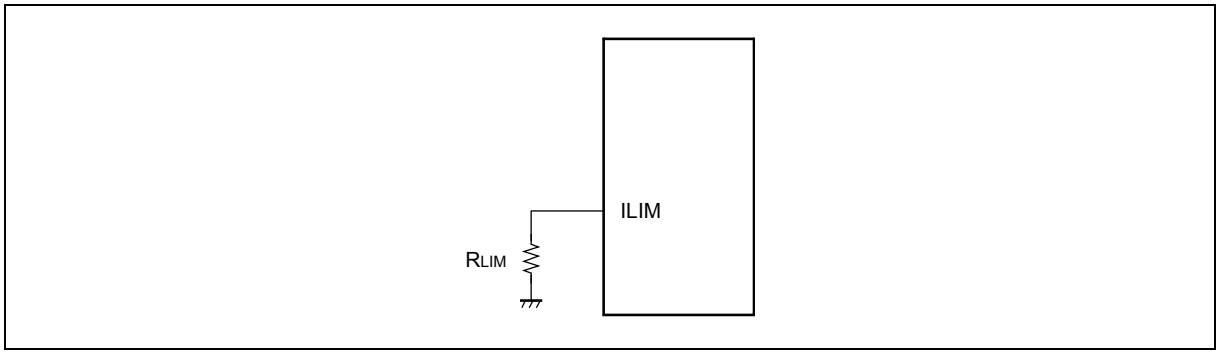
The switching frequency is set at the FREQ pin. As for the setting process, see the switching frequency control function table.

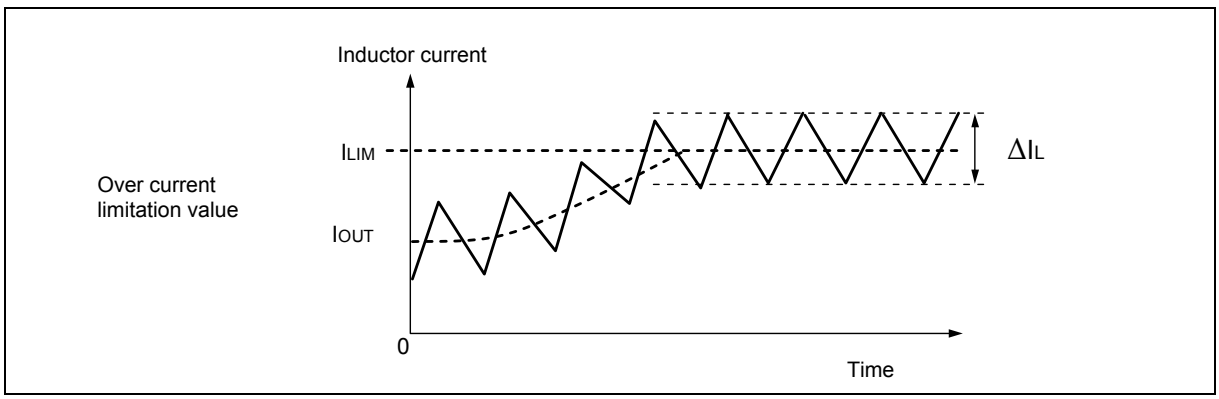
Setting over current limitation

The over current limitation value can be set by adjusting the over current limitation setting resistor value connected to the ILIM pin.
Calculate the resistor value by the following formula.

$$R_{LIM} = 10^6 \times R_{ON\_Sync} \times (I_{LIM} - \frac{\Delta I_L}{2})$$

R_{LIM}	: Over current limitation value setting resistor [Ω]
I_{LIM}	: Over current limitation value [A]
ΔI_L	: Ripple current peak-to-peak value of inductor [A]
R_{ON_Sync}	: ON resistance of low-side FET [Ω]



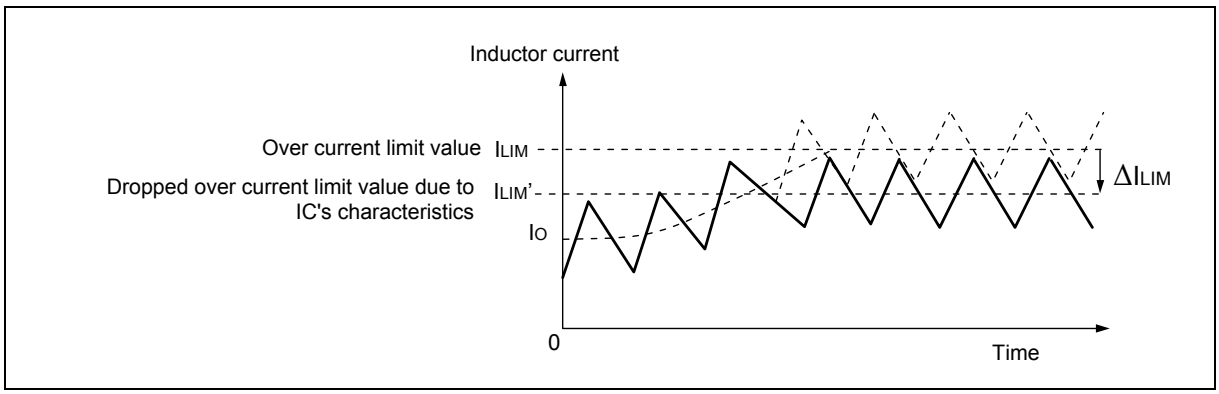


If the rate of inductor saturation current is small, the inductor value decreases and the ripple current of inductor increase when the over-current flows. At that time there is a possibility that the limited output current increases or is not limited, because the bottom of inductor current is detected. It is necessary to use the inductor that has enough large rate of inductor saturation current to prevent the overlap current.

The over current limit value is affected by ILIM pin source current and over current detection offset voltage in the IC except for the on resistance of the low-side FET and the inductor value. The variation of dropped over current limit value caused by IC characteristics is calculated by the following formula.

$$\Delta I_{LIM} = \frac{2 \times 10^{-7} \times R_{LIM} + 0.03}{R_{ON\_Sync}}$$

ΔI_{LIM} : The variation of dropped over current limit value [A]
R_{LIM} : Over current limitation value setting resistor [Ω]
R_{ON_Sync} : ON resistance of low-side FET [Ω]



The over current detection value needs to set a sufficient margin against the maximum load current.

Power dissipation and the thermal design

IC's loss increases, if IC is used under the high power supply voltage, high switching frequency, high load and high temperature. The IC internal loss can be calculated by the following formula.

$$P_{IC} = V_{CC} \times (I_{CC} + Q_{G\_Total1} \times f_{OSC1} + Q_{G\_Total2} \times f_{OSC2})$$

P_{IC} : IC internal loss [W]
V_{CC} : Power supply voltage (V_{IN}) [V]
I_{CC} : Power supply current [A] (2 mA Max)
Q_{G_Total1} : Total quantity of charge for the high-side FET and the low-side FET of each CH1 [C]
Q_{G_Total2} : Total quantity of charge for the high-side FET and the low-side FET of each CH2 [C]
f_{OSC1} : CH1 switching frequency [Hz]
f_{OSC2} : CH2 switching frequency [Hz]

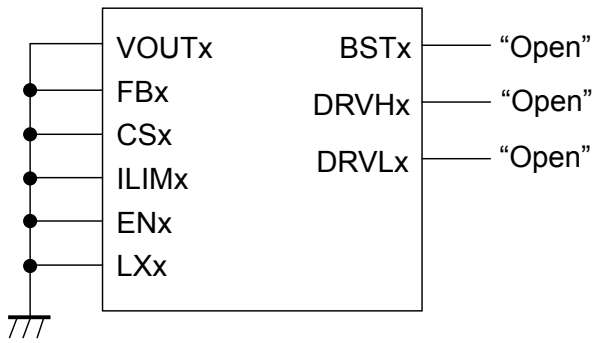
Calculate junction temperature (Tj) by the following formula.

$$Tj = Ta + \theta ja \times P_{IC}$$

Tj : Junction temperature [°C] (+ 125°C Max)
Ta : Ambient temperature [°C]
θja : TSSOP-24P Package thermal resistance (+ 78°C /W)
P_{IC} : IC internal loss [W]

Handling of the pins when using a single channel

Although this device is a 2-channel DC/DC converter control IC, it is also able to be used as a 1-channel DC/DC converter by handling the pins of the unused channel as shown in the following diagram.



Note: x is the unused channel number.

2. Selecting parts

Selection of smoothing inductor

The inductor value selects the value that the ripple current peak-to-peak value of the inductor is 50% or less of the maximum load current as a rough standard. Calculate the inductor value in this case by the following formula.

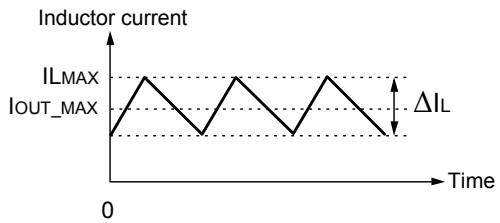
$$L \geq \frac{V_{IN} - V_{OUT}}{LOR \times I_{OUT\_MAX}} \times \frac{V_{OUT}}{V_{IN} \times f_{OSC}}$$

L	: Inductor value [H]
I_{OUT_MAX}	: Maximum load current [A]
LOR	: Ripple current peak-to-peak value of inductor/Maximum load current ratio (= 0.5)
V_{IN}	: Power supply voltage [V]
V_{OUT}	: Output setting voltage [V]
f_{OSC}	: Switching frequency [Hz]

It is necessary to calculate the maximum current value that flows to the inductor to judge whether the electric current that flows to the inductor is a rated value or less. Calculate the maximum current value of the inductor by the following formula.

$$IL_{MAX} \geq I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

IL_{MAX}	: Maximum current value of inductor [A]
I_{OUT_MAX}	: Maximum load current [A]
ΔI_L	: Ripple current peak-to-peak value of inductor [A]
L	: Inductor value [H]
V_{IN}	: Power supply voltage [V]
V_{OUT}	: Output setting voltage [V]
f_{OSC}	: Switching frequency [Hz]



Selection of Switching FET

If selecting the high-side FET so that the value of the high-side FET conduction loss and the high-side FET switching loss is same, the loss is effectively decreased.
Confirm that the high-side FET loss is within the rating value.

$$P_{MainFET} = P_{RON\_Main} + P_{SW\_Main}$$

$P_{MainFET}$: High-side FET loss [W]
P_{RON_Main} : High-side FET conduction loss [W]
P_{SW_Main} : High-side FET switching loss [W]

High-side FET conduction loss

$$P_{RON\_Main} = I_{OUT\_MAX}^2 \times \frac{V_{OUT}}{V_{IN}} \times R_{ON\_Main}$$

P_{RON_Main} : High-side FET conduction loss [W]
I_{OUT_MAX} : Maximum load current [A]
V_{IN} : Power supply voltage [V]
V_{OUT} : Output voltage [V]
R_{ON_Main} : ON resistance of high-side FET [Ω]

The high-side FET switching loss can be calculated roughly by the following formula.

$$P_{SW\_Main} \fallingdotseq 1.56 \times V_{IN} \times f_{OSC} \times I_{OUT\_MAX} \times Q_{SW}$$

P_{SW_Main} : Switching loss [W]
V_{IN} : Power supply voltage [V]
f_{OSC} : Switching frequency [Hz]
I_{OUT_MAX} : Maximum load current [A]
Q_{SW} : Amount of high-side FET gate switch electric charge [C]

MOSFET has a tendency where the gate drive loss increases because the lower drive voltage product has the bigger amount of gate electric charge (Q_G). Normally, we recommend a 4 V drive product, however, the idle period at light load (both the high-side FET and the low-side FET is off-period) gets longer and the gate drive voltage of the high-side FET may decrease, in the automatic PFM/PWM selection mode. The voltage drops most at no-load mode. At this time, confirm that the boost voltage (voltage between BST-LX pins) is a big enough value for the gate threshold value voltage of the high-side FET.
If it is not enough, consider adding the boost diode, increasing the capacitor value of the boost capacitor or using a 2.5 V (or 1.8 V) drive product to the high-side FET.

Select the ON resistance of low-side FET from the range below.

$$R_{ON\_Sync} \leq \frac{0.2}{(I_{LIM} - \frac{\Delta I_L}{2})}, R_{ON\_Sync} \leq \frac{0.1}{\Delta I_L}, R_{ON\_Sync} \geq \frac{0.015}{\Delta I_L}$$

R_{ON_Sync} : ON resistance of low-side FET [Ω]
ΔI_L : Ripple current peak-to-peak value of inductor [A]
I_{LIM} : Over current detection value [A]

If the formula above has been already satisfied and then a low ON resistance FET as possible is used for the low-side FET, the loss is effectively decreased. Especially, it works dramatically in the low on duty mode. The loss of the low-side FET can be calculated by the following formula.

$$P_{SyncFET} = P_{RON\_Sync} = I_{OUT\_MAX}^{2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ON\_Sync}$$

$P_{SyncFET}$: Low-side FET loss [W]
P_{RON_Sync} : Low-side FET conduction loss [W]
I_{OUT_MAX} : Maximum load current [A]
V_{IN} : Power supply voltage [V]
V_{OUT} : Output voltage [V]
R_{ON_Sync} : ON resistance of low-side FET [Ω]

Turn-on and turn-off voltage of the low-side FET is generally small and the switching loss is small enough to ignore, so that is omitted here.
Especially, when turning on the high-side FET under the high power supply voltage condition, the rush-current might be generated by according to self-turn-on of the low-side FET. The parasitic capacitor value of the low-side FET needs to satisfy the following conditions.

$$V_{TH\_Sync} > \frac{C_{rss}}{C_{iss}} \times V_{IN}$$

V_{TH_Sync} : Threshold voltage of low-side FET [V]
C_{rss} : Parasitic feedback capacitance of low-side FET [F]
C_{iss} : Parasitic input capacitance of low-side FET [F]
V_{IN} : Power supply voltage [V]

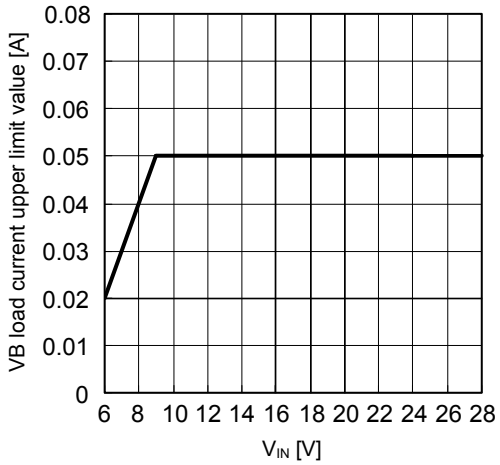
Also approaches of adding a capacitor close between the gate source pins of the low-side FET or adding resistor between the BST pin and the boost capacitor, and so on are effective as a countermeasure of the self-turn-on(adding resistor between the BST pin and the boost capacitor is also effective to adjust turn-on time of the high-side FET).

This device monitors the gate voltage of the switching FET and optimizes the dead time. If the dumping resistor is inserted among DRVH, DRVL and the switching FET gate to adjust turn-on and turn-off time of the switching FET, this function might malfunction. In this device, resistor should not be connected among the DRVH pin, the DRVL pin of IC and the switching FET gate, and should be connected by low impedance as possible.

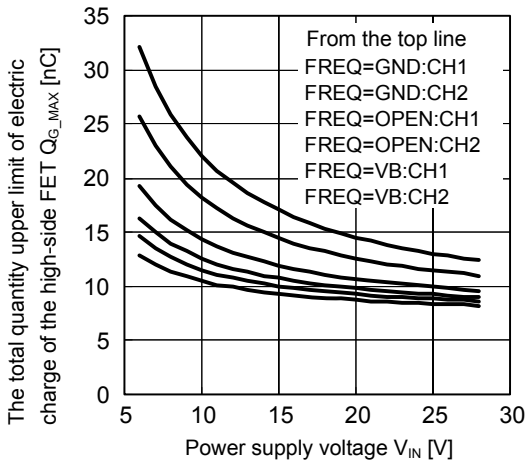
The gate drive power of the switching FET is supplied from LDO (VB) of IC inside. Select switching FET so that the total amount of the switching FET electric charge for 2 channels (QG_Total1, QG_Total2) satisfies the following formula.

$$I_{VB\_MAX} > Q_{G\_Total1} \times f_{OSC1} + Q_{G\_Total2} \times f_{OSC2}$$

I_{VB_MAX} : VB load current upper limit value (see the following graph) [A]
Q_{G_Total1} : Total quantity of charge for the high-side FET and the low-side FET of each CH1 [C]
Q_{G_Total2} : Total quantity of charge for the high-side FET and the low-side FET of each CH2 [C]
f_{OSC1} : CH1Switching frequency [Hz]
f_{OSC2} : CH2 Switching frequency [Hz]



Moreover, select the total quantity of the high-side FET electric charge as a guide that does not exceed the total quantity of the high-side FET electric charge upper limit value shown below.



Whether the mean current value that flows to switching FET is a rated value or less of switching FET is judged. Each rating value for the switching FET can be calculated roughly by the following formula.

$I_{D\_Main} > I_{OUT\_MAX} \times D$
$I_{D\_Sync} > I_{OUT\_MAX} \times (1 - D)$

I_{D_Main} : high-side FET drain current [A]
I_{D_Sync} : Low-side FET drain current [A]
I_{OUT_MAX} : Maximum load current [A]
D : On-duty

$V_{DSS} > V_{IN}$

V_{DSS} : Voltage between the high-side FET drain and source and the low-side FET drain and source [V]
V_{IN} : Power supply voltage [V]

Selection of fly-back diode

This device is improved by adding the fly-back diode when the conversion efficiency improvement or the suppression of the low-side FET fever is desired, although those are unnecessary to execute normally. The effect is achieved in the condition where the switching frequency is high or output voltage is lower. Select schottky barrier diode (SBD) that the forward current is as small as possible. In this DC/DC control IC, the period for the electric current flow into fly-back diode is limited to dead time period because the synchronous rectification system is adopted. (as for the dead time, see “Output Block” in “ELECTRICAL CHARACTERISTICS”). Each rating for the fly-back diode can be calculated by the following formula.

$$I_D \geq I_{OUT\_MAX} \times f_{OSC} \times (t_{D1} + t_{D2})$$

I_D : Forward current rating of SBD [A]
I_{OUT_MAX} : Maximum load current [A]
f_{OSC} : Switching frequency [Hz]
t_{D1}, t_{D2} : Dead time [s]

$$I_{FSM} \geq I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

I_{FSM} : Peak forward surge current ratings of SBD [A]
I_{OUT_MAX} : Maximum load current [A]
ΔI_L : Ripple current peak-to-peak value of inductor [A]

$$V_{R\_Fly} > V_{IN}$$

V_{R_Fly} : Reverse voltage of fly-back diode direct current [V]
V_{IN} : Power supply voltage [V]

Selection of input capacitor

Select the input capacitor whose ESR is as small as possible. The ceramic capacitor is an ideal. Use the tantalum capacitor and the polymer capacitor of the low ESR when a mass capacitor is needed as the ceramic capacitor can not support.
The ripple voltage is generated in the power supply voltage by the switching operation of DC/DC. Calculate the lower bound of input capacitor according to an allowable ripple voltage. Calculate the ripple voltage of the power supply from the following formula.

$$\Delta V_{IN} = \frac{I_{OUT\_MAX}}{C_{IN}} \times \frac{V_{OUT}}{V_{IN} \times f_{OSC}} + ESR \times \left(I_{OUT\_MAX} + \frac{\Delta I_L}{2}\right)$$

ΔV_{IN} : Power supply ripple voltage peak-to-peak value [V]
I_{OUT_MAX} : Maximum load current value [A]
C_{IN} : Input capacitor value [F]
V_{IN} : Power supply voltage [V]
V_{OUT} : Output setting voltage [V]
f_{OSC} : Switching frequency [Hz]
ESR : Series resistance component of input capacitor [Ω]
ΔI_L : Ripple current peak-to-peak value of inductor [A]

Capacitor has frequency characteristic, the temperature characteristic, and the bias voltage characteristic, etc. The effective capacitor value might become extremely small depending on the use conditions. Note the effective capacitor value in the use conditions.

Calculate ratings of the input capacitor by the following formula:

$$V_{CIN} > V_{IN}$$

V_{CIN} : Withstand voltage of the input capacitor [V]
V_{IN} : Power supply voltage [V]

$$Irms \geq I_{OMAX} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

Irms : Allowable ripple current of input capacitor (effective value) [A]
I_{OMAX} : Maximum load current value [A]
V_{IN} : Power supply voltage [V]
V_{OUT} : Output setting voltage [V]

Selection of output capacitor

A certain level of ESR is required for stable operation of this IC. Use a tantalum capacitor or polymer capacitor as the output capacitor. If using a ceramic capacitor with low ESR, a resistor should be connected in series with it to increase ESR equivalently.
Calculate the output capacitor value by the following formula as a guide.

$$C_{OUT} \geq \frac{1}{4 \times f_{OSC} \times ESR}$$

C_{OUT} : Output capacitor value [F]
f_{OSC} : Switching frequency [Hz]
ESR : Series resistance of output capacitor [Ω]

Moreover, the output capacitor values are also derived from the allowable amount of overshoot and undershoot. The following formula is represented as the worst condition in which the shift time for a sudden load change is 0s. The output capacitor value allow a smaller amount than the value calculated by the following formula when a longer shift time.

$$C_{OUT} \geq \frac{\Delta I_{OUT}^2 \times L}{2 \times V_{OUT} \times \Delta V_{OUT\_OVER}} \ldots \text{Overshoot condition}$$

$$C_{OUT} \geq \frac{\Delta I_{OUT}^2 \times L \times (V_{OUT} + V_{IN} \times f_{OSC} \times t_{OFF\_MIN})}{2 \times V_{OUT} \times \Delta V_{OUT\_UNDER} \times (V_{IN} - V_{OUT} - V_{IN} \times f_{OSC} \times t_{OFF\_MIN})} \ldots \text{Undershoot condition}$$

C_{OUT} : Output capacitor value [F]
ΔV_{OUT_OVER} : Allowable amount of output voltage overshoot [V]
ΔV_{OUT_UNDER} : Allowable amount of output voltage undershoot [V]
ΔI_{OUT} : Current difference in sudden load change [A]
L : Inductor value [H]
V_{IN} : Power supply voltage [V]
V_{OUT} : Output setting voltage [V]
f_{OSC} : Switching frequency [Hz]
t_{OFF_MIN} : Minimum off time

When changing to no load suddenly, the output voltage is overshoot, however, the current sink is not executed in the mode other than PWM fix. As a result, the decrement of the output voltage might take a long time. This sometimes results in the stop mode because of the over voltage detection. In the mode other than PWM fix, select the capacitor value so that the overshoot value is set to the over voltage detection voltage value or less (115% of the output setting voltage or less).
The capacitor has frequency, operating temperature, and bias voltage characteristics, etc. Therefore, it must be noted that its effective capacitor value may be significantly smaller, depending on the use conditions.

Calculate each rating of the output capacitor by the following formula:

$V_{COUT} > V_{OUT}$

V_{COUT} : Withstand voltage of the output capacitor [V]
V_{OUT} : Output voltage [V]

$$I_{RMS} \geq \frac{\Delta I_L}{2\sqrt{3}}$$

I_{RMS} : Allowable ripple current of output capacitor (effective value) [A]
ΔI_L : Ripple current peak-to-peak value of inductor [A]

When connecting resistance in series configuration while a ceramic capacitor is in use, the resistor rating is calculated by the following formula.

$$P_{ESR} > \frac{ESR \times \Delta I_L{}^2}{12}$$

P_{ESR} : Power dissipation of resistor [W]
ESR : Resistor value [Ω]
ΔI_L : Ripple current peak-to-peak value of inductor [A]

Selection of bootstrap capacitor

To drive the gate of high-side FET, the bootstrap capacitor must have enough stored charge. 0.1 µF is assumed to be standard, however, it is necessary to adjust it when the high-side FET Q_G is big. Consider the capacitor value calculated by the following formula as the lowest value for the bootstrap capacitor and select a thing any more.

$$C_{BST} \geq 10 \times Q_G$$

C_{BST} : Bootstrap capacitor value [F]
Q_G : Total quantity of charge for the high-side FET gate [C]

Calculate ratings of the bootstrap capacitor by the following formula:

$$V_{CBST} > V_B$$

V_{CBST} : Withstand voltage of the bootstrap capacitor [V]
V_B : VB voltage [V]

VB pin capacitor

4.7 µF is assumed to be a standard, and when Q_G of switching FET used is large, it is necessary to adjust it. To suppress the ripple voltage by the switching FET gate drive, consider the capacitor value calculated by the following formula as the lowest value for VB capacitor and select a thing any more.

$$C_{VB} \geq 50 \times Q_G$$

C_{VB} : VB pin capacitor value [F]
Q_G : Total amount of gate charge of high-side FET and low-side switching FET for 2CH [C]

Calculate ratings of the VB pin capacitor by the following formula:

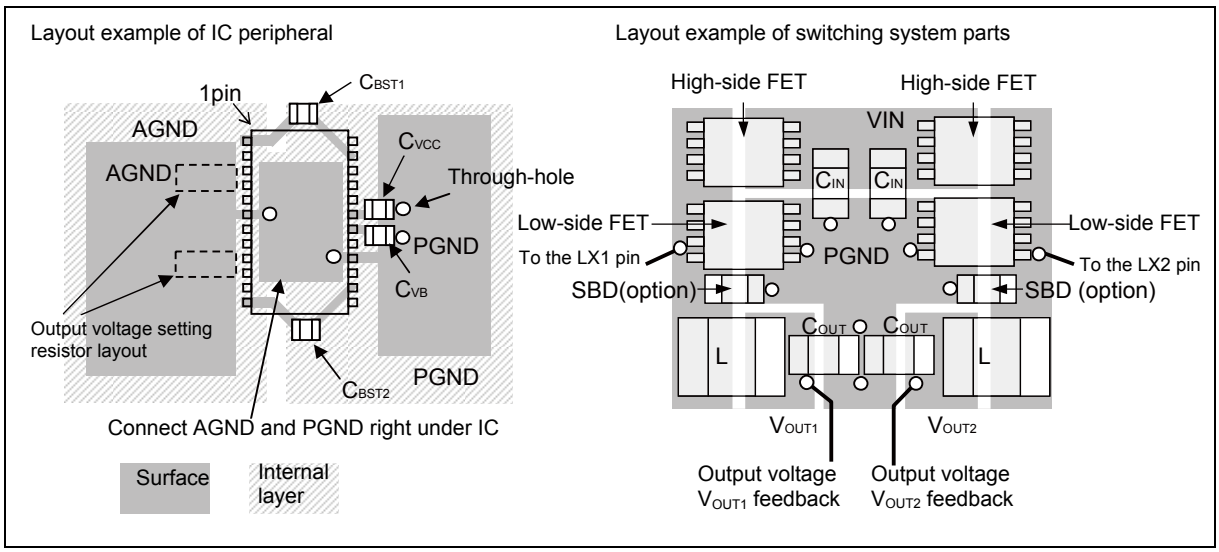
$$V_{CVB} > V_B$$

V_{CVB} : Withstand voltage of the VB pin capacitor [V]
V_B : VB voltage [V]

Layout

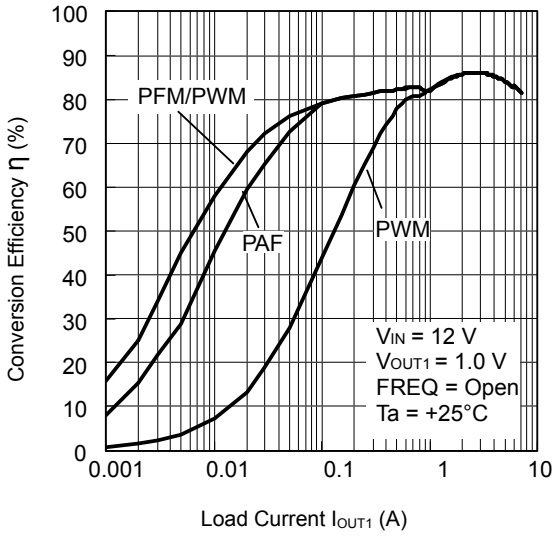
Consider the points listed below and do the layout design.

- Provide the ground plane as much as possible on the IC mounted face. Connect bypass capacitor connected with the VCC and VB pins, and GND pin of the switching system parts with switching system GND (PGND). Connect other GND connection pins with control system GND (AGND), and separate each GND, and try not to pass the heavy current path through the control system GND (AGND) as much as possible. In that case, connect control system GND (AGND) and switching system GND (PGND) at the single point of GND (PGND) directly below IC. Switching system parts are Input capacitor (C_{IN}), Switching FET, fly-back diode (SBD), inductor (L) and Output capacitor (C_{OUT}).
- Connect the switching system parts as much as possible on the surface. Avoid the connection through the through-hole as much as possible.
- As for GND pins of the switching system parts, provide the through hole at the proximal place, and connect it with GND of internal layer.
- Pay the most attention to the loop composed of input capacitor (C_{IN}), switching FET, and fly-back diode (SBD). Consider parts are disposed mutually to be near for making the current loop as small as possible.
- Place the bootstrap capacitor (C_{BST1}, C_{BST2}) proximal to BSTx and LXx pins of IC as much as possible.
- Connect the line to the LX pin proximal to the drain pin of low-side FET. Also large electric current flows momentary in this net. Wire the line of width of about 0.8 mm as standard, and as short as possible.
- Large electric current flows momentary in the net of DRVHx and DRVLx pins connected with the gate of switching FET. Wire the linewidth of about 0.8 mm to be a standard, as short as possible. Take special care about the line of the DRVLx pin, and wire the line as short as possible.
- By-pass capacitor (C_{VCC}, C_{VB}) connected with VCC, and VB should be placed close to the pin as much as possible. Also connect the GND pin of the bypass capacitor with GND of internal layer in the proximal through-hole.
- Pull the feedback line to be connected to the VOUTx pin of the IC separately from near the output capacitor pin, whenever possible. Consider the line connected with VOUTx and FBx pins to keep away from a switching system parts as much as possible because it is sensitive to the noise.
  Also, place the output voltage setting resistor connected to this line near IC, and try to shorten the line to the FBx pin. In addition, for the internal layer right under the component mounting place, provide the control system GND (AGND) of few ripple and few spike noises, or provide the ground plane of the power supply as much as possible.
  Consider that the discharge current momentary flows into the VOUTx pin (about 200 mA at Vout = 5 V) when the DC/DC operation stops, and then sustain the width for the feedback line.
  There is leaked magnetic flux around the inductor or backside of place equipped with inductor. Line and parts sensitive to noise should be considered to be placed away from the inductor (or backside of place equipped with inductor).

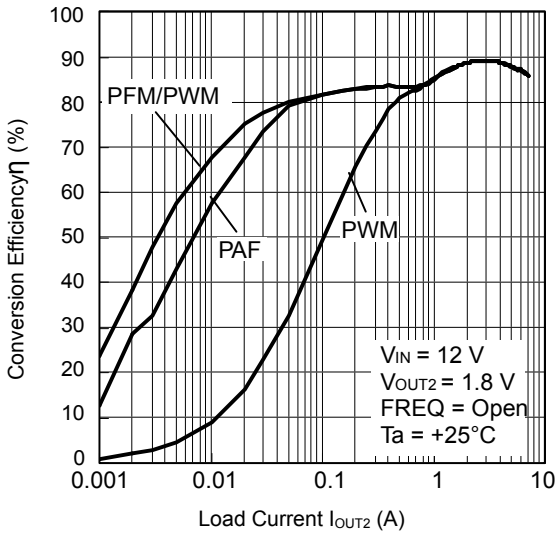


■ REFERENCE DATA

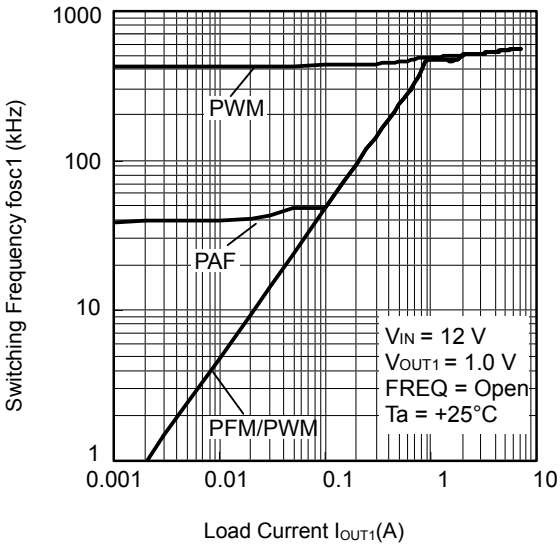
Conversion Efficiency vs.Load Current



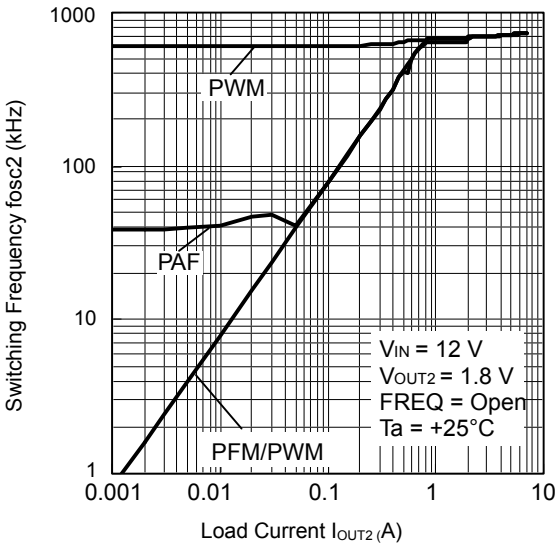
Conversion Efficiency vs.Load Current



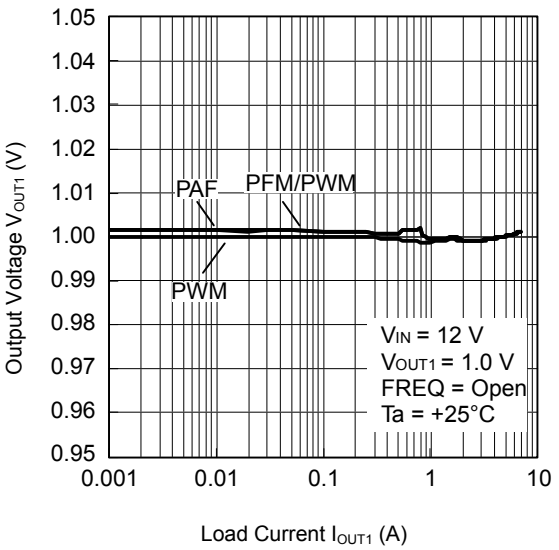
Switching Frequency vs. Load Current



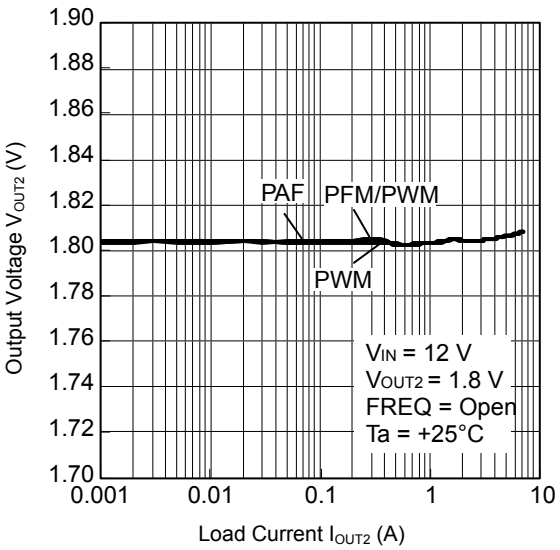
Switching Frequency vs. Load Current



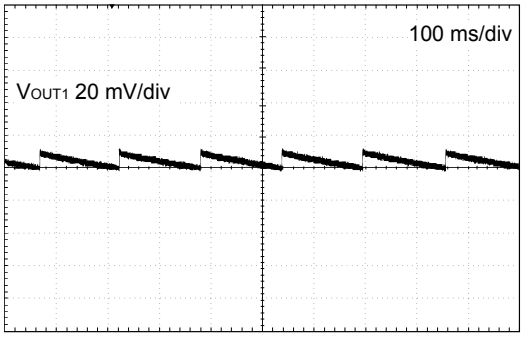
Output Voltage vs. Load Current



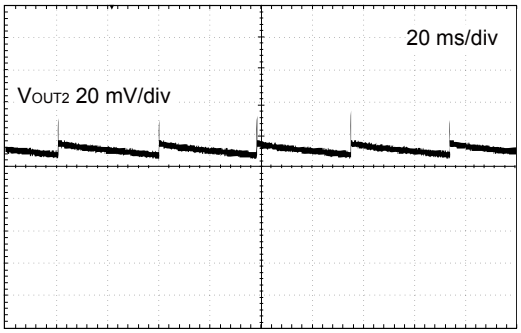
Output Voltage vs. Load Current



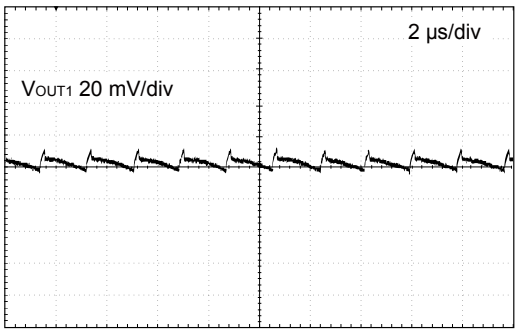
Ripple Waveform



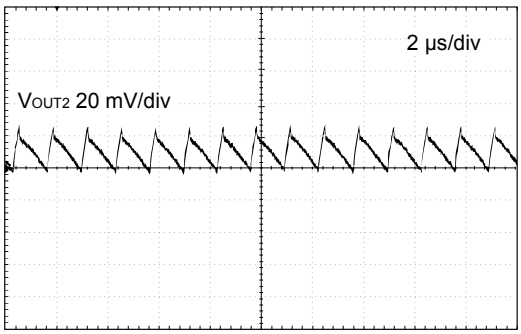
V_{IN}=12 V, V_{OUT1}=1.0 V, I_{OUT1}=0 A, MODE=GND,
FREQ=Open, Ta=+25°C



V_{IN}=12 V, V_{OUT2}=1.8 V, I_{OUT2}=0 A, MODE=GND,
FREQ=Open, Ta=+25°C

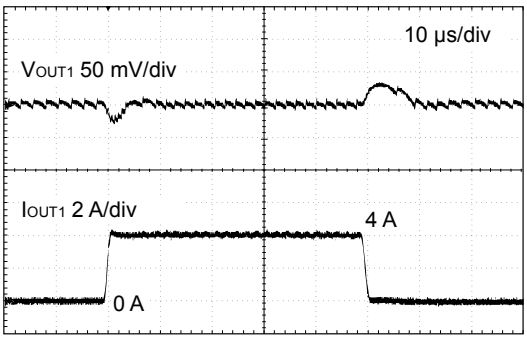


V_{IN}=12 V, V_{OUT1}=1.0 V, I_{OUT1}=7 A, MODE=GND,
FREQ=Open, Ta=+25°C

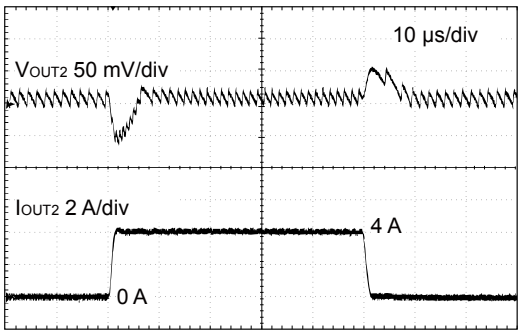


V_{IN}=12 V, V_{OUT2}=1.8 V, I_{OUT2}=7 A, MODE=GND,
FREQ=Open, Ta=+25°C

Load Sudden Change Waveform

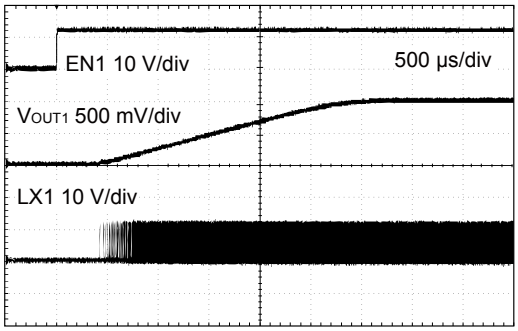


V_{IN}=12 V, V_{OUT1}=1.0 V, I_{OUT1}=0 A ⇔4 A, MODE=GND,
FREQ=Open, Ta=+25°C

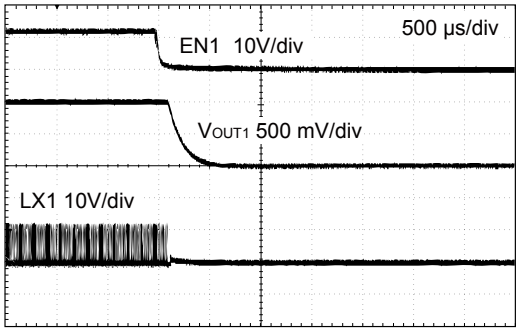


V_{IN}=12 V, V_{OUT2}=1.8 V, I_{OUT2}=0 A ⇔4 A, MODE=GND,
FREQ=Open, Ta=+25°C

EN Startup and Shutdown Waveform

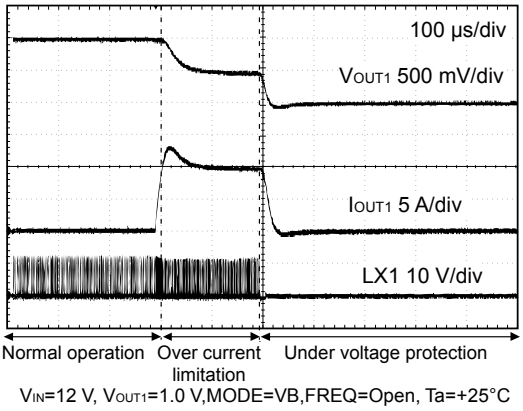


V_{IN}=12 V, V_{OUT1}=1.0 V, I_{OUT1}=7 A (0.14 Ω), MODE=GND, FREQ=Open, Ta=+25°C



V_{IN}=12V, V_{OUT2}=1.8 V, I_{OUT2}=7 A (0.26 Ω), MODE=GND, FREQ=Open, Ta=+25°C

Output Over Current Waveform



V_{IN}=12 V, V_{OUT1}=1.0 V,MODE=VB,FREQ=Open, Ta=+25°C

■ USAGE PRECAUTION

1. Do not configure the IC over the maximum ratings.

If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions can have an adverse effect on the reliability of the LSI.

2. Use the device within the recommended operating conditions.

The recommended values guarantee the normal LSI operation under the recommended operating conditions. The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

3. Printed circuit board ground lines should be set up with consideration for common impedance.

4. Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

5. Do not apply negative voltages.

The use of negative voltages below −0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB39A214APFT	24-pin plastic TSSOP (FPT-24P-M09)	

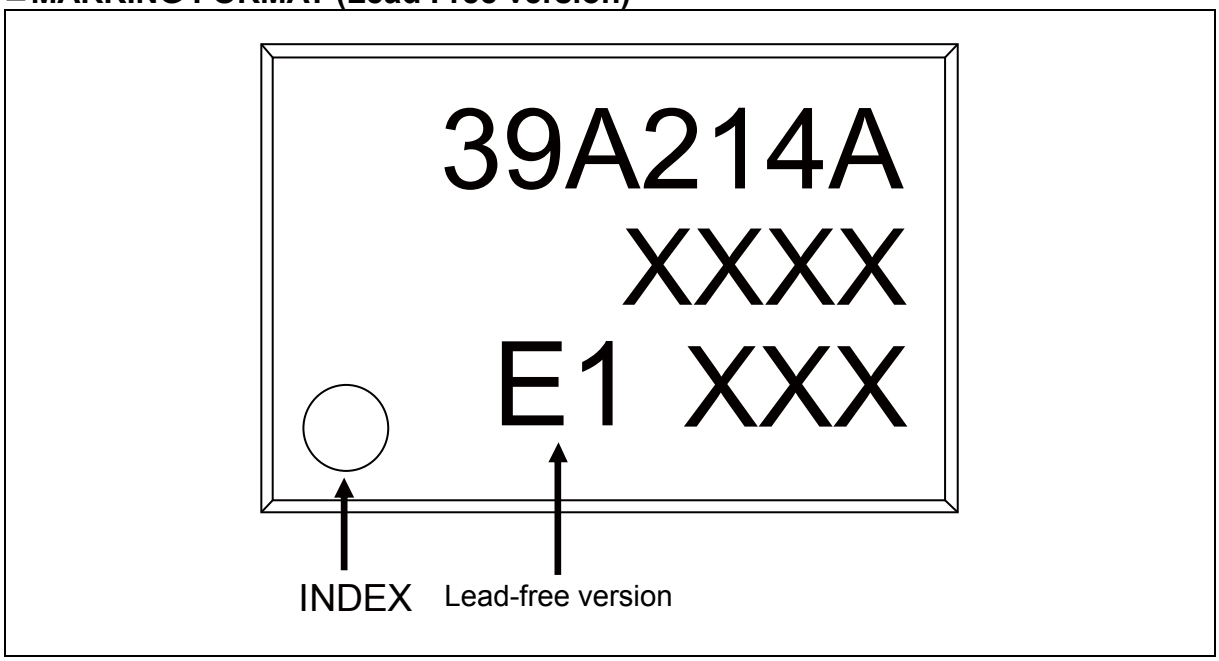
■ EV BOARD ORDERING INFORMATION

EV board number	EV board version No.	Remarks
MB39A214A-EVB-01	MB39A214A-EVB-01 Rev. 1.0	TSSOP-24

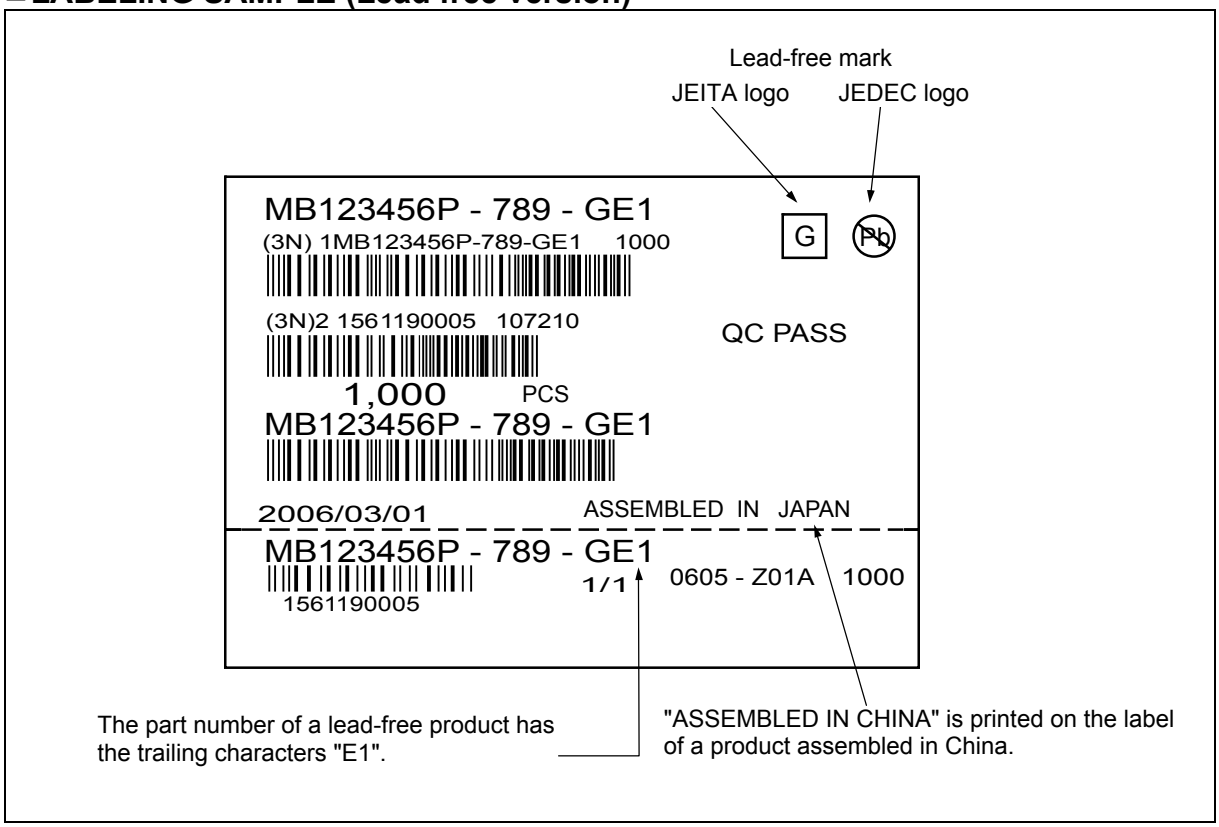
■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

The LSI products of FUJITSU SEMICONDUCTOR with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE). A product whose part number has trailing characters “E1” is RoHS compliant.

■ MARKING FORMAT (Lead Free version)



■ LABELING SAMPLE (Lead free version)



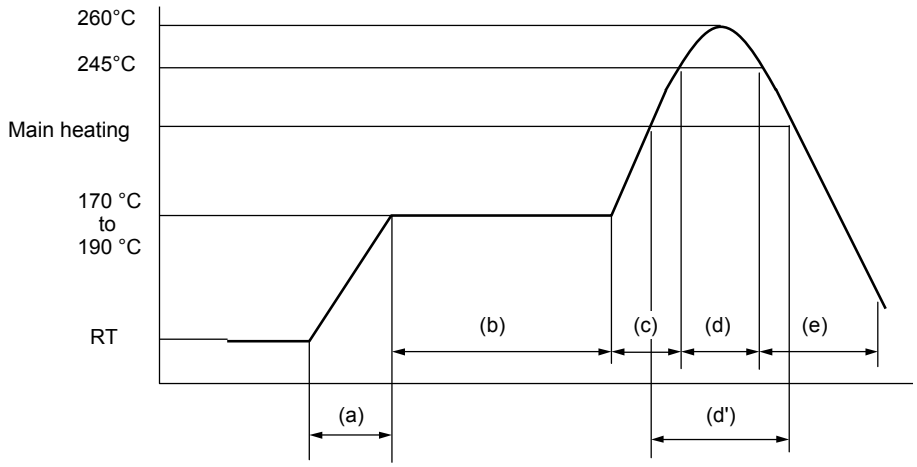
■ MB39A214APFT RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL

[FUJITSU SEMICONDUCTOR Recommended Mounting Conditions]

Item	Condition	
Mounting Method	IR (infrared reflow), warm air reflow	
Mounting times	2 times	
Storage period	Before opening	Please use it within two years after manufacture.
	From opening to the 2nd reflow	Less than 8 days
	When the storage period after opening was exceeded	Please process within 8 days after baking (125°C ±3°C, 24H+ 2H/−0H) . Baking can be performed up to two times.
Storage conditions	5°C to 30°C, 70% RH or less (the lowest possible humidity)	

[Mounting Conditions]

(1) IR (infrared reflow)



"M" rank : 250°C Max

(a) Temperature Increase gradient	: Average 1°C/s to 4°C /s
(b) Preliminary heating	: Temperature 170°C to 190°C, 60 s to 180 s
(c) Temperature Increase gradient	: Average 1°C /s to 4°C /s
(d) Peak temperature	: Temperature 250°C Max; 245°C or more, 10 s or less
(d') Main Heating	: Temperature 230°C or more, 40 s or less or Temperature 225°C or more, 60 s or less or Temperature 220°C or more, 80 s or less
(e) Cooling	: Natural cooling or forced cooling

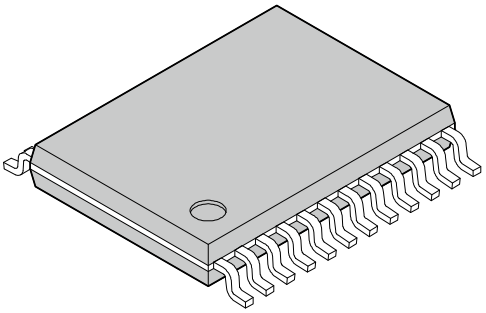
Note: Temperature : the top of the package bod

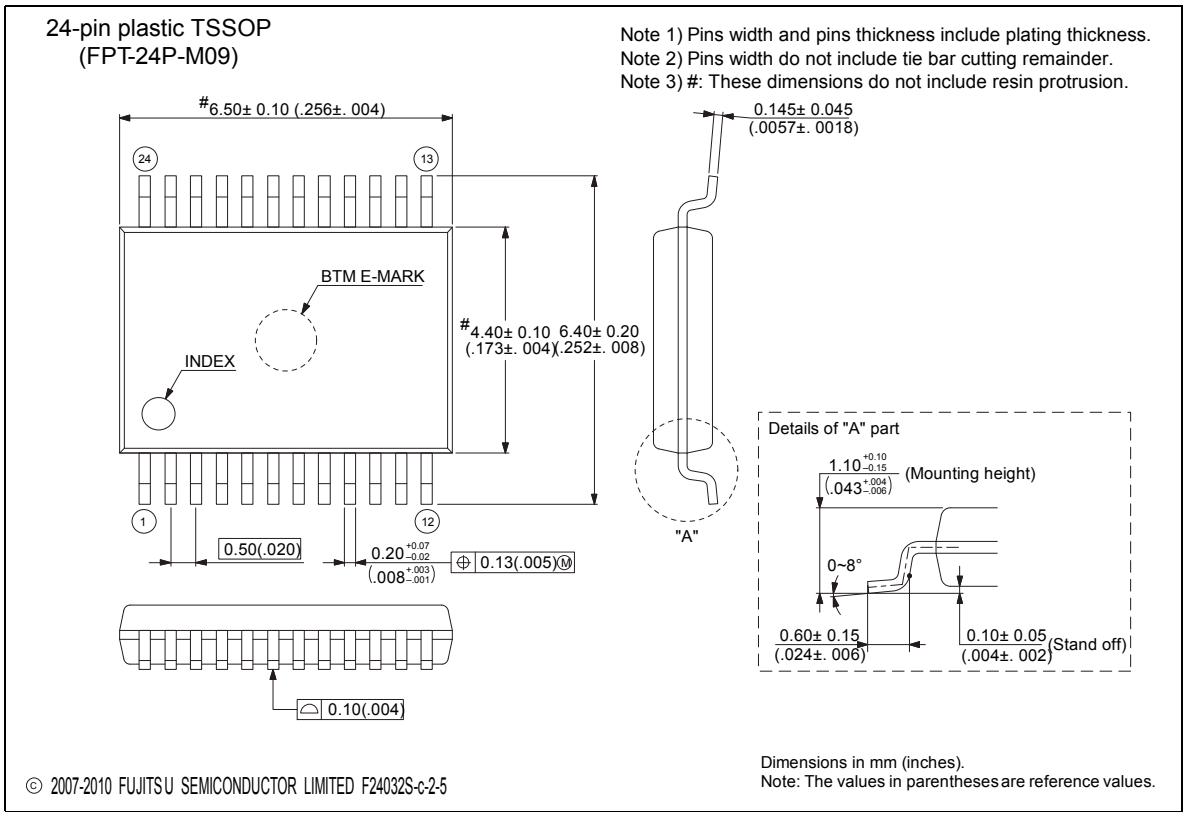
(2) Manual soldering (partial heating method)

Item	Condition	
Storage period	Before opening	Within two years after manufacture
	Between opening and mounting	Within two years after manufacture (No need to control moisture during the storage period because of the partial heating method.)
Storage conditions	5°C to 30°C, 70% RH or less (the lowest possible humidity)	
Mounting conditions	Temperature at the tip of a soldering iron: 400°C Max Time: Five seconds or below per pin*	

*: Make sure that the tip of a soldering iron does not come in contact with the package body.

■ PACKAGE DIMENSIONS

24-pin plastic TSSOP		
	Lead pitch	0.50 mm
	Package width × package length	4.40 mm × 6.50 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.08 g
(FPT-24P-M09)		



Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ CONTENTS

page

MEMO

MEMO

MEMO

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