AK4558

108dB 216kHz 32Bit ΔΣ CODEC with PLL

1. General Description

The AK4558 is a low voltage 32bit 216kHz CODEC for high performance battery powered digital audio subsystems. An internal circuit includes newly developed 32-bit Digital Filter achieving short group delay and high quality sound. In addition, “OSR-Doubler” technology is newly adopted, making the AK4558 capable of supporting wide range signals and achieving low out-of-band noise while realizing low power consumption. The AK4558 is ideal for a wide range of applications that demands high sound quality including Electronic musical instruments and Audio Interfaces. The analog inputs and outputs are single-ended to minimize pin count and external filtering requirements. The AK4558 is housed in a very small 28-pin QFN. It is ideal for space-sensitive applications.

2. Features

- **Single-ended ADC**
  - **Dynamic Range, S/N: 108dB@AVDD=3.3V**
  - **S/(N+D): 92dB@AVDD=3.3V**
  - **Selectable HPF for DC-offset cancel (fc = 1Hz @ fs=48kHz)**
  - **4-types Digital Filter for High Sound Quality**
- **Single-ended DAC**
  - **Dynamic Range, S/N: 108dB@AVDD=3.3V**
  - **S/(N+D): 100dB@AVDD=3.3V**
  - **Digital de-emphasis for 32kHz, 44.1kHz and 48kHz sampling**
  - **5-types Digital Filter for High Sound Quality**
  - **Channel Independent Digital Attenuator (256 levels, 0.5dB steps)**
- **Audio I/F format: MSB First, 2’s Complement**
  - **ADC: 24/32bit MSB justified , 24/32bit I^2S compatible or TDM**
  - **DAC: 24/32bit MSB justified, 16/20/24/32bit LSB justified, 24/32bit I^2S compatible or TDM**
- **Input/Output Voltage: ADC = 2.64Vpp @ AVDD=3.3V**
  DAC = 2.51Vpp @ AVDD=3.3V
- **Master/Slave mode**
- **μP I/F: I^2C Bus**
- **Sampling Rate:**

(1) PLL Mode

- **PLL Slave Mode (LRCK pin): fs = 8kHz ~ 216kHz**
- **PLL Slave Mode (BICK pin): fs = 8kHz ~ 216kHz**
- **PLL Master Mode: 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 54kHz, 88.2kHz, 96kHz, 128kHz, 176.4kHz, 192kHz**

(2) External Clock Mode

- **Normal Speed: 8kHz to 54kHz (256fs or 512fs)**
  8kHz to 48kHz (384fs or 768fs)
- **Double Speed: 54kHz to 108kHz (256fs)**
  48kHz to 96kHz (384fs)
- **Quad Speed: 108kHz to 216kHz (128fs)**
  96kHz to 192kHz (192fs)

- ☐ **Master Clock:**
  - **(1) PLL Mode**
    - **MCKI pin: 27MHz, 26MHz, 24MHz, 19.2MHz, 13.5MHz, 13MHz, 12.288MHz, 12MHz, 11.2896MHz**
    - **LRCK pin: 1fs**
    - **BICK pin: 32fs, 64fs, 128fs(TDM), 256fs(TDM)**
  - **(2) External Clock Mode (MCKI pin)**
    - **Slave mode: 256fs, 384fs, 512fs or 768fs (Normal Speed)**
      256fs or 384fs (Double Speed)
      128fs or 192fs (Quad Speed)
    - **Master mode: 256fs or 512fs (Normal Speed)**
      256fs (Double Speed)
      128fs (Quad Speed)
- ☐ **Power Supply:**
  - **AVDD = 2.4 to 3.6V (typ. 3.3V)**
  - **TVDD = 1.7 to 3.6V (typ. 1.8V)**
- ☐ **Power Supply Current: 18mA(fs=48kHz)**
- ☐ **Ta = -40 to 105°C**
- ☐ **Package: 28-pin QFN (0.5mm pitch)**

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4. Block Diagram and Functions

■ Block Diagram

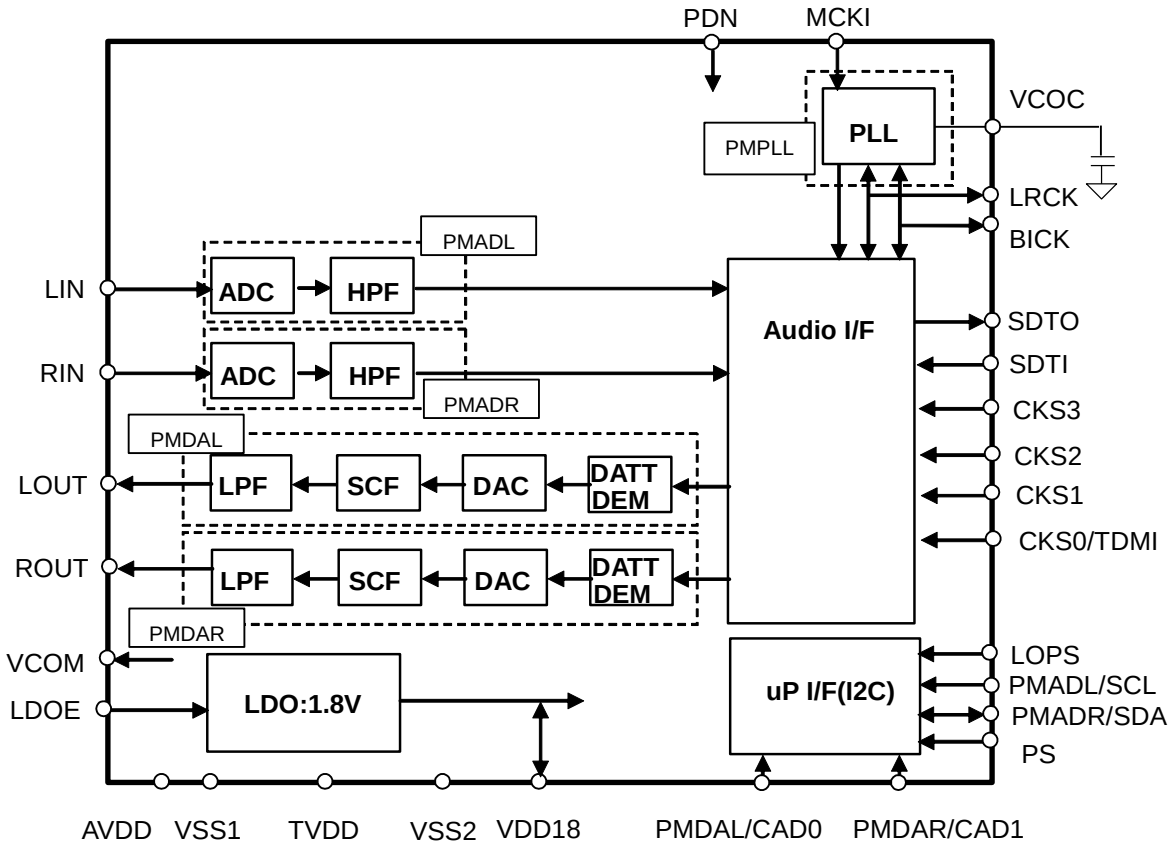


Figure 1. Block Diagram

■ Compatibility with the AK4556

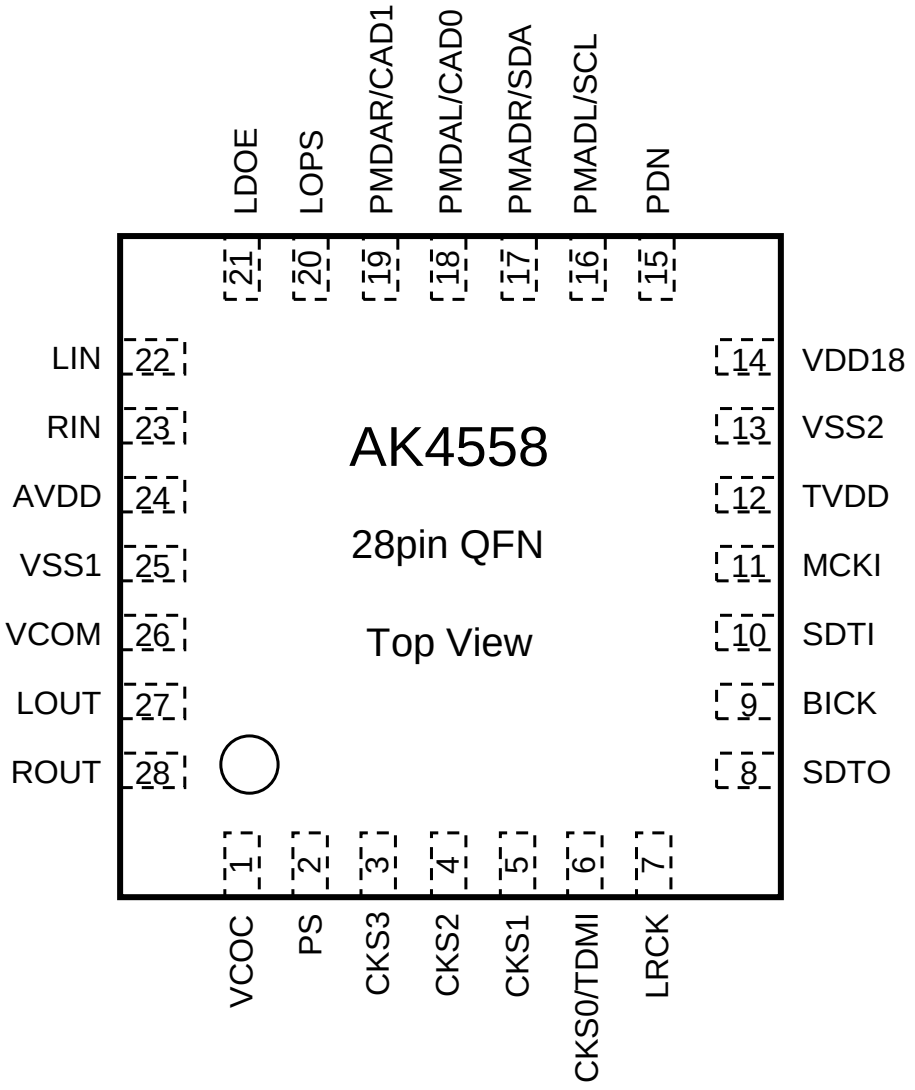
Function		AK4556	AK4558
fs (max)		216kHz	216kHz
HFP Cut-off		1Hz @ fs = 48kHz	1Hz @ fs = 48kHz
HPF Disable		Yes	Yes
ADC			
Input Level		0.7 x VA	0.8 x AVDD
Input Resistance		8kΩ@ fs = 48kHz, 96kHz, 192kHz	8kΩ@ fs = 48kHz, 96kHz, 192kHz
Init Cycle		4134/fs @ Normal Speed, Slave mode	5200/fs @ Normal Speed, Slave mode
S/(N+D)		91dB	92dB
DR, S/N		103dB	108dB
DF	SA	68dB	85dB
	SB	28kHz	27.8kHz
	GD	18/fs	5/fs
DAC			
Output Level		0.7 x VA	0.76 x AVDD
Load Resistance		5kΩ	5kΩ
S/(N+D)		90dB	100dB
DR, S/N		106dB	108dB
DF	SA	54dB	80dB
	GD	21/fs	6.8/fs
MCKI (Slave)		256/384/512/768fs @ Normal Speed	256/384/512/768fs @ Normal Speed
		256/384fs @ Double Speed	256/384fs @ Double Speed
		128/192fs @ Quad Speed	128/192fs @ Quad Speed
Audio I/F	ADC	24bit MSB justified / I^2S	24/32bit MSB justified 24/32bit I^2S/TDM
	DAC	24bit MSB justified /24bit LSB justified / I^2S	24/32bit MSB justified 16/20/24/32bit LSB justified 24/32bit I^2S/TDM
Volume		No	0.5dB/step
Digital Filter Option		No	Yes
PLL		No	Yes
M/S mode		Master / Slave	Master / Slave
Parallel/Serial mode		No	Yes
Pop Guard		No	Yes
Idd		27.5mA (Vdd = 3V)	18.0mA (AVDD = 3.3V,TVDD=1.8V)
AVDD		2.4V to 3.6V	2.4V to 3.6V
VDD18		2.4V to 3.6V (Normal/Double Speed) 2.7V to 3.6V (Quad Speed)	1.7V to 1.98V
TVDD		-	1.7V to 3.6V
Package		20TSSOP (6.5mm x 6.4mm, 0.65mm Pitch)	28QFN (5.0mm x 5.0mm, 0.5mm Pitch)

5. Pin Configurations and Functions

■ Ordering Guide

AK4558EN	-40 ~ +105°C	28-pin QFN (0.5mm pitch)
AKD4558	Evaluation Board for the AK4558	

■ Pin Layout



Note 1. The exposed pad on the bottom surface of the package must be connected to VSS.

■ Pin Functions

No.	Pin Name	I/O	PD State	Function
1	VCOC	O	Hi-z	(PS pin = "H") This pin should be connected to VSS. (PS pin = "L") Output Pin for Loop Filter of PLL Circuit This pin should be connected to VSS, unless PLL Mode 15 used.
2	PS	I	Hi-z	Parallel/Serial Mode Select Pin "L": Serial Mode, "H": Parallel Mode Do not change this pin during PDN pin = "H".
3	CKS3	I	Hi-z	Mode Setting Pin #3
4	CKS2	I	Hi-z	Mode Setting Pin #2
5	CKS1	I	Hi-z	Mode Setting Pin #1
6	CKS0	I	Hi-z	(PS pin = "H") Mode Setting Pin #0
	TDMI	I	Hi-z	(PS pin = "L") TDM Data Input Pin
7	LRCK	I/O	Hi-Z /L	Input/Output Channel Clock Pin When PDN pin is "L", LRCK pin outputs "L" in master mode. LRCK pin outputs "Hi-Z" in slave mode.
8	SDTO	O	L	Audio Serial Data Output Pin When PDN pin is "L", SDTO pin outputs "L".
9	BICK	I/O	Hi-Z /L	Audio Serial Data Clock Pin When PDN pin is "L", BICK pin outputs "L" in master mode. BICK pin outputs "Hi-Z" in slave mode.
10	SDTI	I	Hi-z	Audio Serial Data Input Pin
11	MCKI	I	Hi-z	External Master Clock Input Pin
12	TVDD	-	-	LDO Power Supply/Digital I/F Power Supply Pin
13	VSS2	-	-	Digital Ground Pin
14	VDD18	O	Pulldown (500ohm)	(LDOE pin = "H") LDO Output Pin This pin must be connected to VSS2 pin with 1μF ± 50% capacitor in series.
		I	Hi-z	(LDOE pin = "L") 1.8V Power Input Pin
15	PDN	I	Hi-z	Power-Down & Reset Mode Pin "L": Power-down and Reset, "H": Normal operation The AK4558 should be reset once by bringing PDN pin = "L".
16	PMADL	I	Hi-z	(PS pin = "H") ADC Lch Power Management Pin
	SCL	I	Hi-z	(PS pin = "L") Control Data Clock Pin
17	PMADR	I	Hi-z	(PS pin = "H") ADC Rch Power Management Pin
	SDA	I/O	Hi-z	(PS pin = "L") Control Data Input/Output Pin
18	PMDAL	I	Hi-z	(PS pin = "H") DAC Lch Power Management Pin
	CAD0	I	Hi-z	(PS pin = "L") Chip Address 0 Pin
19	PMDAR	I	Hi-z	(PS pin = "H") DAC Rch Power Management Pin
	CAD1	I	Hi-z	(PS pin = "L") Chip Address 1 Pin
20	LOPS	I	Hi-z	(PS pin = "H") DAC Output Power Save Mode Control Pin (PS pin = "L") This pin must be connected to VSS2.
21	LDOE	I	Hi-z	LDO Enable Pin "L": LDO Disable, "H": LDO Enable
22	LIN	I	Hi-z	Lch Analog Input Pin
23	RIN	I	Hi-z	Rch Analog Input Pin
24	AVDD	-	-	Analog Power Supply Pin

25	VSS1	-	-	Analog Ground Pin
26	VCOM	O	Pulldown (400ohm)	Common Voltage Output Pin, 0.5 x AVDD This pin must be connected to VSS1 pin with 1μF±50% capacitor in series.
27	LOUT	O	Pulldown (100kohm)	Lch Analog Output Pin
28	ROUT	O	Pulldown (100kohm)	Rch Analog Output Pin

Note 2. All input pins except analog input pins (LIN and RIN) must not be allowed to float.

■ Handling of Unused Pins

Unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	LOUT, ROUT, LIN, RIN	Open
Digital	MCKI, SDTI, CKS0/TDMI, CKS1, LOPS	Connect to VSS2
	SDTO	Open

6. Absolute Maximum Ratings

(VSS1=VSS2=0V; Note 3)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog	AVDD	-0.3	6.0	V
	Digital core	VDD18	-0.3	2.5	V
	Digital I/O	TVDD	-0.3	6.0	V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
Analog Input Voltage (LIN, RIN pin)		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage (Note 4)		VIND	-0.3	TVDD+0.3	V
Ambient Temperature (power applied) (Note 5)		Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 3. All voltages with respect to ground. VSS1 and VSS2 must be connected to analog ground.

Note 4. PMDAL/CAD0, PMDAR/CAD1, LOPS, CKS0/TDMI, CKS3, CKS2, CKS1, PMADL/SCL, PMADR/SDA, SDTI, LRCK, BICK, MCKI, SDA, PS, LDOE and PDN pins. The external pull-up resistors at the SDA and SCL pins should be connected to (TVDD+0.3) voltage or less.

Note 5. In case that PCB drawing density is more than 100%. The exposed pad on the bottom surface of the package must be connected to VSS.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1=VSS2=0V; Note 3)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 6)	Analog	AVDD	2.4	3.3	3.6	V
	Digital (LDOE pin="L")	TVDD	VDD18	1.8	3.6	V
	Digital Core(LDOE pin="L")	VDD18	1.7	1.8	1.98	V
	Digital (LDOE pin="H")	TVDD	2.4	3.3	3.6	

Note 3. All voltages with respect to ground. VSS1 and VSS2 must be connected to analog ground.

Note 6. When the LDOE pin = "L" VDD18 must be powered up either at the same time or after TVDD is powered up. Internal LDO generates 1.8V, when the LDOE pin ="H". The power-up sequence with AVDD and TVDD is not critical. The PDN pin should be held "L" prior to when power is applied. The PDN pin is allowed to be "H" after all power supplies are applied and settled. All power pins of the AK4558 must be supplied. Do not turn any power supply off independently (neither grounded nor floating). When using the AK4558 with I²C bus, the power supply of the AK4558 must not be turned off unless the power supplies of the surrounding device are turned off.

*AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Analog Characteristics

(Ta=25°C; AVDD= TVDD=3.3V; VSS1=VSS2=0V; EXT Slave Mode; fs=48kHz, 96kHz, 192kHz; Signal Frequency=1kHz; BICK=64fs; Data=32bit, Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 20Hz ~ 40kHz at fs=96kHz, 20Hz ~ 40kHz at fs=192kHz; unless otherwise specified)

Parameter			Min.	Typ.	Max.	Unit
ADC Analog Input Characteristics:						
Resolution			-	-	32	bit
Input Voltage		(Note 7)	2.38	2.64	2.90	Vpp
S/(N+D)	fs=48kHz	–1dBFS	82	92	-	dB
	BW=20kHz	–60dBFS	-	43	-	dB
	fs=96kHz	–1dBFS	81	91	-	dB
	BW=40kHz	–60dBFS	-	40	-	dB
	fs=192kHz	–1dBFS	-	91	-	dB
	BW=40kHz	–60dBFS	-	40	-	dB
DR	(–60dBFS with A-weighted)		100	108	-	dB
S/N	(A-weighted)		100	108	-	dB
Input Resistance			7	10	-	kΩ
Interchannel Isolation			90	110	-	dB
Interchannel Gain Mismatch			-	0	0.5	dB
Gain Drift			-	100	-	ppm/°C
Power Supply Rejection		(Note 11)	-	50	-	dB
DAC Analog Output Characteristics:						
Resolution			-	-	32	bit
Output Voltage		(Note 8)	2.26	2.51	2.76	Vpp
S/(N+D)	fs=48kHz	0dBFS	90	100	-	dB
	BW=20kHz	–60dBFS	-	45	-	dB
	fs=96kHz	0dBFS	88	98	-	dB
	BW=40kHz	–60dBFS	-	42	-	dB
	fs=192kHz	0dBFS	-	98	-	dB
	BW=40kHz	–60dBFS	-	42	-	dB
DR	(–60dBFS with A-weighted)		100	108	-	dB
S/N	(A-weighted)		100	108	-	dB
Load Capacitance		(Note 9)	-	-	30	pF
Load Resistance		(Note 10)	5	-	-	kΩ
Interchannel Isolation			90	107	-	dB
Interchannel Gain Mismatch			-	0	0.5	dB
Gain Drift			-	100	-	ppm/°C
Power Supply Rejection		(Note 11)	-	50	-	dB

Note 7. This value is the full scale (0dB) of the input voltage. Input voltage is proportional to AVDD voltage. Vin = 0.8 x AVDD (Vpp).

Note 8. This value is the full scale (0dB) of the output voltage. Output voltage is proportional to AVDD voltage. Vout = 0.76 x AVDD (Vpp).

Note 9. When LOUT/ROUT drives some capacitive load, a 220Ω resistor should be added in series between LOUT/ROUT and capacitive load. In this case, LOUT/ROUT pins can drive a capacitor of 400pF.

Note 10. For AC-load

Note 11. VCOM pin is connected to VSS1 pin with 1µF±50% capacitor in series.
When LDOE pin = "L", PSR is applied to AVDD, VDD18 and TVDD with 1kHz, 50mVpp.
When LDOE pin = "H", PSR is applied to AVDD and TVDD with 1kHz, 50mVpp.

Ta=25℃; AVDD=3.3V, TVDD=VDD18=1.8V;
Slave Mode, MCKI=24.576MHz, ADC Single Input / DAC Single Output (LDOE pin= “L”)
Register Setting: TDM1-0 bits = “00”, DIF2-0 bits = “111”, CKS1-0 bits = “10”, DFS1-0 bits = “00”
Output Pin Load: DAC Single-end＝4.7kohm, 33pF, LRCK=BICK=SDTO pins=22pF

Parameter		Min.	Typ.	Max.	Unit
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = “H”)					
AVDD	fs=48kHz, 96kHz, 192kHz		12.0	16.0	mA
TVDD+VDD18	fs=48kHz		6.0	9.0	mA
	fs=96kHz		10.0	15.0	mA
	fs=192kHz		10.0	15.0	mA
Power-down mode					
(PDN pin = “L”) (Note 12)			1	100	μA
AVDD+ TVDD+VDD18					

Note 12. Powered-down. All digital input pins are held VSS2.

9. ADC Filter Characteristics (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD =2.4~ 3.6V, TVDD=1.7~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF): SHARP ROLL-OFF (SLAD bit="0" ; SDAD bit="0")						
Passband (Note 13)	0dB/-0.06dB –6.0dB	PB	0 -	- 24.4	22.1 -	kHz kHz
Stopband (Note 13)		SB	27.8	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	19	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (SLAD bit="0" ; SDAD bit="1")						
Passband (Note 13)	0dB/-0.06dB –6.0dB	PB	0 -	- 24.4	22.1 -	kHz kHz
Stopband (Note 13)		SB	27.8		-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	2.6	1/fs
Group Delay (Note 14)		GD	-	5.0	-	1/fs
ADC Digital Filter (Decimation LPF): SLOW ROLL-OFF (SLAD bit="1" ; SDAD bit="0")						
Passband (Note 13)	0dB/-0.074dB –6.0dB	PB	0 -	- 21.9	12.5 -	kHz kHz
Stopband (Note 13)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	7.0	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF (SLAD bit="1" ; SDAD bit="1")						
Passband (Note 13)	0dB/-0.074dB –6.0dB	PB -	0 -	- 21.9	12.5 -	kHz kHz
Stopband (Note 13)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 14)		GD	-	5.0	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response	–3.0dB –0.5dB	FR	- -	1.0 2.5	- -	Hz Hz
(Note 13)	–0.1dB		-	6.5	-	Hz

Note 13. The passband and stopband frequencies scales with fs (sampling frequency).
For example, PB(0dB/-0.06dB) = 0.46 x fs (@fs=48kHz) for ADC block(SHARP ROLL-OFF).
For example, PB(0dB/-0.074dB) = 0.26 x fs (@fs=48kHz) for ADC block(SLOW ROLL-OFF).

Note 14. The calculated delay time by digital filtering. This is the time from the input of an analog signal to the output of MSB for L channel of SDTO. The error of the delay at audio interface is within +1[1/fs].

10. ADC Filter Characteristics (fs=96kHz)

(Ta= -40 ~ +105°C; AVDD =2.4~ 3.6V, TVDD=1.7~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF): SHARP ROLL-OFF (SLAD bit="0" ; SDAD bit="0")						
Passband (Note 13)	0dB/-0.06dB –6.0dB	PB	0	- 48.7	44.2	kHz kHz
Stopband (Note 13)		SB	55.6	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	19	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (SLAD bit="0" ; SDAD bit="1")						
Passband (Note 13)	0dB/-0.06dB –6.0dB	PB	0 -	- 48.7	44.2 -	kHz kHz
Stopband (Note 13)		SB	55.6		-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	2.6	1/fs
Group Delay (Note 14)		GD	-	5.0	-	1/fs
ADC Digital Filter (Decimation LPF): SLOW ROLL-OFF (SLAD bit="1" ; SDAD bit="0")						
Passband (Note 13)	0dB/-0.074dB –6.0dB	PB	0 -	- 43.7	25	kHz kHz
Stopband (Note 13)		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	7.0	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF FILTER (SLAD bit="1" ; SDAD bit="1")						
Passband (Note 13)	0dB/-0.074dB –6.0dB	PB	0 -	- 43.7	25 -	kHz kHz
Stopband (Note 13)		SB	73	-	-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 14)		GD	-	5.0	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response	–3.0dB	FR	- -	2.0 5.0	- -	Hz Hz
(Note 13)	–0.1dB		-	13	-	Hz

Note 13. The passband and stopband frequencies scales with fs (sampling frequency).
For example, PB(0dB/-0.06dB) = 0.46 x fs (@fs=96kHz) for ADC block(SHARP ROLL-OFF).
For example, PB(0dB/-0.074dB) = 0.26 x fs (@fs=96kHz) for ADC block(SLOW ROLL-OFF).

Note 14. The calculated delay time by digital filtering. This is the time from the input of an analog signal to the output of MSB for L channel of SDTO. The error of the delay at audio interface is within +1[1/fs].

11. ADC Filter Characteristics (fs=192kHz)

(Ta= -40 ~ +105°C; AVDD =2.4~ 3.6V, TVDD=1.6~ 1.98V, 2.4~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF): SHARP ROLL-OFF (SLAD bit="0" ; SDAD bit="0")						
Passband (Note 13)	0dB/-0.04dB –6.0dB	PB	0	- 100.1	83.7	kHz kHz
Stopband (Note 13)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	15	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (SLAD bit="0" ; SDAD bit="1")						
Passband (Note 13)	0dB/-0.04dB –6.0dB	PB	0 -	- 100.1	83.7 -	kHz kHz
Stopband (Note 13)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85		-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	0.3	1/fs
Group Delay (Note 14)		GD	-	6.0	-	1/fs
ADC Digital Filter (Decimation LPF): SLOW ROLL-OFF (SLAD bit="1" ; SDAD bit="0")						
Passband (Note 13)	0dB/-0.1dB –6.0dB	PB	0 -	- 75.2	31.1 -	kHz kHz
Stopband (Note 13)		SB	145.9	-		kHz
Stopband Attenuation		SA	85	-		dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	8.0	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF FILTER (SLAD bit="1" ; SDAD bit="1")						
Passband (Note 13)	0dB/-0.1dB –6.0dB	PB	0 -	- 75.2	31.1 -	kHz kHz
Stopband (Note 13)		SB	145.9	-		kHz
Stopband Attenuation		SA	85	-		dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	0.6	1/fs
Group Delay (Note 14)		GD	-	6.0	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response	–3.0dB	FR	- -	4.0 10.0	- -	Hz Hz
(Note 13)	–0.1dB		-	26.0	-	Hz

Note 13. The passband and stopband frequencies scales with fs (sampling frequency).
For example, PB(0dB/-0.04dB) = 0.436 x fs (@fs=192kHz) for ADC block(SHARP ROLL-OFF).
For example, PB(0dB/-0.1dB) = 0.16 x fs (@fs=192kHz) for ADC block(SLOW ROLL-OFF).

Note 14. The calculated delay time by digital filtering. This is the time from the input of an analog signal to the output of MSB for L channel of SDTO. The error of the delay at audio interface is within +1[1/fs].

12. DAC Filter Characteristics (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD =2.4~ 3.6V, TVDD=1.7~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF): Sharp roll-off mode(DEM=OFF; SLDA bit="0"; SDDA bit="0")						
Passband (Note 15)	±0.05dB −6.0dB	PB	0 -	- 24.0	21.8 -	kHz kHz
Stopband		SB	26.2	-	-	kHz
Passband Ripple		PR	-0.0032		0.0032	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	27.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 18)		FR	-0.3	-	0.2	dB
DAC Digital Filter (LPF): Short delay Sharp roll-off mode (DEM=OFF; SLDA bit="0" ; SDDA bit="1")						
Passband (Note 15)	±0.05dB −6.0dB	PB	0 -	- 24.0	21.8 -	kHz kHz
Stopband		SB	26.2	-	-	kHz
Passband Ripple		PR	-0.0031		0.0031	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	6.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 18)		FR	-0.4		0.3	dB
DAC Digital Filter (LPF): Slow roll-off mode(DEM=OFF; SLDA bit="1" ; SDDA bit="0")						
Passband (Note 16)	±0.07dB −3.0dB	PB	0 -	 19.7	8.8 -	kHz kHz
Stopband		SB	42.6			kHz
Passband Ripple		PR	-0.043		0.043	dB
Stopband Attenuation		SA	73			dB
Group Delay (Note 17)		GD	-	7.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 18)		FR	-5	-	0.1	dB
DAC Digital Filter (LPF): Short delay Slow roll-off mode(DEM=OFF; SLDA bit="1" ; SDDA bit="1")						
Passband (Note 16)	±0.07dB −3.0dB	PB	0 -	- 24.3	12.1 -	kHz kHz
Stopband		SB	41.5	-	-	kHz
Passband Ripple		PR	-0.05		0.05	dB
Stopband Attenuation		SA	82	-	-	dB
Group Delay (Note 17)		GD	-	5.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 18)		FR	-5		0.1	dB

Note 15. The passband and stopband frequencies scale with fs (sampling frequency).
For example, Passband (±0.06dB) = 0.454 x fs (@ fs=48kHz).

Note 16. The passband and stopband frequencies scale with fs (sampling frequency).
For example, Passband (±0.06dB) = 0.204 x fs (@ fs=48kHz).

Note 17. The calculated delay time is resulting from digital filtering. For the DAC, this is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1[1/fs].

Note 18. The reference frequency is 1kHz.

13. DAC Filter Characteristics (fs=96kHz)

(Ta= -40 ~ +105°C; AVDD =2.4~ 3.6V, TVDD=1.7~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF): Sharp roll-off mode(DEM=OFF; SLDA bit="0" ; SDDA bit="0")						
Passband (Note 15)	±0.05dB	PB	0	-	43.5	kHz
	–6.0dB		-	48.0	-	kHz
Stopband		SB	52.5	-	-	kHz
Passband Ripple		PR	-0.0032		+0.0032	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	27.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 18)		FR	-0.4	-	0.3	dB
DAC Digital Filter (LPF): Short delay Sharp roll-off mode (DEM=OFF; SLDA bit="0" ; SDDA bit="1")						
Passband (Note 15)	±0.05dB	PB	0	-	43.5	kHz
	–6.0dB		-	48.0	-	kHz
Stopband		SB	52.5	-	-	kHz
Passband Ripple		PR	-0.0031		+0.0031	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	6.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 18)		FR	-0.4	-	0.3	dB
DAC Digital Filter (LPF): Slow roll-off mode (DEM=OFF; SLDA bit="1" ; SDDA bit="0")						
Passband (Note 16)	±0.07dB	PB	0		17.7	kHz
	–3.0dB		-	39.6	-	kHz
Stopband		SB	85.3			kHz
Passband Ripple		PR	-0.043		+0.043	dB
Stopband Attenuation		SA	73			dB
Group Delay (Note 17)		GD	-	7.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 18)		FR	-4	-	0.1	dB
DAC Digital Filter (LPF): Short delay Slow roll-off mode(DEM=OFF; SLDA bit="1" ; SDDA bit="1")						
Passband (Note 16)	±0.07dB	PB	0	-	24.2	kHz
	–3.0dB		-	44.6	-	kHz
Stopband		SB	83.0	-	-	kHz
Passband Ripple		PR	-0.05		+0.05	dB
Stopband Attenuation		SA	82	-	-	dB
Group Delay (Note 17)		GD	-	5.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 18)		FR	-5	-	0.1	dB

Note 15. The passband and stopband frequencies scale with fs (sampling frequency).
For example, Passband (±0.06dB) = 0.454 x fs (@ fs=96kHz).

Note 16. The passband and stopband frequencies scale with fs (sampling frequency).
For example, Passband (±0.06dB) = 0.204 x fs (@ fs=96kHz).

Note 17. The calculated delay time is resulting from digital filtering. For the DAC, this is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1[1/fs].

Note 18. The reference frequency is 1kHz.

14. DAC Filter Characteristics (fs=192kHz)

(Ta= -40 ~ +105°C; AVDD =2.4~ 3.6V, TVDD=1.7~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF): Sharp roll-off mode(DEM=OFF; SLDA bit="0" ; SDDA bit="0")						
Passband (Note 15)	±0.05dB −6.0dB	PB	0 -	- 96.0	87.0 -	kHz kHz
Stopband		SB	105	-	-	kHz
Passband Ripple		PR	-0.0032		+0.0032	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	27.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 18)		FR	-1.0	-	1.0	dB
DAC Digital Filter (LPF): Short delay Sharp roll-off mode (DEM=OFF; SLDA bit="0" ; SDDA bit="1")						
Passband (Note 15)	±0.05dB −6.0dB	PB	0 -	- 96.0	87.0 -	kHz kHz
Stopband		SB	105	-	-	kHz
Passband Ripple		PR	-0.0031		+0.0031	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay (Note 17)		GD	-	6.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 18)		FR	-1.0	-	1.0	dB
DAC Digital Filter (LPF): Slow roll-off mode (DEM=OFF; SLDA bit="1" ; SDDA bit="0")						
Passband (Note 16)	±0.07dB −3.0dB	PB	0 -	 79.1	35.5 -	kHz kHz
Stopband		SB	171			kHz
Passband Ripple		PR	-0.043		+0.043	dB
Stopband Attenuation		SA	73			dB
Group Delay (Note 17)		GD	-	7.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 18)		FR	-5.0	-	0.1	dB
DAC Digital Filter (LPF): Short delay Slow roll-off mode (DEM=OFF; SLDA bit="1" ; SDDA bit="1")						
Passband (Note 16)	±0.07dB −3.0dB	PB	0 -	- 89.2	48.4 -	kHz kHz
Stopband		SB	165.9	-	-	kHz
Passband Ripple		PR	-0.05		+0.05	dB
Stopband Attenuation		SA	82	-	-	dB
Group Delay (Note 17)		GD	-	5.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 18)		FR	-5.0	-	0.1	dB

Note 15. The passband and stopband frequencies scale with fs (sampling frequency).
For example, Passband (±0.06dB) = 0.454 x fs (@ fs=192kHz).

Note 16. The passband and stopband frequencies scale with fs (sampling frequency).
For example, Passband (±0.06dB) = 0.204 x fs (@ fs=192kHz).

Note 17. The calculated delay time is resulting from digital filtering. For the DAC, this is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1[1/fs].

Note 18. The reference frequency is 1kHz.

15. DC Characteristics

(Ta= -40 ~ +105°C; AVDD=2.4~3.6V, TVDD=1.7~ 3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
TVDD ≤ 3.0V					
High-Level Input Voltage (CKS3, CKS2, CKS1, CKS0/TDMI, SDTI, LRCK, BICK, MCKI, PMADL/SCL, PMADR/SDA, PMDAL/CAD0, PMDAR/CAD1, PS, LDOE and PDN pins)	VIH	80%TVDD	-	-	V
Low-Level Input Voltage (CKS3, CKS2, CKS1, CKS0/TDMI, SDTI, LRCK, BICK, MCKI, PMADL/SCL, PMADR/SDA, PMDAL/CAD0, PMDAR/CAD1, PS, LDOE and PDN pins)	VIL	-	-	20%TVDD	V
TVDD > 3.0V					
High-Level Input Voltage (CKS3, CKS2, CKS1, CKS0/TDMI, SDTI, LRCK, BICK, MCKI, PMADL/SCL, PMADR/SDA, PMDAL/CAD0, PMDAR/CAD1, PS, LDOE and PDN pins)	VIH	70%TVDD	-	-	V
Low-Level Input Voltage (CKS3, CKS2, CKS1, CKS0/TDMI, SDTI, LRCK, BICK, MCKI, PMADL/SCL, PMADR/SDA, PMDAL/CAD0, PMDAR/CAD1, PS, LDOE and PDN pins)	VIL	-	-	30%TVDD	V
High-Level Output Voltage (SDTO,LRCK,BICK pins: Iout=-100μA)	VOH	TVDD-0.5	-	-	V
Low-Level Output Voltage (SDTO, LRCK, BICK pins: Iout= 100μA)	VOL	-	-	0.5	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.6V Iout= 3mA)	VOL	-	-	0.4	V
(SDA pin, 1.7V ≤ TVDD < 2.0V Iout= 3mA)	VOL	-	-	20%TVDD	V
Input Leakage Current	Iin	-	-	±10	μA

16. Switching Characteristics

(Ta= -40 ~ +105°C; AVDD= 2.4 ~ 3.6V; TVDD=1.7 ~ 3.6V; C_L=20pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Output Timing						
Frequency		fsn, fsd, fsq	-	Table 19	-	kHz
Stereo Mode: Duty Cycle		Duty	-	50	-	%
TDM128 Mode: (Note 19)						
I^2S compatible: Pulse Width Low		tLRCKL	-	1/(8fsn) 1/(8fsd)	-	s
MSB or LSB justified: Pulse Width High		tLRCKH	-	1/(8fsn) 1/(8fsd)	-	s
TDM256 Mode: (Note 19)						
I^2S compatible: Pulse Width Low		tLRCKL	-	1/(4fsq)	-	s
MSB or LSB justified: Pulse Width High		tLRCKH	-	1/(4fsq)	-	s
BICK Output Timing (Table 21)						
Period	BCKO1-0 bits = "00"	tBCK	-	1/(32fs)	-	s
	BCKO1-0 bits = "01"	tBCK	-	1/(64fs)	-	s
	BCKO1-0 bits = "10"	tBCK	-	1/(128fsn) 1/(128fsd)	-	s
	BCKO1-0 bits = "11"	tBCK	-	1/(256fsn)	-	s
	TDM Mode (Note 19)	tBCK	-	1/(256fsn) 1/(256fsd) 1/(128fsq)	-	s
Duty Cycle		dBCK	-	50	-	%

Note 19. In TDM modes, TVDD=3.0V~3.6V. The AK4558 does not support variable pitch mode.

Parameter		Symbol	Min.	Typ.	Max.	Unit
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency						
Normal Speed Mode:	256fs, 512fs	fsn	8	-	54	kHz
	384fs, 768fs		8	-	48	kHz
Double Speed Mode:	256fs	fsd	54	-	108	kHz
	384fs		48	-	96	kHz
Quad Speed Mode:	128fs	fsq	108	-	216	kHz
	192fs		96	-	192	kHz
Stereo mode duty cycle		Duty	45		55	%
TDM128Mode: (Note 19)						s
I^2S compatible: Pulse Width Low		tLRCKL	1/(128fsq)	-	127/(128fsq)	s
MSB or LSB justified: Pulse Width High		tLRCKH	1/(128fsq)	-	127/(128fsq)	s
TDM256 Mode: (Note 19)						
I^2S compatible: Pulse Width Low		tLRCKL	1/(256fsn) 1/(256fsd)	-	255/(256fsn) 255/(256fsd)	s
MSB or LSB justified: Pulse Width High		tLRCKH	1/(256fsn) 1/(256fsd)	-	255/(256fsn) 255/(256fsd)	s
BICK Input Timing						
Period	Stereo Mode					
	PLL3-0 bits = “0011”	tBCK	-	1/(32fs)	-	s
	PLL3-0 bits = “0010”	tBCK	-	1/(64fs)	-	s
	PLL3-0 bits = “0001”	tBCK		1/(128fsn) 1/(128fsd)		s
	PLL3-0 bits = “0000”	tBCK	-	1/(256fsn)	-	s
	TDM128 Mode PLL3-0 bits = “0001”	tBCK	-	1/(128fsq)	-	s
	TDM256 Mode PLL3-0 bits = “0000”	tBCK	-	1/(256fsn) 1/(256fsd)	-	s
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	s
Pulse Width High		tBCKH	0.4 x tBCK	-	-	s

PLL Slave Mode (PLL Reference Clock = LRCK pin)						
LRCK Input Timing						
Frequency						
Normal Speed Mode:	256fs, 512fs	fsn	8	-	54	kHz
	384fs, 768fs		8	-	48	kHz
Double Speed Mode:	256fs	fsd	54	-	108	kHz
	384fs		48	-	96	kHz
Quad Speed Mode:	128fs	fsq	108	-	216	kHz
	192fs		96	-	192	kHz
Stereo Mode: Duty Cycle		Duty	45	-	55	%
TDM128Mode:						s
I^2S compatible: Pulse Width Low		tLRCKL	1/(128fsq)	-	127/(128fsq)	s
MSB or LSB justified: Pulse Width High		tLRCKH	1/(128fsq)	-	127/(128fsq)	s
TDM256 Mode:						
I^2S compatible: Pulse Width Low		tLRCKL	1/(256fsn) 1/(256fsd)	-	255/(256fsn) 255/(256fsd)	s
MSB or LSB justified: Pulse Width High		tLRCKH	1/(256fsn) 1/(256fsd)	-	255/(256fsn) 255/(256fsd)	s
BICK Input Timing						
Period	Stereo Mode	tBCK	1/(64fs) 1/(128fsd) 1/(256fsn)	-	1/(32fsn)	s
	TDM128 Mode (Note 19)	tBCK	-	1/(128fsq)	-	s
	TDM256 Mode (Note 19)	tBCK	-	1/(256fsn) 1/(256fsd)	-	s
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	s
Pulse Width High		tBCKH	0.4 x tBCK	-	-	s

Parameter	Symbol	Min.	Typ.	Max.	Unit
External Slave Mode					
MCKI Input Timing					
External Clock					
256fsn:	fCLK	2.048	-	13.824	MHz
Pulse Width Low	tCLKL	29	-	-	ns
Pulse Width High	tCLKH	29	-	-	ns
384fsn:	fCLK	3.072	-	18.432	MHz
Pulse Width Low	tCLKL	22	-	-	ns
Pulse Width High	tCLKH	22	-	-	ns
512fsn, 256fsd, 128fsq:	fCLK	4.096	-	27.648	MHz
Pulse Width Low	tCLKL	15	-	-	ns
Pulse Width High	tCLKH	15	-	-	ns
768fsn, 384fsd, 192fsq:	fCLK	6.144	-	36.864	MHz
Pulse Width Low	tCLKL	11	-	-	ns
Pulse Width High	tCLKH	11	-	-	ns
Pulse Width Low	tCLKL	0.4/fCLK	-	-	s
Pulse Width High	tCLKH	0.4/fCLK	-	-	s
LRCK Input Timing					
Stereo mode					
(TDM1-0 bits = "00")					
Normal Speed Mode: 256fs, 512fs	fsn	8	-	54	kHz
384fs, 768fs		8	-	48	kHz
Double Speed Mode: 256fs	fsd	54	-	108	kHz
384fs		48	-	96	kHz
Quad Speed Mode: 128fs	fsq	108	-	216	kHz
192fs		96	-	192	kHz
Duty Cycle	Duty	45	-	55	%
TDM256 mode (Note 19) (Note 20)					
(TDM1-0 bits = "01")					
LRCK frequency	fsn	8	-	48	kHz
"H" time	tLRH	1/256fsn	-	-	ns
"L" time	tLRL	1/256fsn	-	-	ns
TDM256 mode (Note 19) (Note 21)					
(TDM1-0 bits = "01")					
LRCK frequency	fsd	48	-	96	kHz
"H" time	tLRH	1/256fsd	-	-	ns
"L" time	tLRL	1/256fsd	-	-	ns
TDM128 mode (Note 19) (Note 22)					
(TDM1-0 bits = "10")					
LRCK frequency	fsq	96	-	192	kHz
"H" time	tLRH	1/128fsq	-	-	ns
"L" time	tLRL	1/128fsq	-	-	ns

Note 20. The AK4558 should be in Normal Speed mode.
Note 21. The AK4558 should be in Double Speed mode.
Note 22. The AK4558 should be in Quad Speed mode.

Parameter		Symbol	Min.	Typ.	Max.	Unit
External Master Mode						
MCKI Input Timing						
External Clock						
256fsn:		fCLK	2.048	-	13.824	MHz
384fsn:		fCLK	3.072	-	18.432	MHz
512fsn, 256fsd, 128fsq:		fCLK	4.096	-	27.648	MHz
768fsn, 384fsd, 192fsq:		fCLK	6.144	-	36.864	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Output Timing						
Stereo mode						
(TDM1-0 bits = "00")						
Normal Speed Mode: 256fs, 512fs		fsn	8	-	54	kHz
384fs, 768fs			8		48	
Double Speed Mode: 256fs		fsd	54		108	
384fs			48		96	
Quad Speed Mode: 128fs		fsq	108		216	
192fs			96		192	
Stereo Mode: Duty Cycle		Duty	-	50	-	%
TDM256 mode (Note 23)						
(TDM1-0 bits = "1X")		fsn	8	-	48	kHz
LRCK frequency						
I^2S compatible: Pulse Width Low		tLRCKL	-	1/(8fsn)	-	s
MSB justified: Pulse Width High		tLRCKH	-	1/(8fsn)	-	s
TDM256 mode (Note 24)						
(TDM1-0 bits = "1X")		fsd	48	-	96	kHz
LRCK frequency						
I^2S compatible: Pulse Width Low		tLRCKL	-	1/(8fsd)	-	s
MSB justified: Pulse Width High		tLRCKH	-	1/(8fsd)	-	s
TDM128 mode (Note 25)						
(TDM1-0 bits = "01")		fsq	96	-	192	kHz
LRCK frequency						
I^2S compatible: Pulse Width Low		tLRCKL	-	1/(4fsq)	-	s
MSB justified: Pulse Width High		tLRCKH	-	1/(4fsq)	-	s
BICK Output Timing (Table 15)						
Period	BCKO1-0 bits = "00"	tBCK	-	1/(32fs)	-	s
	BCKO1-0 bits = "01"	tBCK	-	1/(64fs)	-	s
	BCKO1-0 bits = "10"	tBCK	-	1/(128fs)	-	s
	BCKO1-0 bits = "11"	tBCK	-	1/(256fsn)	-	s
	TDM Mode	tBCK	-	1/(256fsn) 1/(256fsd) 1/(128fsq)	-	s
Duty Cycle (Note 26)		dBCK	-	50	-	%

Note 23. The AK4558 should be in Normal Speed mode.
Note 24. The AK4558 should be in Double Speed mode.
Note 25. The AK4558 should be in Quad Speed mode.
Note 26. When MCKI = 256fsn or 256fsd and BICK output frequency is 256fs, or when MCKI = 128fsq and BICK output frequency is 128fs, the Duty of BICK is MCKI pulse width.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Slave mode)					
Stereo mode (TDM1-0 bits = "00")					
Normal, Double, Quad Speed Mode (TVDD= 1.7V~3.6V)					
BICK Period	tBCK	1/128fsn	-	-	ns
		1/64fsd	-	-	ns
		1/32fsq	-	-	ns
BICK Pulse Width Low	tBCKL	58	-	-	ns
Pulse Width High	tBCKH	58	-	-	ns
LRCK Edge to BICK "↑" (Note 27)	tLRB	58	-	-	ns
BICK "↑" to LRCK Edge (Note 27)	tBLR	58	-	-	ns
LRCK to SDTO(MSB) (Except I^{2}S mode)	tLRS	-	-	48	ns
BICK "↓" to SDTO	tBSD	-	-	48	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns
Normal, Double, Quad Speed Mode (TVDD= 2.7V~3.6V)					
BICK Period	tBCK	1/256fsn	-	-	ns
		1/128fsd	-	-	ns
		1/64fsq	-	-	ns
BICK Pulse Width Low	tBCKL	33	-	-	ns
Pulse Width High	tBCKH	33	-	-	ns
LRCK Edge to BICK "↑" (Note 27)	tLRB	33	-	-	ns
BICK "↑" to LRCK Edge (Note 27)	tBLR	33	-	-	ns
LRCK to SDTO(MSB) (Except I^{2}S mode)	tLRS	-	-	28	ns
BICK "↓" to SDTO	tBSD	-	-	28	ns
SDTI Hold Time	tSDH	5	-	-	ns
SDTI Setup Time	tSDS	5	-	-	ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Slave mode)					
Stereo mode (TDM1-0 bits = "00")					
TDM256 mode (Normal Speed Mode (TDM1-0 bits = "1X") (Note 23)					
BICK Period	tBCK	1/256fsn	-	-	ns
BICK Pulse Width Low	tBCKL	33	-	-	ns
Pulse Width High	tBCKH	33	-	-	ns
LRCK Edge to BICK "↑" (Note 27)	tLRB	23	-	-	ns
BICK "↑" to LRCK Edge (Note 27)	tBLR	23	-	-	ns
SDTO Setup time BICK "↑"	tBSS	5	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI/TDMI Hold Time	tSDH	5	-	-	ns
SDTI/TDMI Setup Time	tSDS	5	-	-	ns
TDM256 mode (Double Speed Mode) (TDM1-0 bits = "1X") (Note 24)					
BICK Period	tBCK	1/256fsd	-	-	ns
BICK Pulse Width Low	tBCKL	14	-	-	ns
Pulse Width High	tBCKH	14	-	-	ns
LRCK Edge to BICK "↑" (Note 27)	tLRB	14	-	-	ns
BICK "↑" to LRCK Edge (Note 27)	tBLR	14	-	-	ns
SDTO Setup time BICK "↑"	tBSS	5	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI/TDMI Hold Time	tSDH	5	-	-	ns
SDTI/TDMI Setup Time	tSDS	5	-	-	ns
TDM128 mode (Quad Speed Mode) (TDM1-0 bits = "01") (Note 25)					
BICK Period	tBCK	1/128fsq	-	-	ns
BICK Pulse Width Low	tBCKL	14	-	-	ns
Pulse Width High	tBCKH	14	-	-	ns
LRCK Edge to BICK "↑" (Note 27)	tLRB	14	-	-	ns
BICK "↑" to LRCK Edge (Note 27)	tBLR	14	-	-	ns
SDTO Setup time BICK "↑"	tBSS	5	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI/TDMI Hold Time	tSDH	5	-	-	ns
SDTI/TDMI Setup Time	tSDS	5	-	-	ns

Note 27. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Master mode)					
Stereo mode (TDM1-0 bits = "00")					
Normal ,Double, Quad Speed Mode (TVDD= 1.7V～3.6V) (Note 28)					
BICK "↓" to LRCK	tMBLR	–14	-	14	ns
LRCK to SDTO(MSB) (Except I²S mode)	tLRS	–38	-	38	ns
BICK "↓" to SDTO	tBSD	–52	-	52	ns
SDTI Hold Time	tSDH	20	-	-	ns
SDTI Setup Time	tSDS	20	-	-	ns
Normal, Double, Quad Speed Mode (TVDD= 2.7V～3.6V) (Note 29)					
BICK "↓" to LRCK	tMBLR	–7	-	7	ns
LRCK to SDTO(MSB) (Except I²S mode)	tLRS	–20	-	20	ns
BICK "↓" to SDTO	tBSD	–27	-	27	ns
SDTI Hold Time	tSDH	9	-	-	ns
SDTI Setup Time	tSDS	9	-	-	ns
TDM256 mode, TDM128 mode (TDM1-0 bits = "01", "10")					
BICK "↓" to LRCK	tMBLR	–6	-	6	ns
SDTO Setup time BICK "↑"	tBSS	5	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI/TDMI Hold Time	tSDH	5	-	-	ns
SDTI/TDMI Setup Time	tSDS	5	-	-	ns

Note 28. When BICK output frequency ≦6.912MHz.
Note 29. When BICK output frequency ＞6.912MHz.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 30)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	1.0	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 31)	tAPD	150	-	-	ns
PDN Reject Pulse Width	tRPD	-	-	30	ns
PDN "↑" to SDTO valid (Note 32)	tPDV	-	5200	-	1/fs

Note 30. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 31. The AK4558 can be reset by setting the PDN pin to "L" upon power-up.
The PDN pin must held "L" for more than 150ns for a certain reset. The AK4558 is not reset by the "L" pulse less than 30ns.

Note 32. This cycle is the numbers of LRCK rising from the PDN pin rising. (Internal power-down is released in 5ms (max.) after the PDN pin = "H")

■ Timing Diagram

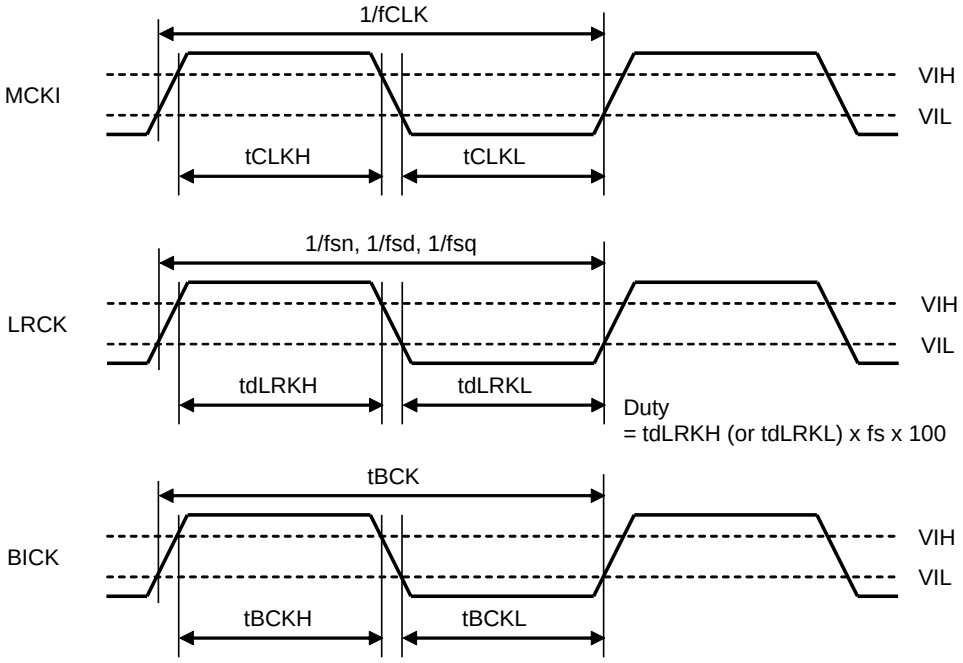


Figure 2. Clock Timing (TDM1-0 bits = “00” & Slave Mode)

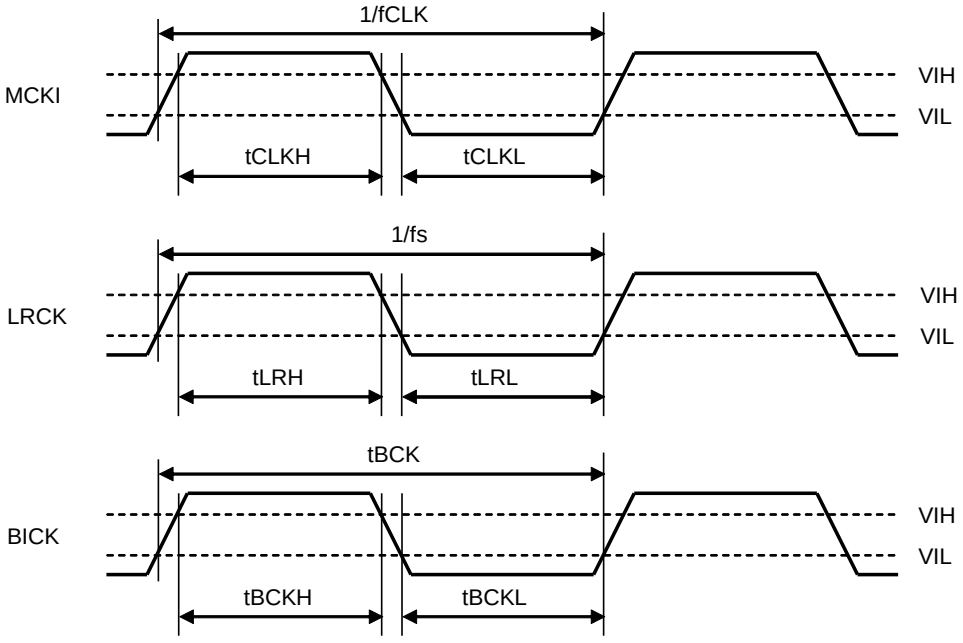


Figure 3. Clock Timing (Except TDM1-0 bits = “00” & Slave Mode)

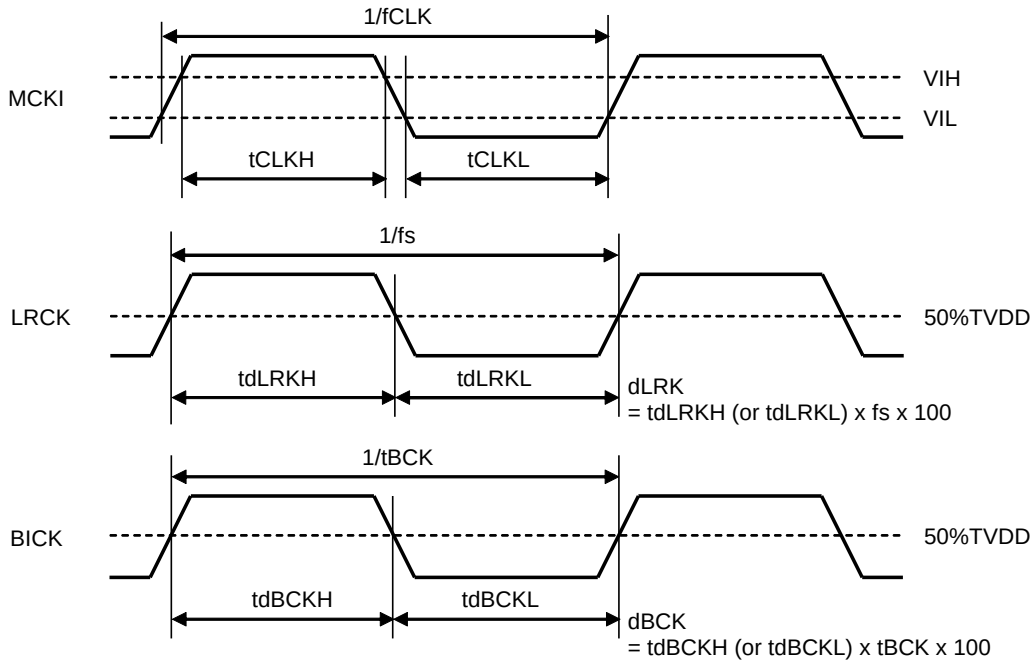


Figure 4. Clock Timing (TDM1-0 bits = “00” & Master Mode)

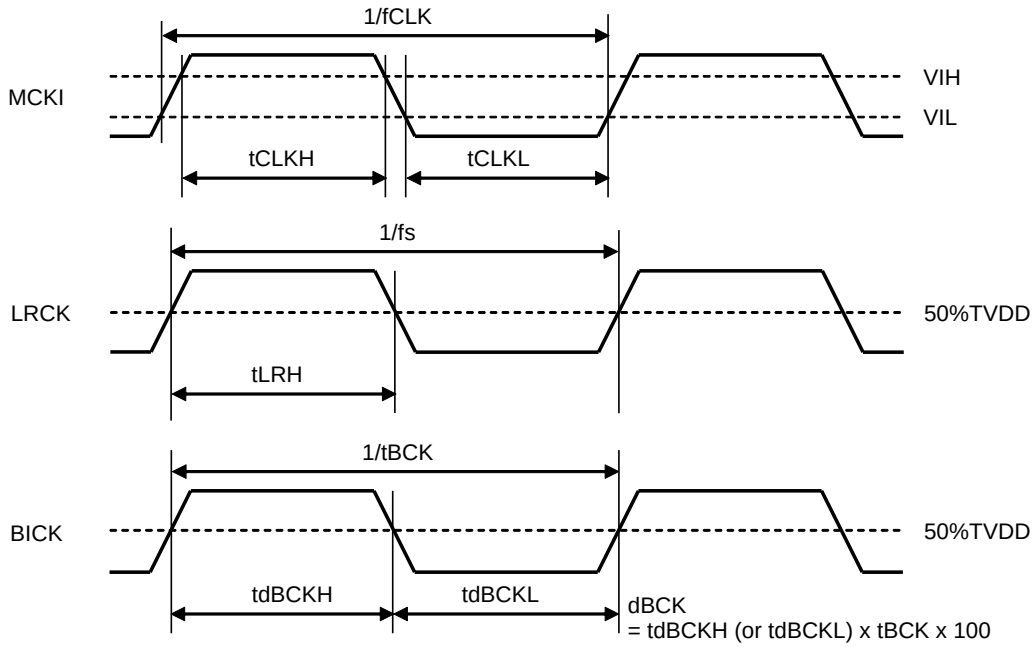


Figure 5. Clock Timing (Except TDM1-0 bits = “00” & Master Mode)

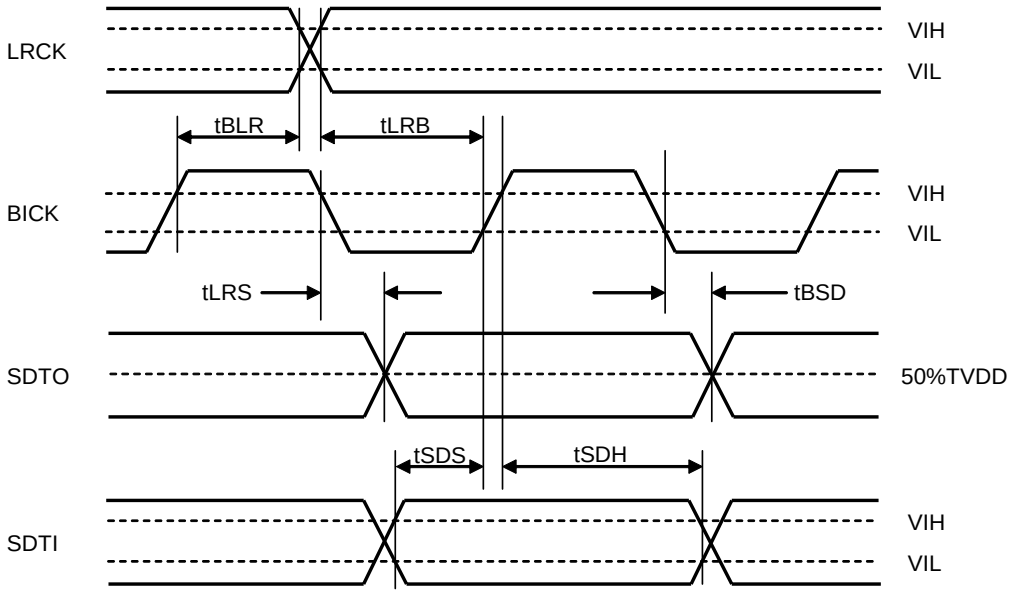


Figure 6. Audio Interface Timing (TDM1-0 bits = “00” & Slave Mode)

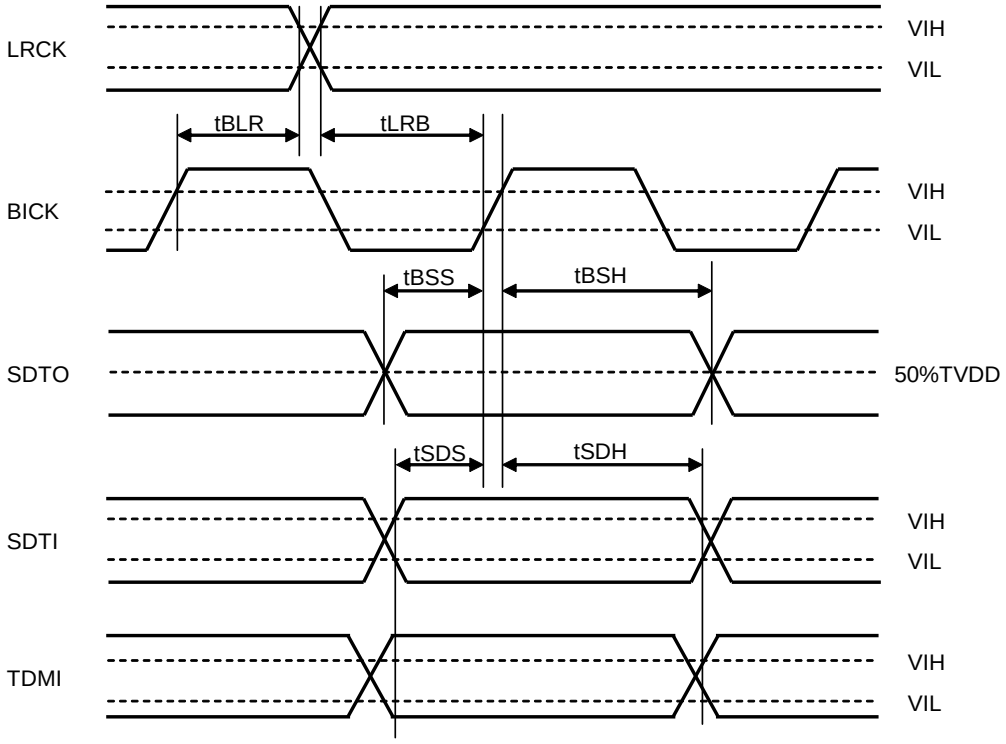


Figure 7. Audio Interface Timing (Except TDM1-0 bits = “00” & Slave Mode)

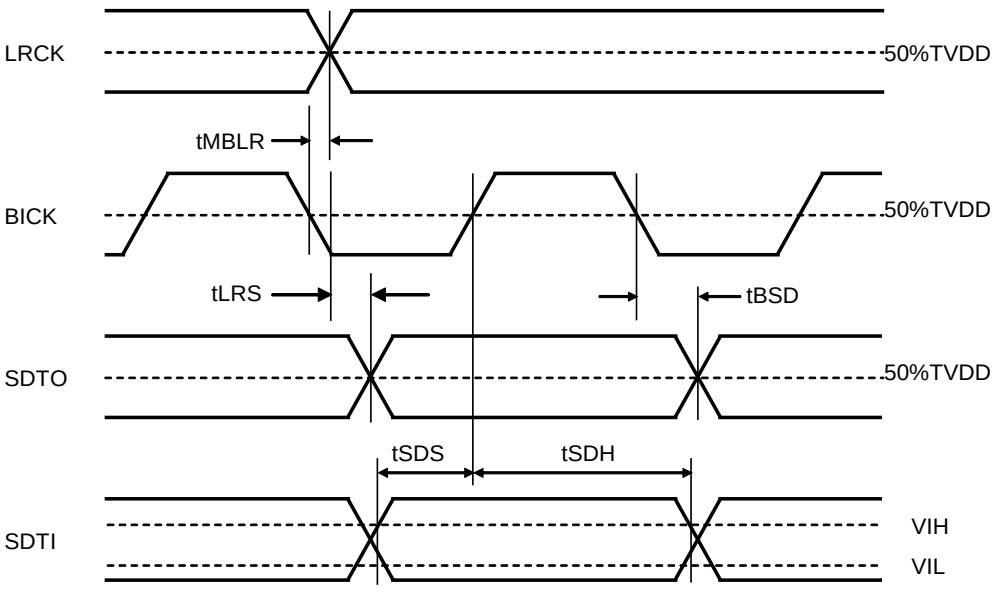


Figure 8. Audio Interface Timing (TDM1-0 bits = “00” & Master Mode)

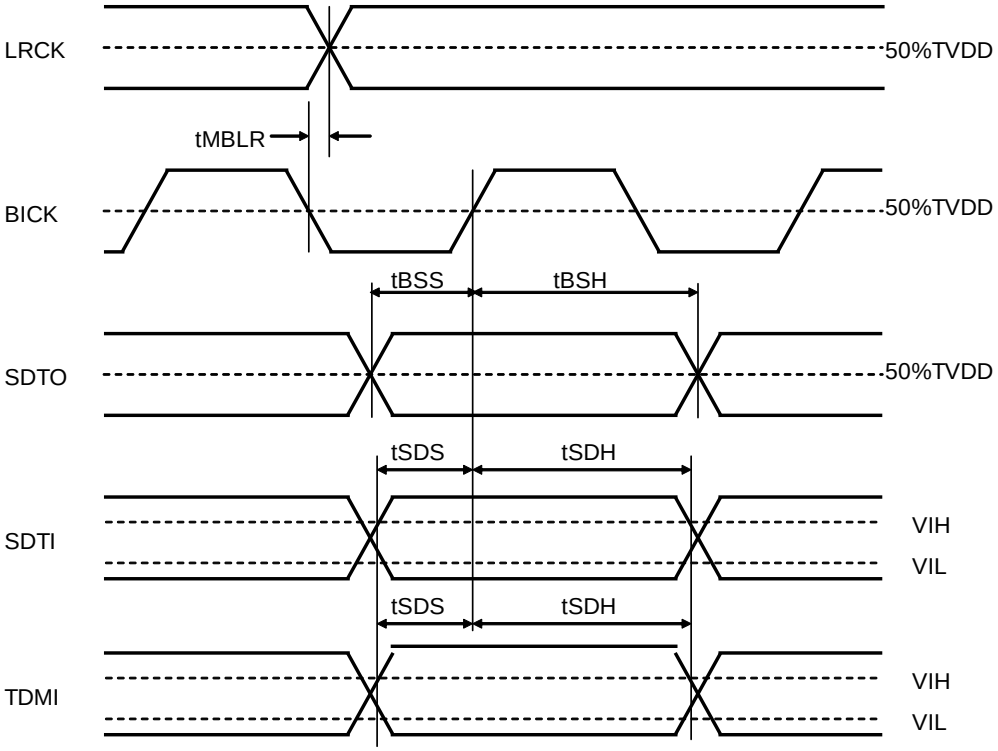


Figure 9. Audio Interface Timing (Except TDM1-0 bits = “00” & Master Mode)

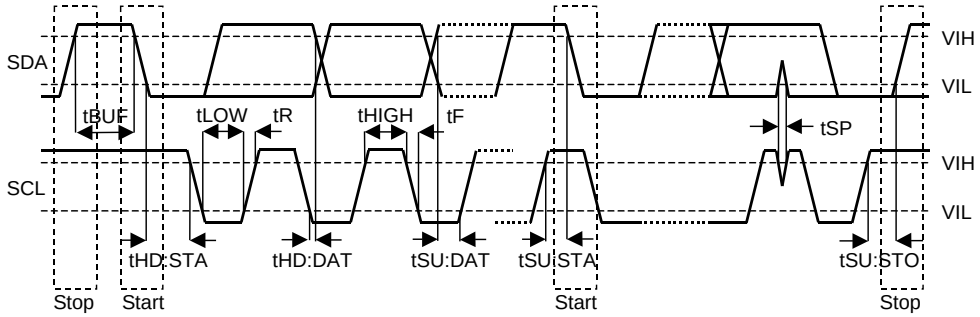


Figure 10. I^{2}C Bus Mode Timing

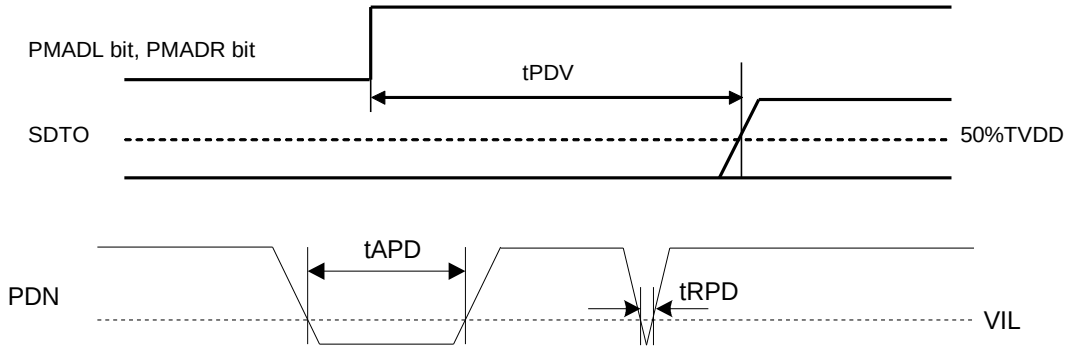


Figure 11. Power-down & Reset Timing

17. Functional Descriptions

■ Parallel / Serial Mode

The AK4558 is in parallel control mode (not using I^2C bus) by setting the PS pin = “H”. Operation mode in parallel control mode is selected by the CKS3-0 pins. I^2C bus of the AK4458 is available when the PS pin = “L”. When the AK4558 is in operation, setting of the PS pin cannot be changed.

■ Master Mode/Slave Mode

The CKS3and CKS2 pins select either master or slave mode. When the CKS3 pin = “H” and CKS2 pin = H”, the AK4558 is in master mode. The AK4558 is in slave mode with all other settings.

CKS3 pin	CKS2 pin	Mode
L	L	Slave Mode
L	H	Slave Mode
H	L	Slave Mode
H	H	Master Mode

Table 1. Select Master/Slave Mode

PDN pin	CKS3 pin	CKS2 pin	LRCK pin	BICK pin
L	L	L	Input	Input
	L	H	Input	Input
	H	L	Input	Input
	H	H	“L” Output	“L” Output
H	L	L	Input	Input
	L	H	Input	Input
	H	L	Input	Input
	H	H	Output	Output

Table 2. LRCK, BICK pin

■ System Clock

There are four clock modes to interface with external devices (Table 3, Table 4).

Mode	PMPLL bit	CKS3-2 pins	PLL3-0 bits	Figure
PLL Master Mode	1	"HH"	Table 16	Figure 14
PLL Slave Mode (PLL Reference Clock: LRCK or BICK pin)	1	"LL" "LH"	Table 16	Figure 16
EXT Slave Mode	0	"HL"	x	Figure 12
EXT Master Mode	0	"HH"	x	Figure 13

Table 3. Clock Mode Setting (x: Don't care)

PS pin	Mode	MCKI pin	BICK pin	LRCK pin
"H" Parallel Mode	EXT Slave Mode	Selected by CKS3-0 pins	Input (≥ 32fs)	Input (1fs)
	EXT Master Mode	Selected by CKS3-0 pins	Output (64fs)	Output (1fs)
"L" Serial Mode	PLL Master Mode	Selected PLL3-0 bits	Output (Selected by BCKO1-0 bits)	Output (1fs)
	PLL Slave Mode (PLL Reference Clock: LRCK or BICK pin)	Connect to VSS2	Input (Selected by PLL3-0 bits)	Input (1fs)
	EXT Slave Mode	ACKS bit = "1" or ACKS bit = "0" and DFS1-0 bits	Input (≥ 32fs)	Input (1fs)
	EXT Master Mode	Selected by MCKS1-0 bits and DFS1-0 bits	Output (Selected by BCKO1-0 bits)	Output (1fs)

Table 4. Clock Pin States in Clock Mode

■ Parallel Mode (PS pin= “H”)

The external clocks, which are required to operate the AK4558, are MCKI, BICK and LRCK. MCKI should be synchronized with LRCK but the phase is not critical. MCKI frequencies that corresponds normal audio rate are shown in Table 5. MCKI frequency, BICK frequency, HPF ON/OFF switching and Master/Slave mode switching are controlled by the CKS3-0 pins The AK4558 does not support variable pitch mode when the MCKI is 192fs, 384fs or 768fs (Table 6).

fs	MCKI					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	N/A	N/A	8.192MHz	12.288MHz	16.384MHz	24.576MHz
44.1kHz	N/A	N/A	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz
48kHz	N/A	N/A	12.288MHz	18.432MHz	24.576MHz	36.864MHz
96kHz	N/A	N/A	24.576MHz	36.864MHz	N/A	N/A
192kHz	24.576MHz	36.864MHz	N/A	N/A	N/A	N/A

Table 5. System Clock Example (N/A: Not Available)

Mode	Sampling Frequency	MCKI
Normal Speed	8kHz ≤ fs ≤ 54kHz	256fs/512fs
	8kHz ≤ fs ≤ 48kkHz	384fs/768fs
Double Speed	54kHz < fs ≤ 108kHz	256fs
	48kHz < fs ≤ 96kHz	384fs
Quad Speed	108kHz < fs ≤ 216kHz	128fs
	96kHz < fs ≤ 192kHz	192fs

Table 6. Sampling Frequency Range

Mode	CKS3 pin	CKS2 pin	CKS1 pin	CKS0 pin	HPF	M/S	MCKI	Audio Interface Format
0	L	L	L	L	ON	Slave	128/192fs (Quad Speed) 256/384fs (Double Speed) 512/768fs (Normal Speed)	32bit LJ/RJ (Mode 5) Table 23
1	L	L	L	H	ON	Slave	256/384/512/768fs (Normal Speed)	
2	L	L	H	L	OFF	Slave	128/192fs (Quad Speed) 256/384fs (Double Speed) 512/768fs (Normal Speed)	
3	L	L	H	H	OFF	Slave	256/384/512/768fs (Normal Speed)	
4	L	H	L	L	ON	Slave	128/192fs (Quad Speed) 256/384fs (Double Speed) 512/768fs (Normal Speed)	32bit I^2S (Mode 7) Table 23
5	L	H	L	H	ON	Slave	256/384/512/768fs (Normal Speed)	
6	L	H	H	L	OFF	Slave	128/192fs (Quad Speed) 256/384fs (Double Speed) 512/768fs (Normal Speed)	
7	L	H	H	H	OFF	Slave	256/384/512/768fs (Normal Speed)	
8	H	L	L	L	ON	Slave	128/192fs (Quad Speed) 256/384fs (Double Speed) 512/768fs (Normal Speed)	32bit LJ (Mode 6) Table 23
9	H	L	L	H	ON	Slave	256/384/512/768fs (Normal Speed)	
10	H	L	H	L	OFF	Slave	128/192fs (Quad Speed) 256/384fs (Double Speed) 512/768fs (Normal Speed)	
11	H	L	H	H	OFF	Slave	256/384/512/768fs (Normal Speed)	
12	H	H	L	L	ON	Master	256fs (Double Speed)	32bit I^2S (Mode 15) Table 23
13	H	H	L	H	ON	Master	512fs (Normal Speed)	
14	H	H	H	L	ON	Master	128fs (Quad Speed)	
15	H	H	H	H	ON	Master	256fs (Normal Speed)	

Table 7. Mode Setting

Note 33. When the PS pin = “L”, only Master/Slave mode setting is valid by the CKS3 and CKS2 pins.

■ Serial Mode (PS pin= “L”)

EXT Mode (PMPLL bit = “0”)

The external clocks which are required to operate the AK44558 in slave mode are MCKI, LRCK and BICK. MCKI should be synchronized with LRCK but the phase is not critical. There are two methods to set MCKI frequency; Manual Setting Mode and Auto Setting Mode. In Manual Setting Mode (ACKS bit= “0”: Default), the sampling speed is set by DFS0 and DFS1 bits (Table 8). The frequency of MCKI at each sampling speed is set automatically. (Table 10, Table 11, Table 12). In Auto Setting Mode (ACKS bit= “1”), as MCKI frequency is detected automatically (Table 13) and the internal master clock attains the appropriate frequency (Table 14), so it is not necessary to set DFS.

In master mode, only MCKI is required. Master Clock Input Frequency should be set with the MCKS1-0 bits (Table 9), and the sampling speed should be set by the DFS1-0 bits (Table 8). The frequencies and the duties of the clocks (LRCK, BICK) are not stable immediately after setting MCKS1-0 bits and DFS1-0 bits up. After exiting reset upon power-up in master mode, the AK4558 is in power-down mode until MCKI is input.

After exiting reset upon power-up in slave mode, the AK4558 is in power-down mode until MCKI, LRCK and BICK are input.

If the clock is stopped, click noise occurs when restarting the clock. Mute the digital output externally.

DFS1	DFS0	Sampling Speed Mode (fs)		
0	0	Normal Speed Mode	8kHz~54kHz	(default)
0	1	Double Speed Mode	48kHz~108kHz	
1	0	Quad Speed Mode	96kHz~216kHz	
1	1	Quad Speed Mode	96kHz~216kHz	

Table 8. Sampling Speed (Manual Setting Mode)

MCKS1	MCKS0	Normal Speed Mode	Double Speed Mode	Quad Speed Mode	
0	0	256fs	256fs	128fs	
0	1	384fs	256fs	128fs	
1	0	512fs	256fs	128fs	(default)
1	1	768fs	256fs	128fs	

Table 9. Master Clock Input Frequency Select (Master Mode)

LRCK	MCKI (MHz)				BICK (MHz)
fs	256fs	384fs	512fs	768fs	64fs
8.0kHz	2.0480	3.0720	4.0960	6.1440	0.5120
32.0kHz	8.1920	12.2880	16.3840	24.5760	2.0480
44.1kHz	11.2896	16.9344	22.5792	33.8688	2.8224
48.0kHz	12.2880	18.4320	24.5760	36.8640	3.0720

Table 10. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCKI (MHz)	BICK (MHz)
fs	256fs	64fs
88.2kHz	22.5792	5.6448
96.0kHz	24.5760	6.1440
108.0kHz	27.6480	6.9120

Table 11. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCKI (MHz)	BICK (MHz)
fs	128fs	64fs
176.4kHz	22.5792	11.2896
192.0kHz	24.5760	12.2880
216.0kHz	27.6480	13.8240

Table 12. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCKI		Sampling Speed Mode
512fs	768fs	Normal Speed Mode
256fs	384fs	Double Speed Mode
128fs	192fs	Quad Speed Mode

Table 13. Sampling Speed (Auto Setting Mode)

LRCK	MCKI (MHz)						Sampling Speed Mode
fs	128fs	192fs	256fs	384fs	512fs	768fs	
8.0kHz	-	-	-	-	4.0960	6.1440	Normal Speed Mode
32.0kHz	-	-	-	-	16.3840	24.5760	
44.1kHz	-	-	-	-	22.5792	33.8688	
48.0kHz	-	-	-	-	24.5760	36.8640	
88.2kHz	-	-	22.5792	33.8688	-	-	Double Speed Mode
96.0kHz	-	-	24.5760	36.8640	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	Quad Speed Mode
192.0kHz	24.5760	36.8640	-	-	-	-	
216.0kHz	27.6480	-	-	-	-	-	

Table 14. System Clock Example (Auto Setting Mode)

Mode	BCKO1 bit	BCKO0 bit	BICK Output Frequency (Stereo mode)	BICK Output Frequency (TDM mode)	
0	0	0	32fsn,32fsd,32fsq	N/A (Note 34)	
1	0	1	64fsn,64fsd,64fsq	N/A (Note 34)	(default)
2	1	0	128fsn, 128fsd	N/A (Note 34)	
3	1	1	256fsn	256fsn,256fsd,128fsq	

Table 15. BICK Output Frequency at Master Mode

Note 34. Mode0, Mode1 and Mode2 can not be used in TDM modes.

EXT Slave Mode (PMPLL bit = "0", CKS3-2 pins = "LL" or "LH" or "HL")

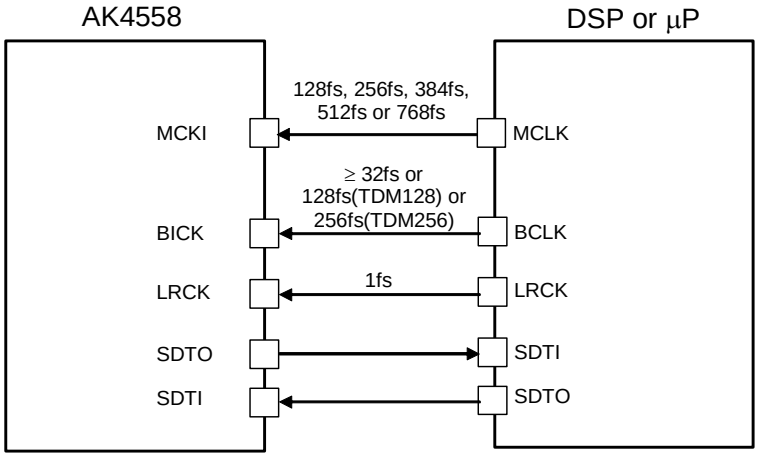


Figure 12. EXT Slave Mode

EXT Master Mode (PMPLL bit = "0", CKS3-2 pins = "HH")

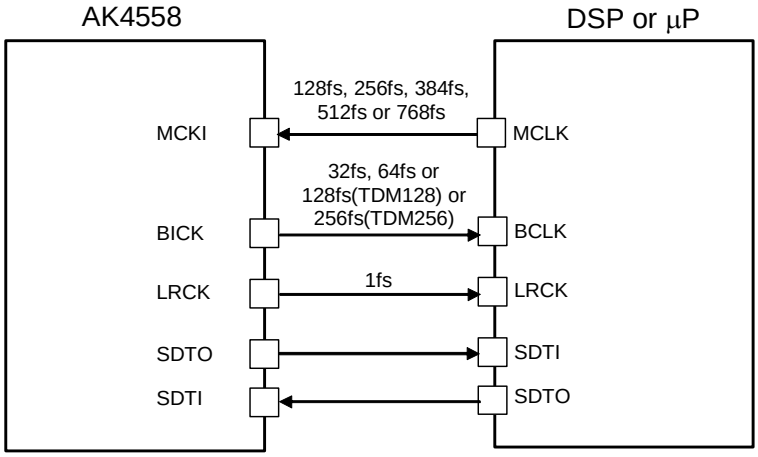


Figure 13. EXT Master Mode

■ PLL Mode (PMPLL bit = "1")

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock times, when the AK4558 is supplied stable clocks or the sampling frequency is changed after PLL is powered-up (PMPLL bit = "0" → "1"), are shown in Table 16. In Mode 15 (LRCK reference), the VCOC pin must be connected to VSS via a 10nF capacitor. In other modes, the VCOC pin must be connected to VSS directly.

1) PLL Mode Setting

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	Connection of VCOC pin C[F]	PLL Lock Time (max)	
0	0	0	0	0	BICK pin	256fs	VSS	2ms	
1	0	0	0	1	BICK pin	128fs	VSS	2ms	
2	0	0	1	0	BICK pin	64fs	VSS	2ms	
3	0	0	1	1	BICK pin	32fs	VSS	2ms	(default)
4	0	1	0	0	MCKI pin	11.2896MHz	VSS	10ms	(Note 35)
5	0	1	0	1	MCKI pin	12.288MHz	VSS	10ms	(Note 36)
6	0	1	1	0	MCKI pin	12MHz	VSS	10ms	
7	0	1	1	1	MCKI pin	24MHz	VSS	10ms	
8	1	0	0	0	MCKI pin	19.2MHz	VSS	10ms	
10	1	0	1	0	MCKI pin	13MHz	VSS	10ms	
11	1	0	1	1	MCKI pin	26MHz	VSS	10ms	
12	1	1	0	0	MCKI pin	13.5MHz	VSS	10ms	
13	1	1	0	1	MCKI pin	27MHz	VSS	10ms	
15	1	1	1	1	LRCK pin	1fs	10n ± 50%	40ms	

Table 16. Setting of PLL Mode (fs: Sampling Frequency)

Note 35. The AK4558 should be in EXT Master Mode when fs = 22.05kHz or 44.1kHz.
Note 36. The AK4558 should be in EXT Master Mode when fs = 16kHz, 24kHz, 32kHz or 48kHz.

2) Sampling Frequency Setting in PLL Mode

When the PLL reference clock input is the MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in Table 17.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency (Note 37)	
0	0	0	0	0	8kHz mode	
1	0	0	0	1	11.025kHz mode	
2	0	0	1	0	12kHz mode	
3	0	0	1	1	16kHz mode	
4	0	1	0	0	22.05kHz mode	
5	0	1	0	1	24kHz mode	(default)
6	0	1	1	0	32kHz mode	
7	0	1	1	1	44.1kHz mode	
8	1	0	0	0	48kHz mode	
9	1	0	0	1	64kHz mode	
10	1	0	1	0	88.2 kHz mode	
11	1	0	1	1	96 kHz mode	
12	1	1	0	0	128 kHz mode	
13	1	1	0	1	176.4 kHz mode	
14	1	1	1	0	192 kHz mode	
15	1	1	1	1	192 kHz mode	

Table 17. Setting of Sampling Frequency at PMPLL bit = "1"

Note 37. When the MCKI pin is the PLL reference clock input, the sampling frequency generated by PLL differs from the sampling frequency of mode name in some combinations of MCKI frequency(PLL3-0 bits) and sampling frequency (FS3-0 bits). Refer to Table 19 for the details of sampling frequency. In master mode, LRCK and BICK output frequency correspond to sampling frequencies shown in Table 19.

When the PLL reference clock input is the LRCK pin or the BICK pin, the sampling frequency is selected by FS3-1 bits as defined in Table 18. When the BICK pin is the PLL reference clock input, the sampling frequency generated by PLL is the same sampling frequency of mode name.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	0	x	8kHz ≤ fs ≤ 13.5kHz	
1	0	0	1	x	12kHz < fs ≤ 27kHz	
2	0	1	0	x	24kHz < fs ≤ 54kHz	(default)
3	0	1	1	x	48kHz < fs ≤ 108kHz	
4	1	0	0	x	96kHz < fs ≤ 216kHz	
Others	Others				N/A	

Table 18. Setting of Sampling Frequency at PLL3-2 bits = "00" or PLL3-0 bits = "1111", and PMPLL bit = "1" in PLL Slave Mode (PLL Mode 0-3: BICK Reference, Mode15: LRCK Reference) (PLL Reference Clock: LRCK or BICK pin), (x: Do not care, N/A: Not Available)

Input Frequency MCKI[MHz]	Sampling Frequency Mode	Sampling Frequency generated by PLL [kHz](Note 19)
11.2896	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	64kHz mode	64.000000
	96kHz mode	96.000000
	128kHz mode	128.000000
	192kHz mode	192.000000
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
	88.2kHz mode	88.200000
	176.4kHz mode	176.400000
12.288	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	64kHz mode	64.000000
	128kHz mode	128.000000
	96kHz mode	96.000000
	192kHz mode	192.000000
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
	88.2kHz mode	88.200000
	176.4kHz mode	176.400000
12	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	64kHz mode	64.000000
	96kHz mode	96.000000
	128kHz mode	128.000000
	192kHz mode	192.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
	88.2kHz mode	88.199013
	176.4kHz mode	176.398026

24	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	64kHz mode	64.000000
	96kHz mode	96.000000
	128kHz mode	128.000000
	192kHz mode	192.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
	88.2kHz mode	88.199013
	176.4kHz mode	176.398026

	Sampling frequency that differs from sampling frequency of mode name

Input Frequency MCKI[MHz]	Sampling Frequency Mode	Sampling Frequency generated by PLL [kHz](Note 38)
19.2	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	64kHz mode	64.000000
	96kHz mode	96.000000
	128kHz mode	128.000000
	192kHz mode	192.000000
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
	88.2kHz mode	88.200000
	176.4kHz mode	176.400000
13	8kHz mode	7.999786
	12kHz mode	11.999679
	16kHz mode	15.999572
	24kHz mode	23.999358
	32kHz mode	31.999144
	48kHz mode	47.998716
	64kHz mode	63.998288
	96kHz mode	95.997432
	128kHz mode	127.996575
	192kHz mode	191.994863
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
	88.2kHz mode	88.199013
	176.4kHz mode	176.398026

26	8kHz mode	7.999786
	12kHz mode	11.999679
	16kHz mode	15.999572
	24kHz mode	23.999358
	32kHz mode	31.999144
	48kHz mode	47.998716
	64kHz mode	63.998288
	96kHz mode	95.997432
	128kHz mode	127.996575
	192kHz mode	191.994863
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
	88.2kHz mode	88.199013
	176.4kHz mode	176.398026
13.5	8kHz mode	8.000300
	12kHz mode	12.000451
	16kHz mode	16.000601
	24kHz mode	24.000901
	32kHz mode	32.001202
	48kHz mode	48.001803
	64kHz mode	64.002404
	96kHz mode	96.003606
	128kHz mode	128.004808
	192kHz mode	192.007212
	11.025kHz mode	11.025218
	22.05kHz mode	22.050436
	44.1kHz mode	44.100871
	88.2kHz mode	88.201742
	176.4kHz mode	176.403485
27	8kHz mode	8.000300
	12kHz mode	12.000451
	16kHz mode	16.000601
	24kHz mode	24.000901
	32kHz mode	32.001202
	48kHz mode	48.001803
	64kHz mode	64.002404
	96kHz mode	96.003606
	128kHz mode	128.004808
	192kHz mode	192.007212
	11.025kHz mode	11.025218
	22.05kHz mode	22.050436
	44.1kHz mode	44.100871
	88.2kHz mode	88.201742
	176.4kHz mode	176.403485
	Sampling frequency that differs from sampling frequency of mode name	

Note 38. These are rounded off to six decimal places.

Table 19. Sampling Frequency at PLL mode (Reference clock is MCKI)

■ PLL Unlock State

PLL Master Mode (PMPLL bit = “1”, CKS3-2 pins = “HH”)

In this mode, LRCK and BICK pins output “L” until the PLL goes to lock state after PMPLL bit = “0” → “1”. (Table 20).

After PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

To avoid invalid outputs of BICK and LRCK pins, set PMPLL bit = “0” once when changing sampling frequency. It enables to output “L” signal without invalid clocks.

PLL State	BICK pin	LRCK pin
After PMPLL bit “0” → “1”	“L” Output	“L” Output
PLL Unlock (except the case above)	Invalid	Invalid
PLL Lock	Table 21	1fs Output

Table 20. Clock Operation at PLL Master Mode (PMPLL bit = “1”, CKS3-2 pins =”HH”)

■ PLL Master Mode (PMPLL bit = “1”, CKS3-2 pins = “HH”)

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 19MHz, 24MHz, 26MHz or 27MHz) is input to the MCKI pin, the internal PLL circuit generates BICK and LRCK clocks. The BICK output frequency is selected from 32fs, 64fs, 128fs and 256fs by BCKO1-0 bits (Table 21).

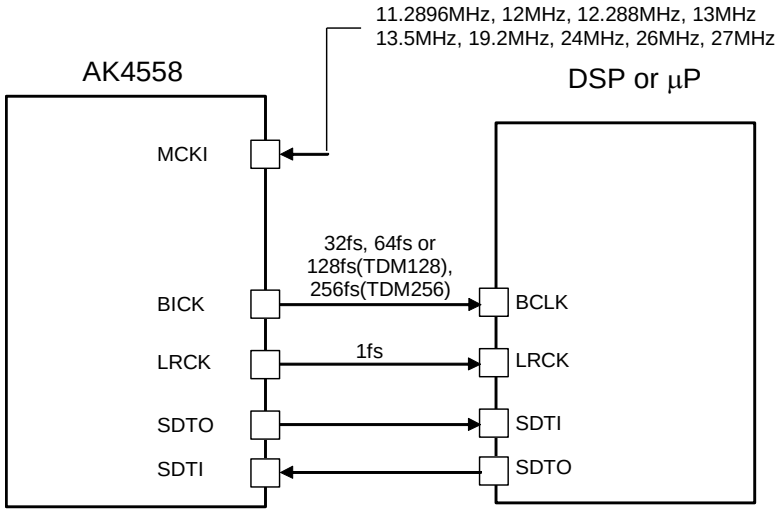


Figure 14. PLL Master Mode

Mode	BCKO1 bit	BCKO0 bit	BICK Output Frequency (Stereo mode)	BICK Output Frequency (TDM mode)	
0	0	0	32fsn,32fsd,32fsq	N/A (Note 39)	
1	0	1	64fsn,64fsd,64fsq	N/A (Note 39)	(default)
2	1	0	128fsn, 128fsd	N/A (Note 39)	
3	1	1	256fsn	256fsn,256fsd,128fsq	

Table 21. BICK Output Frequency at Master Mode (N/A: Not Available)

Note 39. Mode0, Mode1 and Mode2 cannot be used in TDM modes.

■ PLL Slave Mode (PMPLL bit = “1”, CKS3-2 pins = “LL” or “LH” or “HL”)

A reference clock of PLL is selected among the input clocks to the BICK pin or the LRCK pin. The required clock for the AK4558 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 16).

a) PLL Reference Clock: BICK pin

The required clock for the AK4558 is generated by an internal PLL circuit with the BICK input clock. PLL reference clock is selected by PLL3-0 bits. BICK and LRCK inputs must be synchronized. 8kHz ~ 216kHz sampling frequency is supported and it can be set by FS3-0 bits (Table 17).

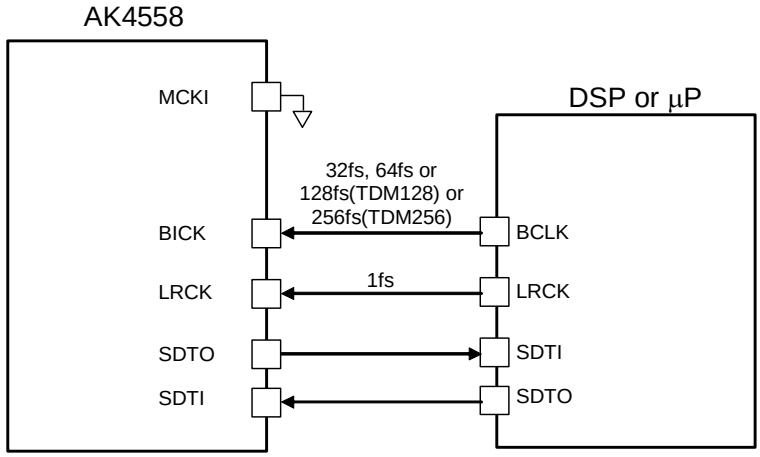


Figure 15. PLL Slave Mode 1 (PLL Reference Clock: BICK pin)

b) PLL Reference Clock: LRCK pin

The required clock for the AK4558 is generated by an internal PLL circuit with the LRCK input clock. Set PLL3-0 bits = “1111”. BICK and LRCK inputs must be synchronized. 8kHz ~ 216kHz sampling frequency is supported and it can be set by FS3-0 bits (Table 17).

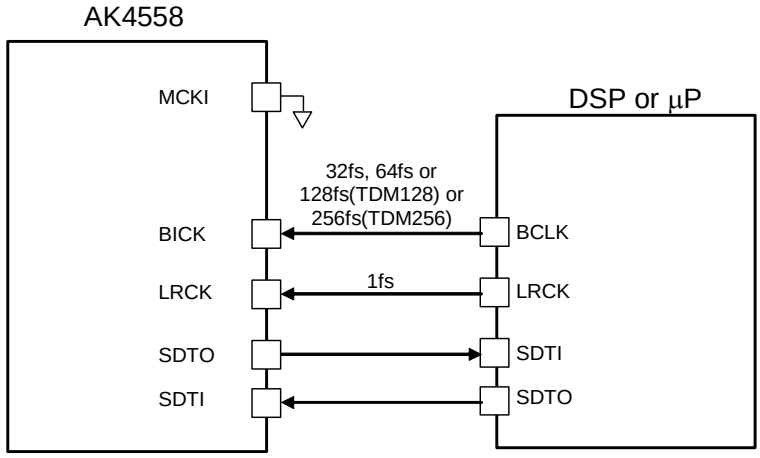


Figure 16. PLL Slave Mode 2 (PLL Reference Clock: LRCK pin)

■ De-emphasis Filter

DEM1-0 bits control a digital de-emphasis filter for DAC (SDTI) inputs. This filter (tc=50/15μs) is composed by IIR filter and corresponds to three frequencies (32kHz, 44.1kHz, 48kHz). It is always OFF in double and quad speed modes.

Mode	Sampling Speed Mode	DEM1	DEM0	DEM	
0	Normal Speed Mode	0	0	44.1kHz	
1	Normal Speed Mode	0	1	OFF	(default)
2	Normal Speed Mode	1	0	48kHz	
3	Normal Speed Mode	1	1	32kHz	
4	Double Speed Mode	Don't Care	Don't Care	OFF	
5	Quad Speed Mode	Don't Care	Don't Care	OFF	

Table 22. De-emphasis Filter Control

■ Digital HPF

The ADC has a Digital High Pass Filter (HPF) for DC-offset cancellation. The cut-off frequency of the HPF is 1Hz at fs=48kHz and the frequency response at 20Hz is -0.12dB. It also scales with the sampling frequency (fs). The HPF is controlled by CKS3-0 pins (Table 7). If the HPF setting (ON/OFF) is changed in operation, click noise occurs by changing DC offset. It is recommended to change HPF setting during power-down state (PDN pin = "L").

When the PS pin = "L", L and R channel HPFs can be ON/OFF independently by HPFEL and HPFER bits, respectively.

■ Audio Interface Format

Eight types of data formats are available and selected by setting the DIF2-0 bits (Table 23). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the AK4558 in master mode, but must be input to the AK4558 in slave mode. The SDTO is clocked out on the falling edge ("↓") of BICK and the SDTI is latched on the rising edge ("↑") of BICK.

Mode	CKS3-2 pins	TDM1 bit	TDM0 bit	DIF2 bit	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure
0	00 01 10	0	0	0	0	0	24bit MSB justified (Note 41)	16bit LSB justified	≥32fs	Figure 17
1		0	0	0	0	1	24bit MSB justified (Note 41)	20bit LSB justified	≥40fs	Figure 18
2		0	0	0	1	0	24bit MSB justified	24bit MSB justified	≥48fs	Figure 19
3		0	0	0	1	1	16bit I^{2}S Compatible		32fs	Figure 20
							24bit I^{2}S Compatible		≥48fs	Figure 21
4		0	0	1	0	0	24bit MSB justified	24bit LSB justified	≥48fs	Figure 22
5		0	0	1	0	1	32bit MSB justified	32bit LSB justified	≥64fs	Figure 23
6		0	0	1	1	0	32bit MSB justified	32bit MSB justified	≥64fs	Figure 24
7		0	0	1	1	1	32bit I^{2}S Compatible		≥64fs	Figure 25
8	11	0	0	0	0	0	24bit MSB justified (Note 41)	16bit LSB justified	≥32fs	Figure 17
9	11	0	0	0	0	1	24bit MSB justified	20bit LSB justified	≥40fs	Figure 18
10	11	0	0	0	1	0	24bit MSB justified	24bit MSB justified	≥48fs	Figure 19
11	11	0	0	0	1	1	16bit I^{2}S Compatible		32fs	Figure 20
							24bit I^{2}S Compatible		≥48fs	Figure 21
12	11	0	0	1	0	1	24bit MSB justified	32bit LSB justified	≥64fs	Figure 22
13	11	0	0	1	0	1	32bit MSB justified	32bit LSB justified	≥64fs	Figure 23
14	11	0	0	1	1	0	32bit MSB justified	32bit MSB justified	≥64fs	Figure 24
15	11	0	0	1	1	1	32bit I^{2}S Compatible		≥64fs	Figure 25

Table 23. Audio Interface Format (Stereo Mode) (N/A: Not available)

Note 40. Longer BICK than selected bit-length should be input each channel.
Note 41. When BICK is under 48fs, the output bit-length of the SDTO pin is limited by the number of BICK in half cycle of LRCK.

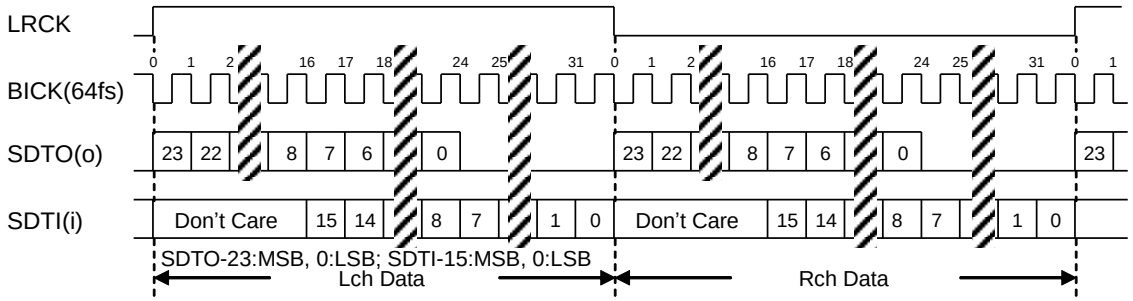


Figure 17. Mode 0/8 Timing

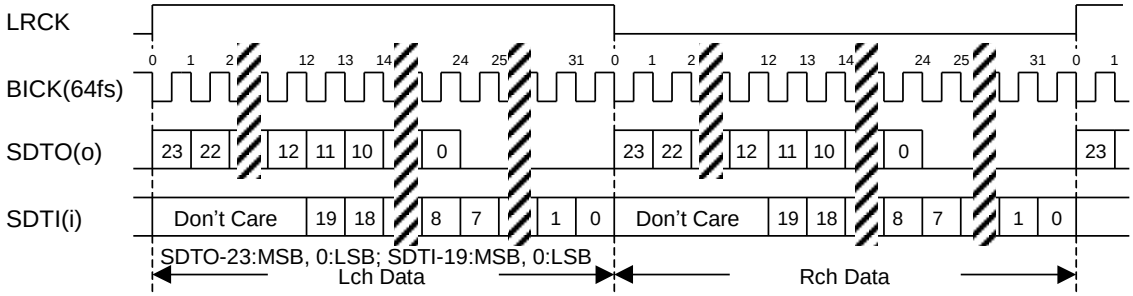


Figure 18. Mode 1/9 Timing

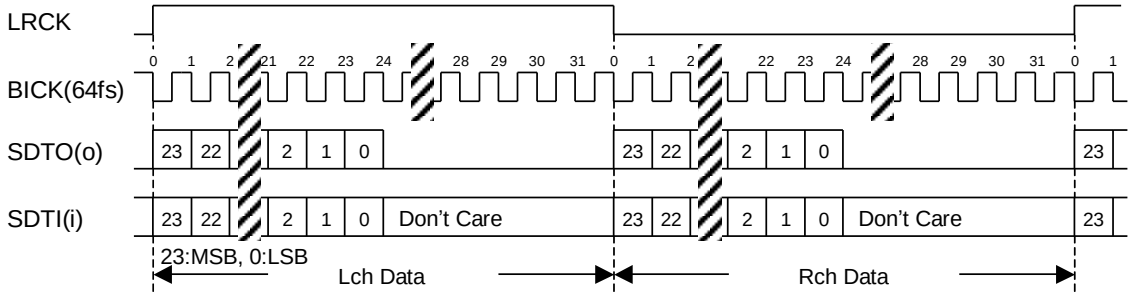


Figure 19. Mode 2/10 Timing

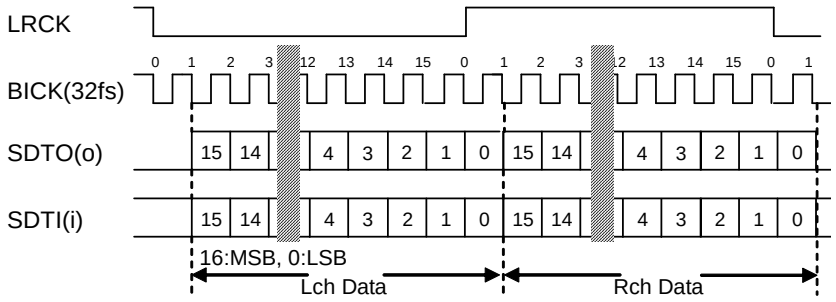


Figure 20. Mode 3/11 Timing (32fs)

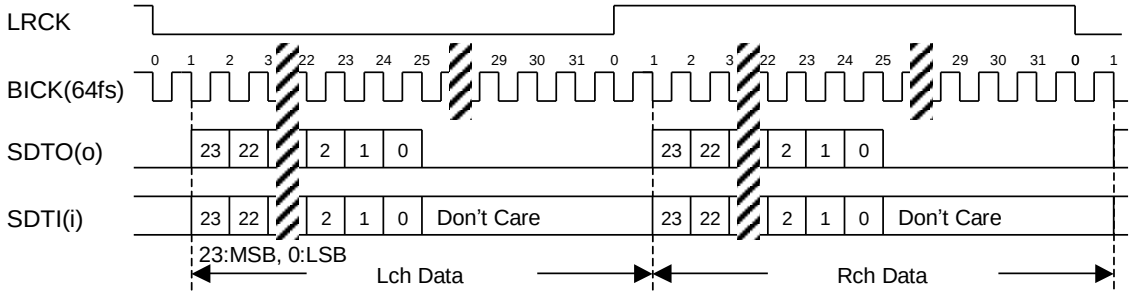


Figure 21. Mode 3/11 Timing (≥48fs)

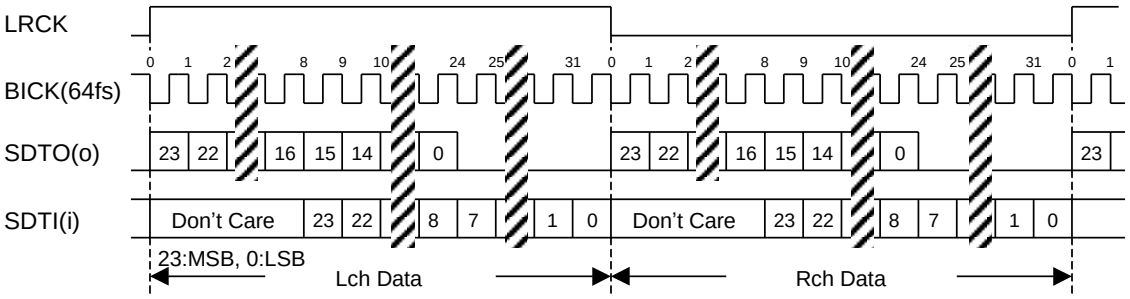


Figure 22. Mode 4/12 Timing

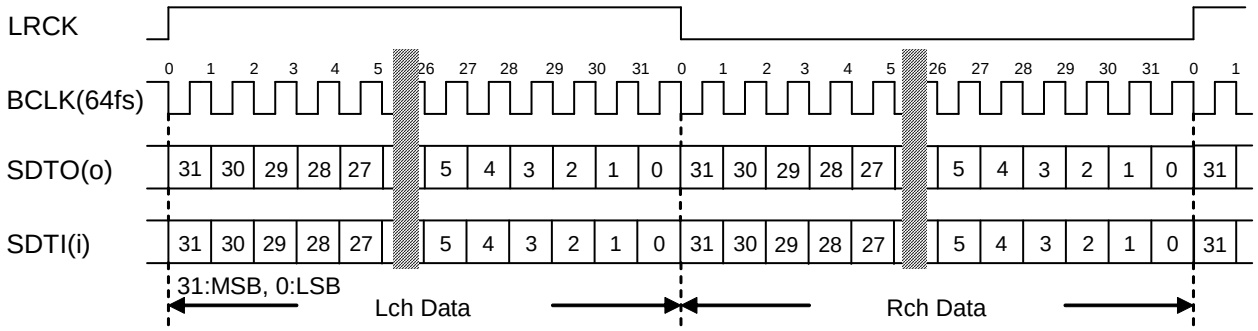


Figure 23. Mode 5/13 Timing

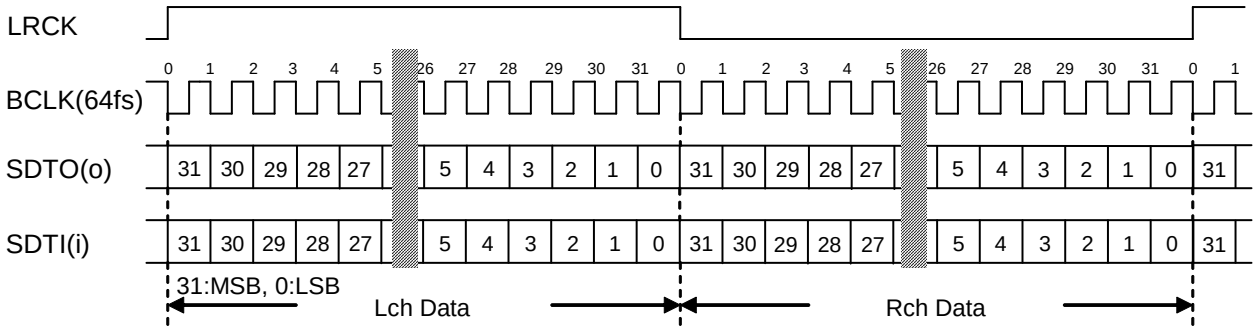


Figure 24. Mode 6/14 Timing

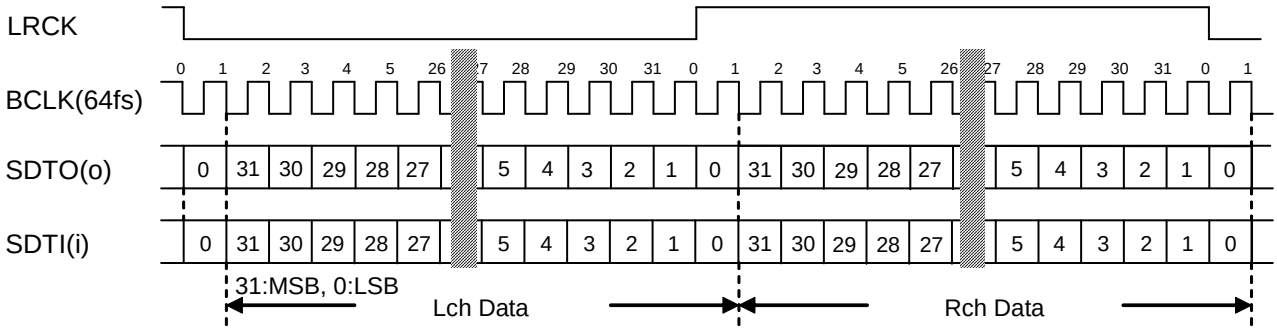


Figure 25. Mode 7/15 Timing

■ TDM Cascade Mode

a) ADC

A cascade connection of four AK4558s (max.) is supported in TDM256 mode and two AK4558s (max.) is supported in TDM128 mode.

(1) TDM256 Mode (Normal or Double speed Mode)

The SDTO pin of device #1, #2, and #3 are connected with the TDMI pin of device #2, #3 and #4, respectively. It is possible to output 8 channel TDM data from the SDTO pin of device #4 as shown in Figure 26 and Figure 27.

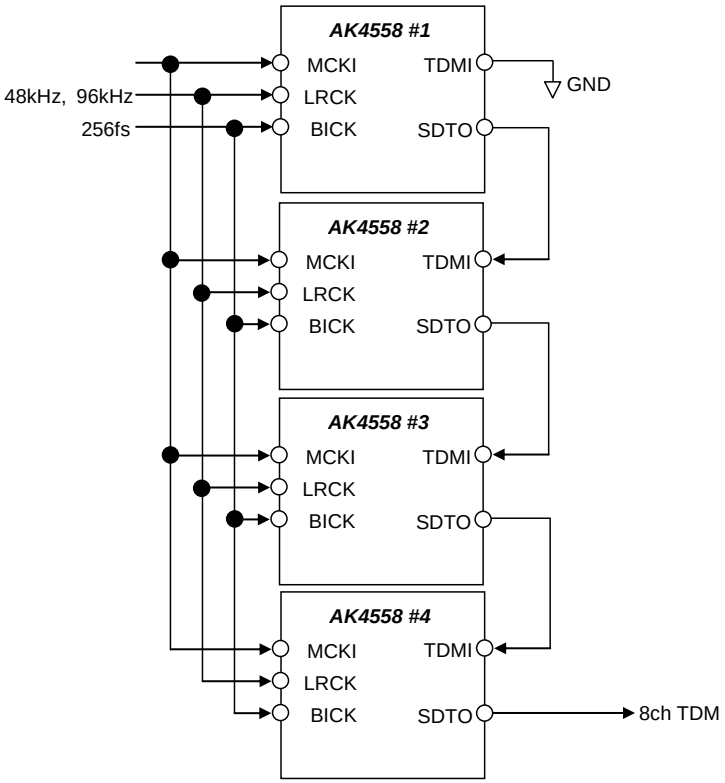


Figure 26. Cascade TDM256 Connection Diagram

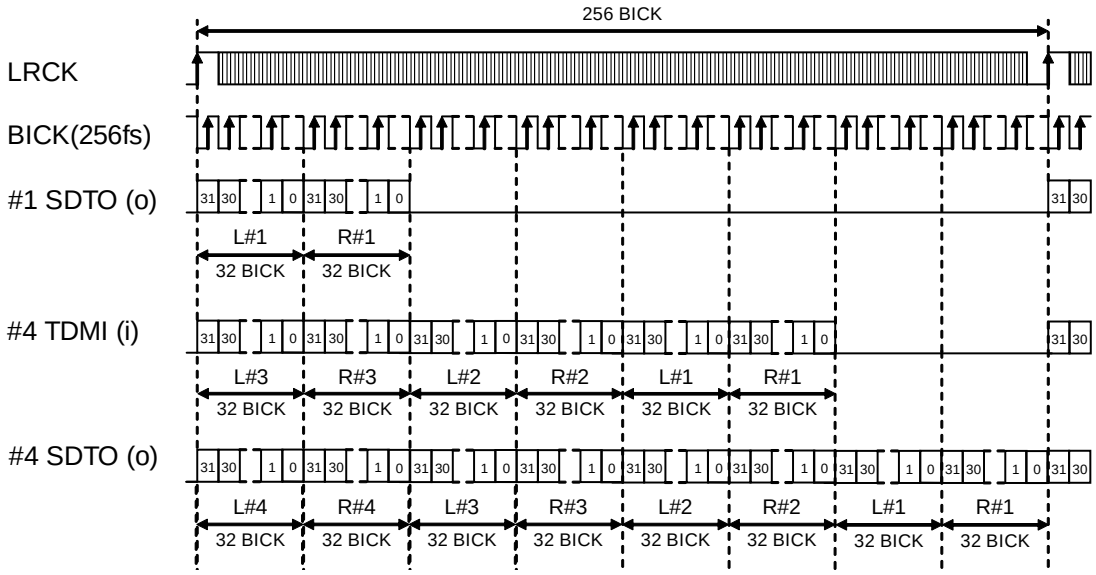


Figure 27. Cascade TDM Timing (Mode 20; TDM256 mode, MSB justified, Slave mode)

(2) TDM128 Mode

The SDTO pin of device #1 is connected with the TDMI pin of device #2. It is possible to output 4 channel TDM data from the SDTO pin of device #2 as shown in Figure 28 and Figure 29.

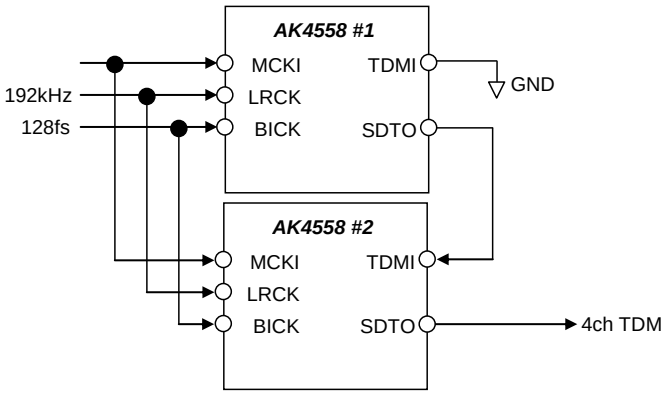


Figure 28. Cascade TDM128 Connection Diagram

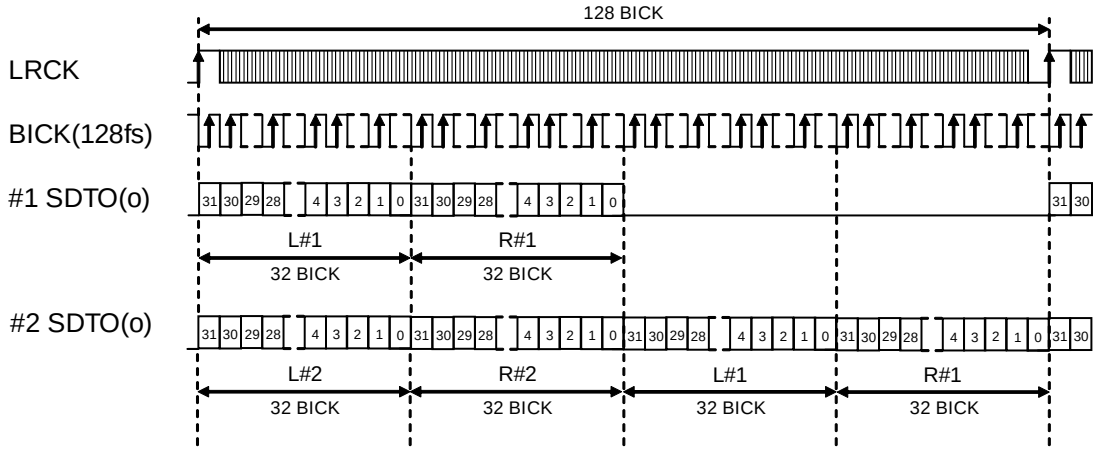


Figure 29. Cascade TDM Timing (Mode 32; TDM128 mode, MSB justified, Slave mode)

b) DAC

(1) TDM256 Mode (Normal, Double Mode)

By setting TDM1-0 bits = “1X” and SDS1-0 bits, eight channel outputs can be supported at maximum. The SDTI input data of the AK4558 #1, #2, #3 and #4 can be selected as DAC TDM data by SDS1-0 bits (Table 24). LOUT/ROUT pins of each device output the data set by SDS1-0 bits as shown in Figure 31.

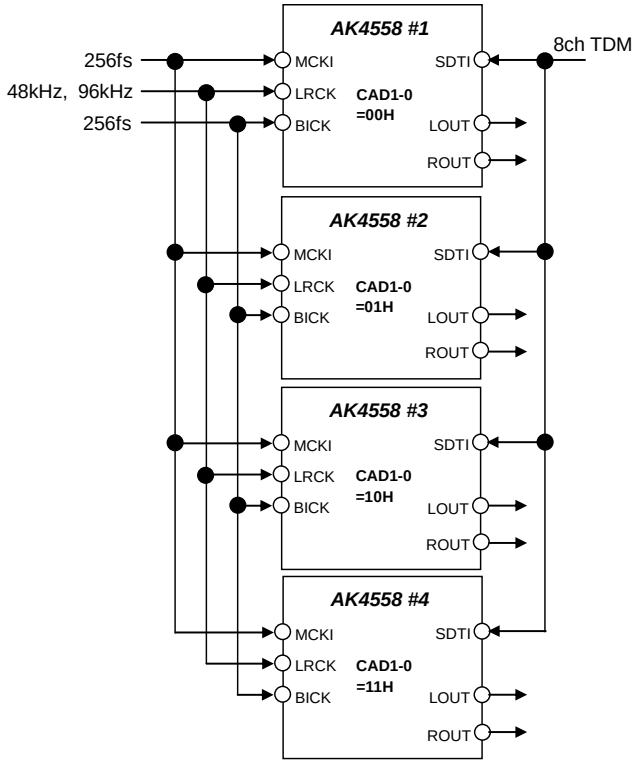


Figure 30. Cascade TDM256 Connection Diagram

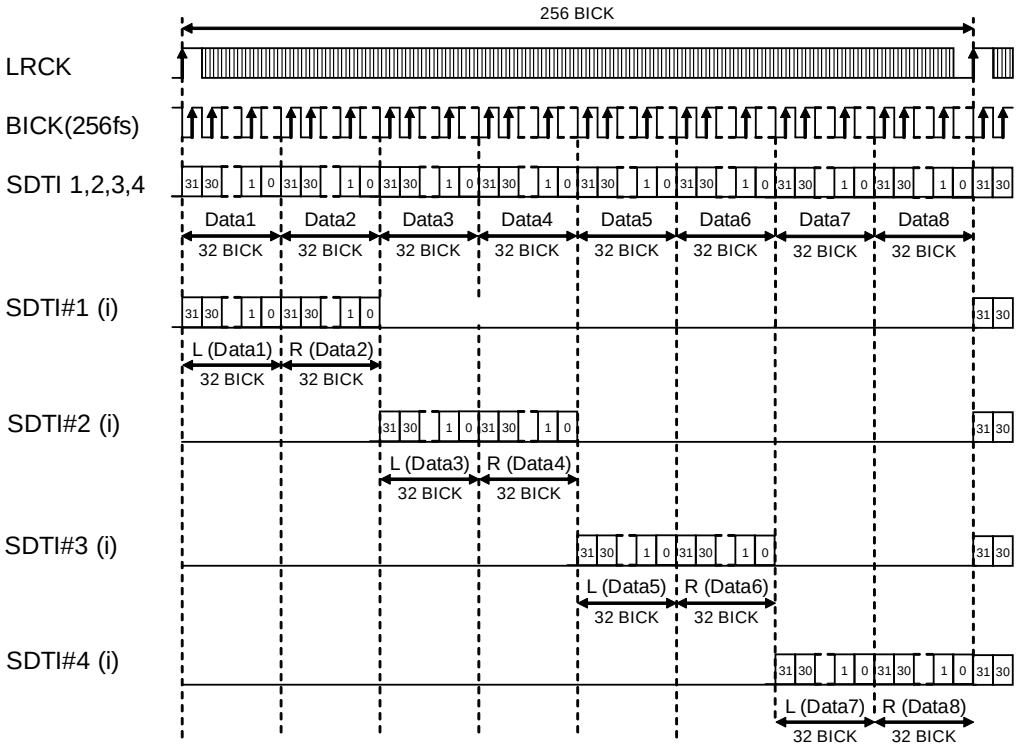


Figure 31. Cascade TDM Timing (Mode 22; TDM256 mode, MSB justified, Slave mode)

(2)TDM128 Mode (Quad Mode)
By setting TDM1-0 bits = “01” and SDS1-0 bits, four channel outputs can be supported at maximum. The SDTI input data of the AK4558 #1 and #2 can be selected as DAC TDM data by SDS1-0 bits (Table 24).

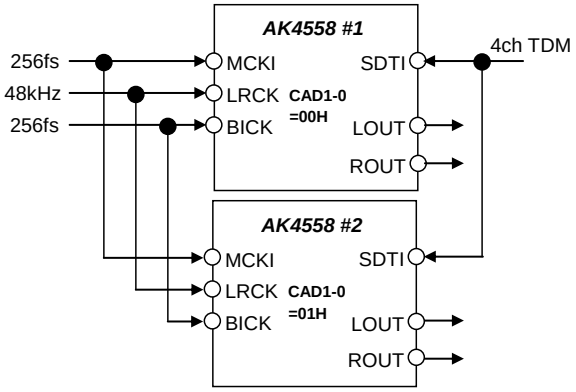


Figure 32. Cascade TDM128 Connection Diagram

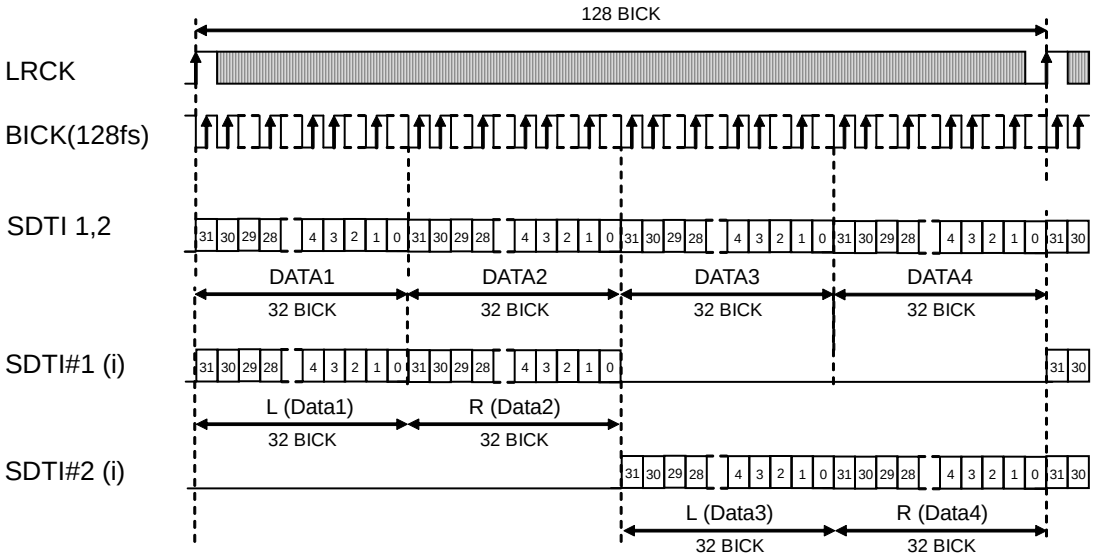


Figure 33. Cascade TDM Timing (Mode 32; TDM128 mode, MSB justified, Slave mode)

Mode			SDS1	SDS0	TDM Data	
0	TDM128	TDM256	0	0	L(Data1)/R(Data2)	(default)
1			0	1	L(Data3)/R(Data4)	
2	-		1	0	L(Data5)/R(Data6)	
3	-		1	1	L(Data7)/R(Data8)	

Table 24. DAC TDM Data Select (SDS 1-0 bits)

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO (ADC)	SDTI (DAC)	BICK	Figure
	0	1	x	0	0	0	N/A			
	0			0	0	1	N/A			
16	0			0	1	0	24bit MSB justified	24bit MSB justified	256fs	Figure 34
17	0			0	1	1	24bit I^2S Compatible		256fs	Figure 35
18	0			1	0	0	24bit MSB justified	24bit LSB justified	256fs	Figure 36
19	0			1	0	1	32bit MSB justified	32bit LSB justified	256fs	Figure 36
20	0			1	1	0	32bit MSB justified	32bit MSB justified	256fs	Figure 34
21	0			1	1	1	32bit I^2S Compatible		256fs	Figure 35
	1			0	0	0	N/A			
	1			0	0	1	N/A			
22	1			0	1	0	24bit MSB justified	24bit MSB justified	256fs	Figure 34
23	1			0	1	1	24bit I^2S Compatible		256fs	Figure 35
24	1			1	0	0	24bit MSB justified	24bit LSB justified	256fs	Figure 36
25	1			1	0	1	32bit MSB justified	32bit LSB justified	256fs	Figure 36
26	1			1	1	0	32bit MSB justified	32bit MSB justified	256fs	Figure 34
27	1			1	1	1	32bit I^2S Compatible		256fs	Figure 35

Table 25. Audio Interface Format (TDM256 Mode) (x: Don't care, N/A: Not Available)

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO (ADC)	SDTI (DAC)	BICK	Figure
	0	0	1	0	0	0	N/A			
	0			0	0	1	N/A			
28	0			0	1	0	24bit MSB justified	24bit MSB justified	128fs	Figure 37
29	0			0	1	1	24bit I^2S Compatible		128fs	Figure 38
30	0			1	0	0	24bit MSB justified	24bit LSB justified	128fs	Figure 39
31	0			1	0	1	32bit MSB justified	32bit LSB justified	128fs	Figure 39
32	0			1	1	0	32bit MSB justified	32bit MSB justified	128fs	Figure 37
33	0			1	1	1	32bit I^2S Compatible		128fs	Figure 38
	0			0	0	0	N/A			
	0			0	0	1	N/A			
34	0			0	1	0	24bit MSB justified	24bit MSB justified	128fs	Figure 37
35	0			0	1	1	24bit I^2S Compatible		128fs	Figure 38
36	0			1	0	0	24bit MSB justified	24bit LSB justified	128fs	Figure 39
37	0			1	0	1	32bit MSB justified	32bit LSB justified	128fs	Figure 39
38	0			1	1	0	32bit MSB justified	32bit MSB justified	128fs	Figure 37
39	0			1	1	1	32bit I^2S Compatible		128fs	Figure 38

Table 26. Audio Interface Format (TDM128 Mode) (N/A: Not available)

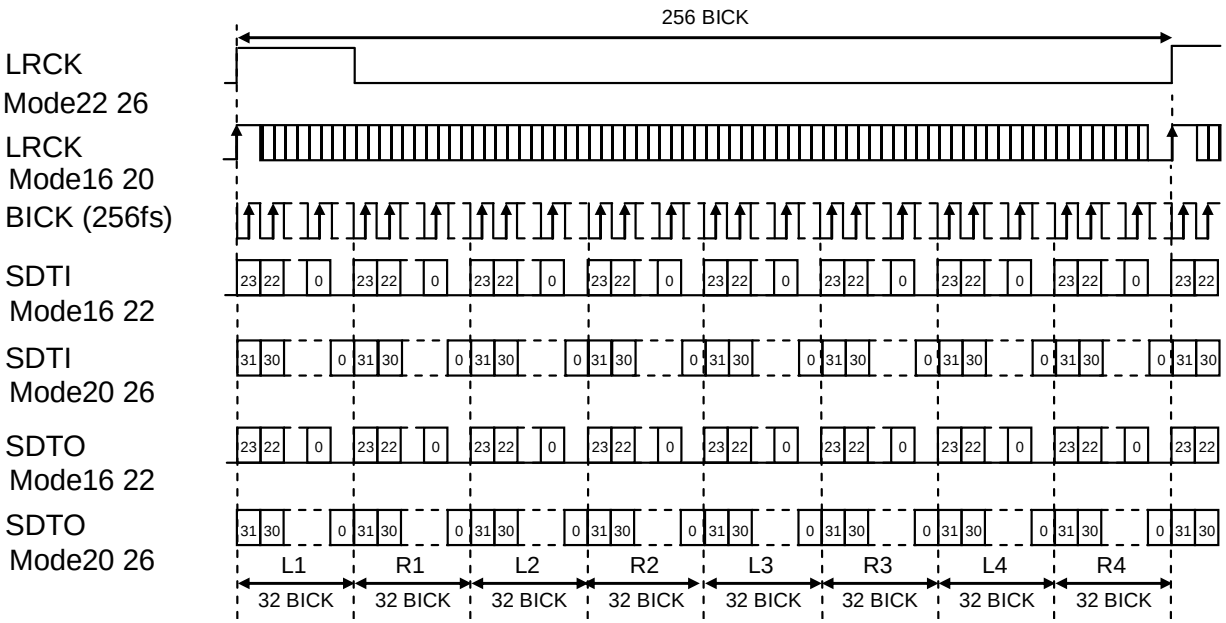


Figure 34. Mode 16/20/22/26 Timing (TDM256 mode, MSB justified)

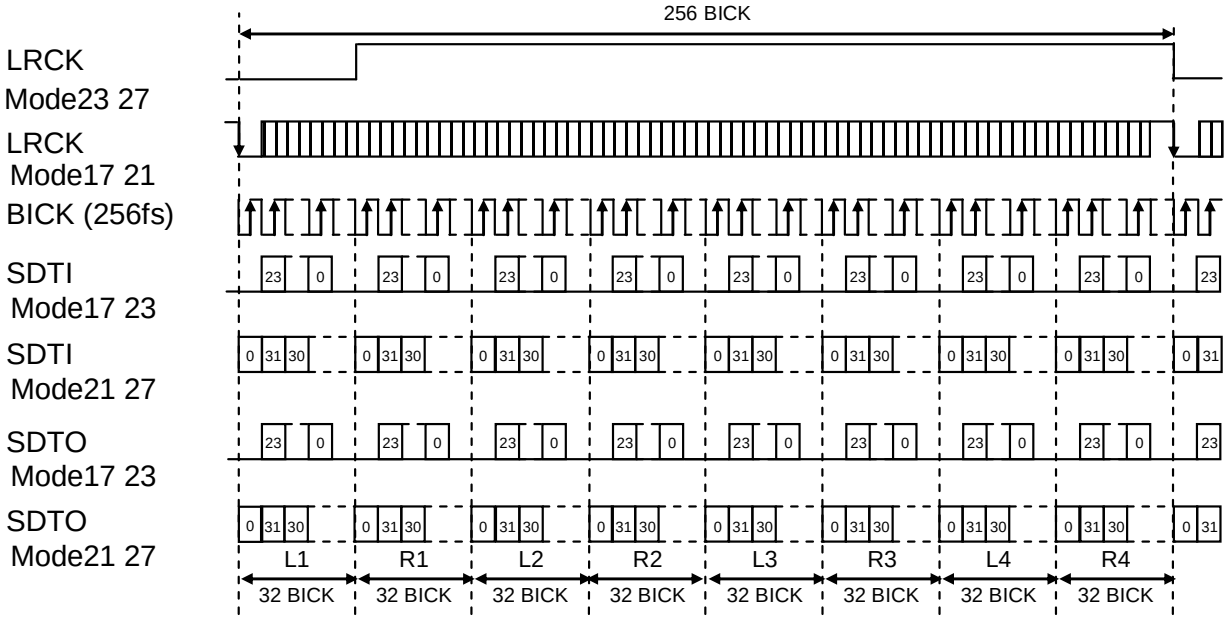


Figure 35. Mode 17/21/23/27 Timing (TDM256 mode, I^{2}S Compatible)

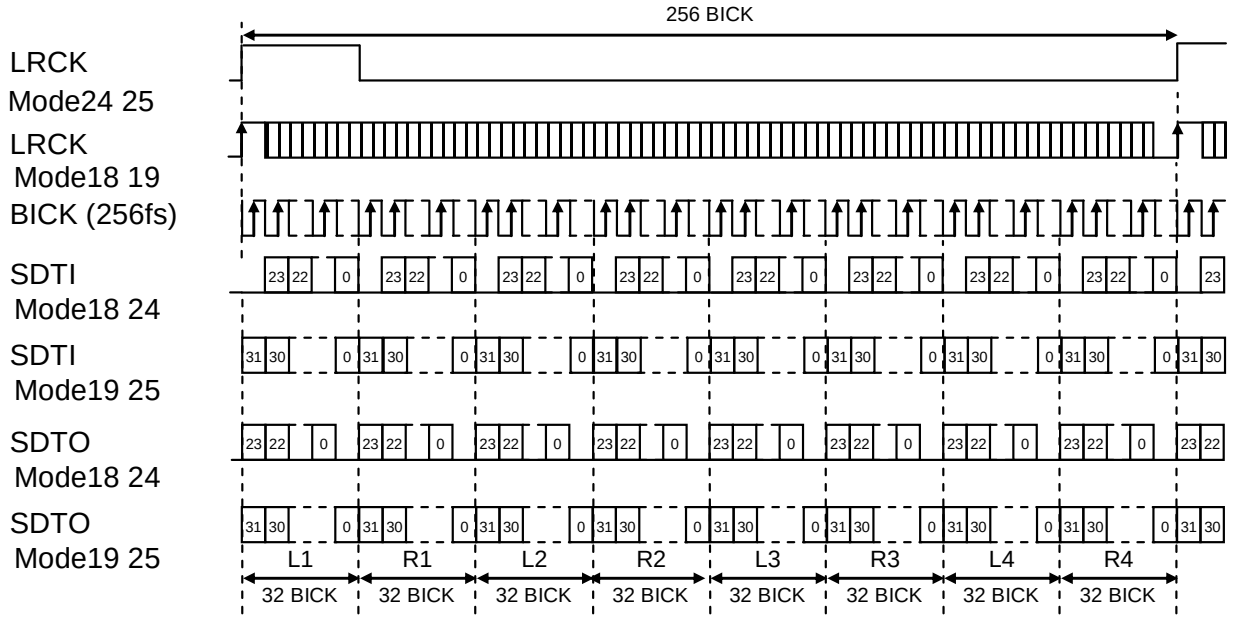


Figure 36. Mode 18/19/24/25 Timing (TDM256 mode, LSB justified)

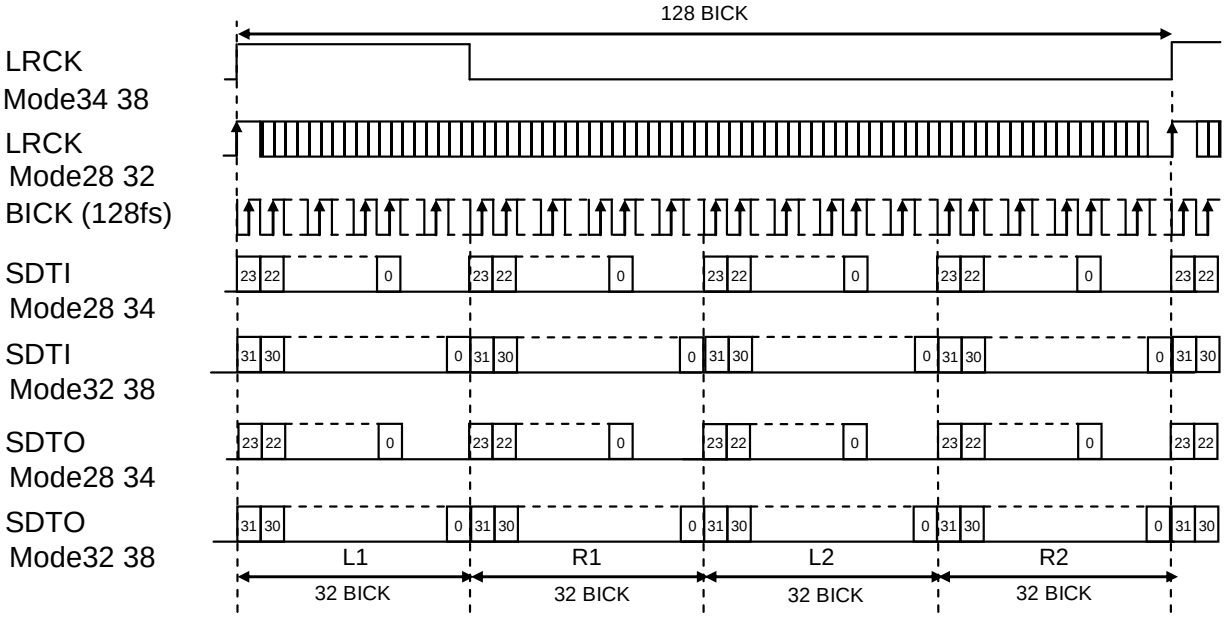


Figure 37. Mode 28/32/34/38 Timing (TDM128 mode, 24bit MSB justified)

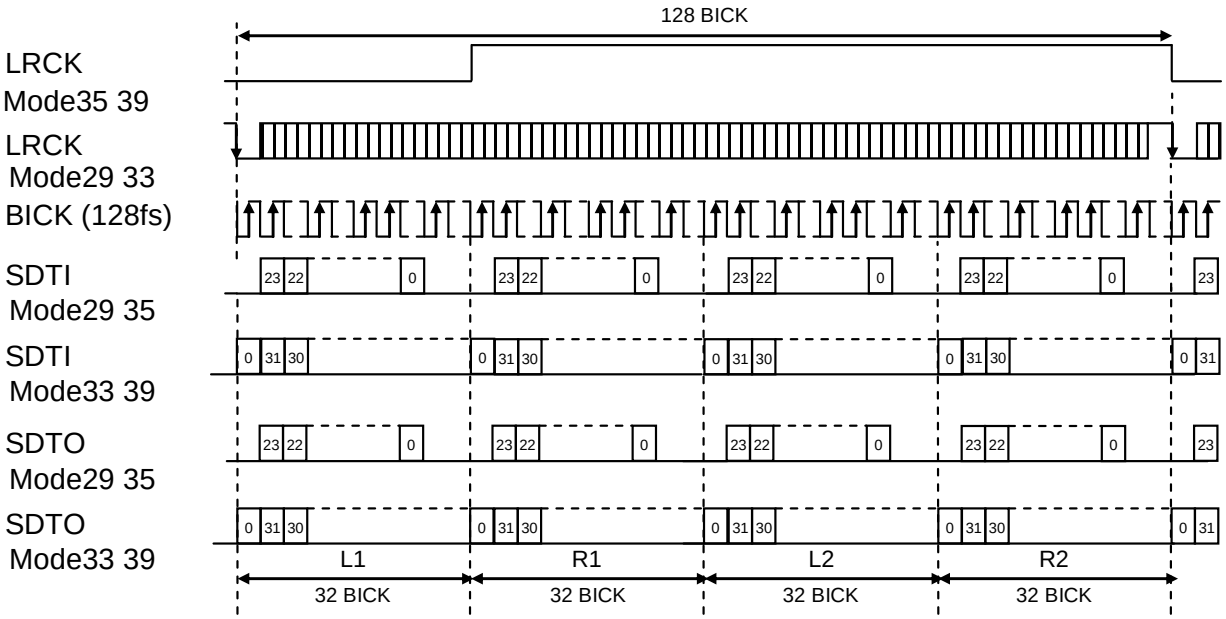


Figure 38. Mode 29/33/35/39 Timing (TDM128 mode, 24bit I^2S Compatible)

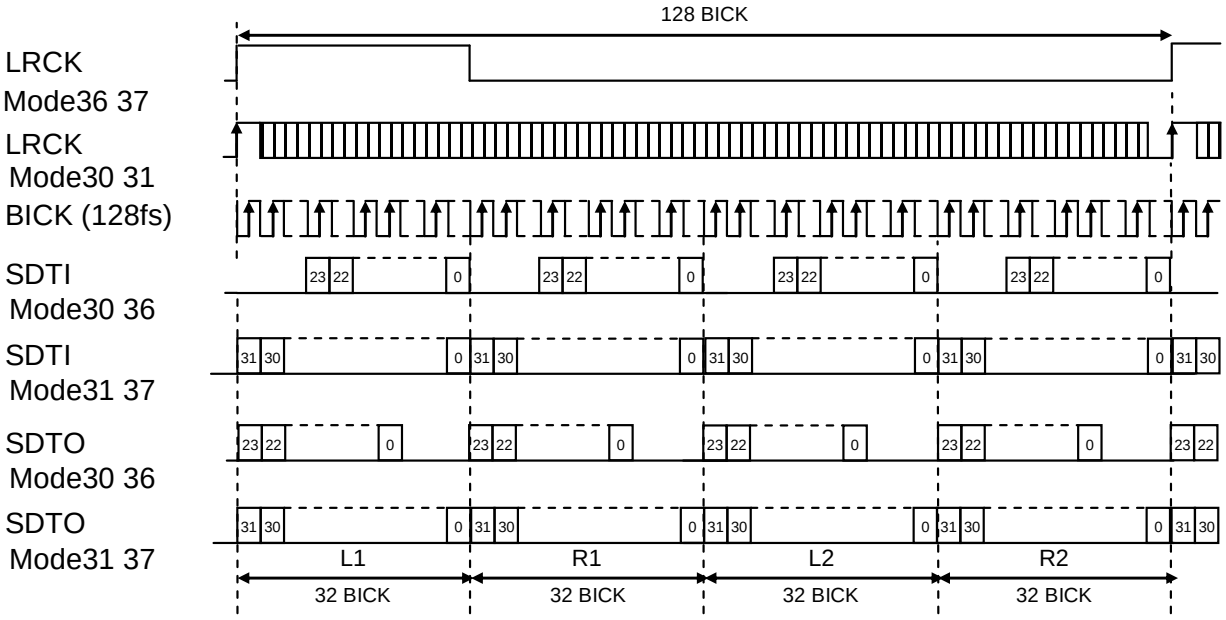


Figure 39. Mode 30/31/36/37 Timing (TDM128 mode, MSB/LSB justified)

■ ADC/DAC Digital Filter

The ADC has four kinds of digital filter modes. SDAD and SLAD bits select ADC digital filter mode. The default setting is SLAD bit = “0”, SDAD bit = “1” (Short delay Sharp Roll-Off Filter).

SLAD bit	SDAD bit	ADC Filter Mode Setting	
0	0	Sharp Roll-off Filter	
0	1	Short delay Sharp Roll-Off Filter	(default)
1	0	Slow Roll-off Filter	
1	1	Short delay Slow Roll-off Filter	

Table 27. ADC Digital Filter Setting

The DAC has five kinds of digital filter modes. SSLOW, SDDA and SLDA bits controls digital filter mode. When SSLOW bit = “1”, the setting of SDDA and SLDA bits is invalid. The default setting is SSLOW bit = SLDA bit = “0”, SDDA bit = “1” (Short delay Sharp Roll-Off Filter).

When SSLOW bit = “1”, DATT cannot be used. When the PS pin = “H”, DAC digital filter is set to Short delay Sharp Roll-Off Filter as default.

SSLOW bit	SLDA bit	SDDA bit	DAC Filter Mode Setting	
0	0	0	Sharp Roll-off Filter	
0	0	1	Short delay Sharp Roll-Off Filter	(default)
0	1	0	Slow Roll-off Filter	
0	1	1	Short delay Slow Roll-off Filter	
1	x		Super Slow Roll-Off Filter	

Table 28. DAC Digital Filter Setting (x: Don’t care)

■ Mono/Stereo Switching

When the PS pin = “L” (“H”), PMADL and PMADR bits(pins) set mono/stereo ADC operation. When changing ADC operation, PMADL and PMADR bits must be set “0” at first.

PMADL bit	PMADR bit	ADC Lch data	ADC Rch data	
0	0	All “0”	All “0”	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 29. Mono/Stereo Switching

■ Digital Attenuator

The AK4558 has a channel-independent digital attenuator (256 levels, 0.5dB steps). Attenuation level of the DAC can be set by ATL/R 7-0 bits (Table 30). Transition time between set values of ATL/R bits can be selected by ATS1-0 bits (Table 31). Transition between set values is the soft transition in Mode1/2/3 eliminating switching noise in the transition. Transition between set values is a soft transition of 4080 levels in Mode 0. It takes 4080/fs (85ms@fs=48kHz) from 00H to FFH. If the PDN pin goes to “L”, ATL/R 7-0 bit are initialized to FFH. These bits are also set to FFH when RSTN bit = “0”, and fade to their current value when RSTN bit returns to “1”.

ATL/R 7-0 bits	Attenuation Level	
FFH	0dB	(default)
FEH	−0.5dB	
FDH	−1.0dB	
FCH	−1.5dB	
:	:	
03H	−126.5dB	
01H	−127.0dB	
00H	MUTE (−∞)	

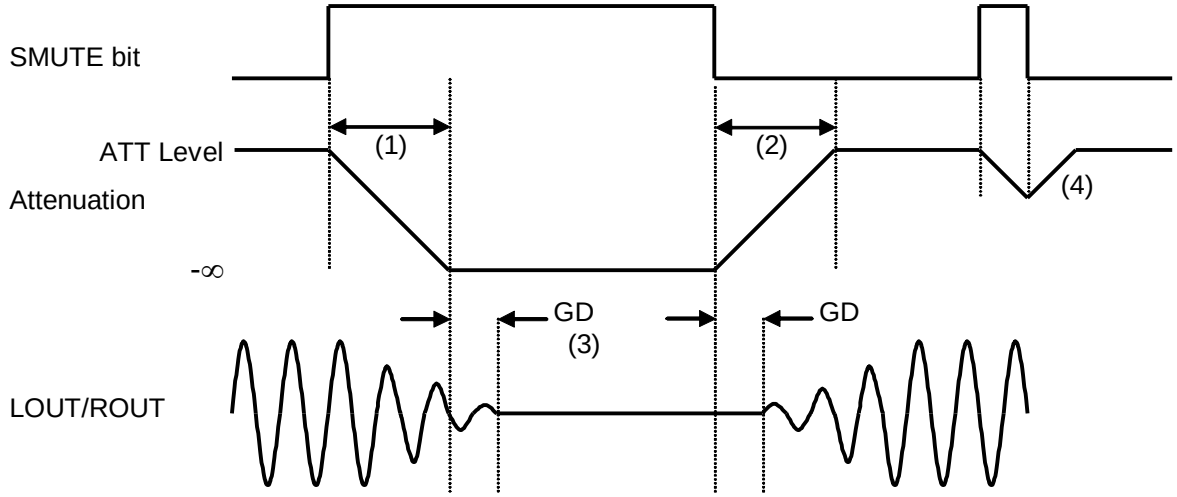
Table 30. Attenuation Level of Digital Attenuator

Mode	ATS1	ATS0	ATT speed	
0	0	0	4080/fs	(default)
1	0	1	2040/fs	
2	1	0	510/fs	
3	1	1	255/fs	

Table 31. Transition Time Setting of Digital Attenuator (ATS 1-0 bits)

■ Soft Mute Operation

Soft mute operation is performed in the digital domain. When SMUTEN bit is set “1”, the output signal is attenuated to -∞ in the cycle set by ATS bit (Table 31) from the current ATT level. When the SMUTEN bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to the ATT level in the cycle set by ATS bit. If the soft mute is cancelled before attenuating to -∞ after starting the operation, attenuation is discontinued and it is returned to ATT level by the same cycle. Soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) The time for input data attenuation to -∞ (Table 31). For example, this time is 4080LRCK cycles (4080/fs) at ATT_DATA=FFH. ATT transition of the soft-mute is from FFH to 00H

(2) The time for input data recovery to ATT level (Table 31). For example, this time is 4080LRCK cycles (4080/fs) at ATT-DATA=00H. ATT transition of soft-mute is from 00H to FFH.

(3) The analog output corresponding to the digital input has group delay (GD).

(4) If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returned to ATT level by the same cycle.

Figure 40. Soft Mute

■ Out of Band Noise Reduction Filter

The AK4558 has an out of band noise reduction filter that can change frequency response. This FIR filter attenuates out of band noise and prevents a degradation of the analog characteristics caused by a switching regulator, etc. FIRDA2-0 bits set the frequency for noise attenuation. (Table 32)

FIRDA2-0 bits	FIR filter Mode	FIR filter	
000	0	1/4*[1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0]	
001	1	1/4*[1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1]	(default)
010	2	1/4*[1 0 1 0 0 0 0 0 0 0 0 0 0 1 0 1]	
011	3	1/4*[1 0 0 1 0 0 0 0 0 0 0 0 1 0 0 1]	
100	4	1/4*[1 0 0 0 1 0 0 0 0 0 0 1 0 0 0 1]	
101	5	1/4*[1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1]	
110	6	1/4*[1 0 0 0 0 0 1 0 0 1 0 0 0 0 0 1]	
111	7	1/4*[1 0 0 0 0 0 0 1 1 0 0 0 0 0 0 1]	

Table 32. FIR Filter Setting

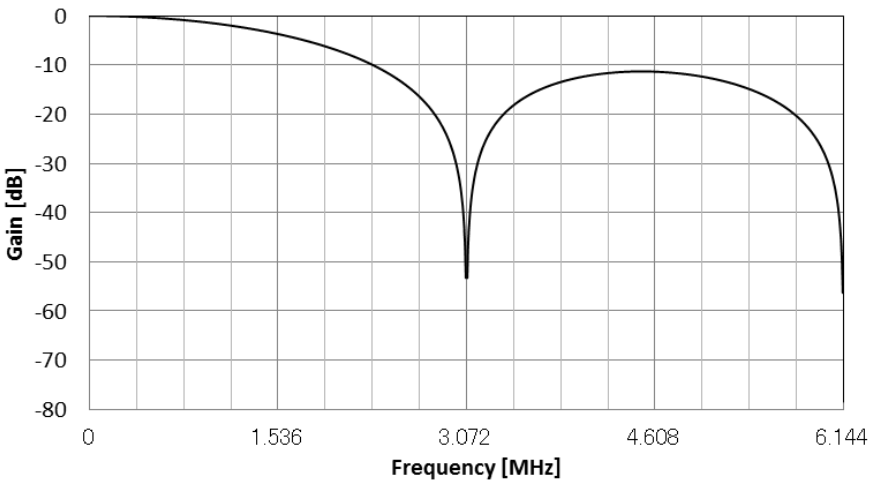


Figure 41. Mode0 FIR Filter

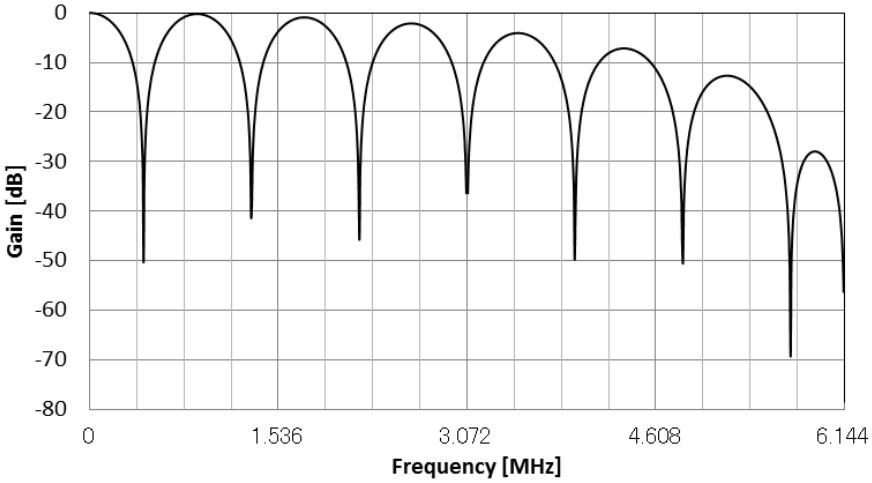


Figure 42. Mode1 FIR Filter

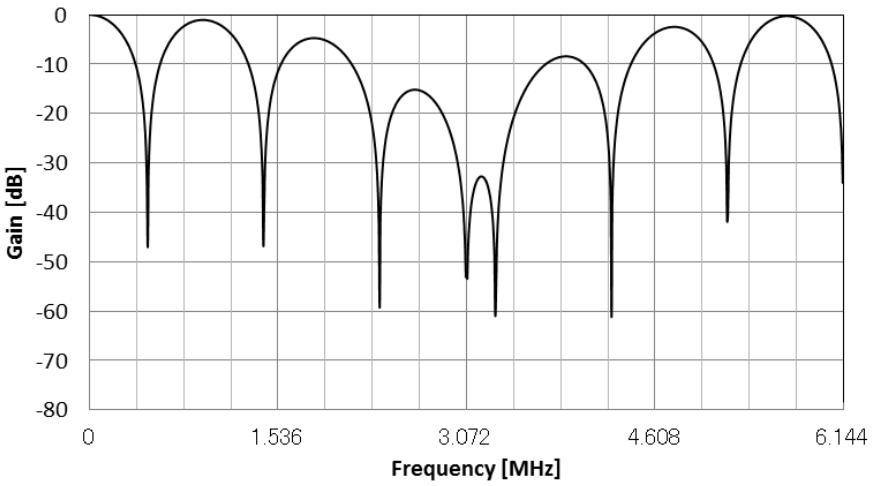


Figure 43. Mode2 FIR Filter

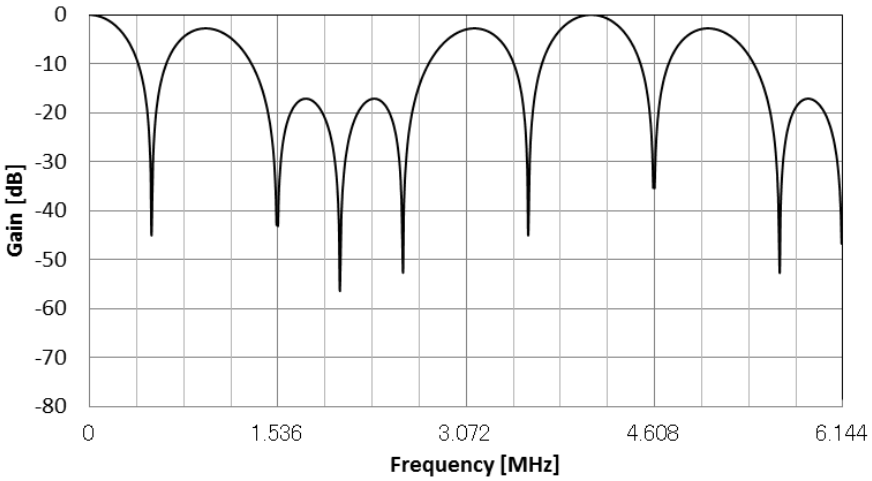


Figure 44. Mode3 FIR Filter

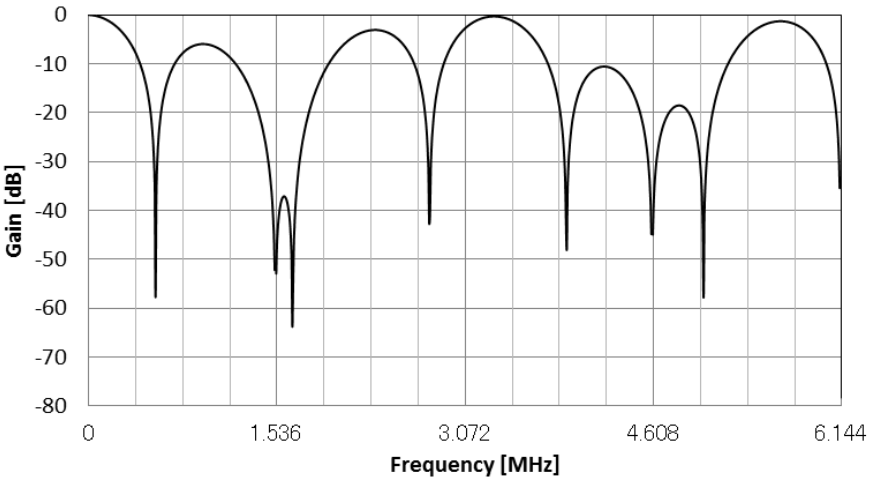


Figure 45. Mode4 FIR Filter

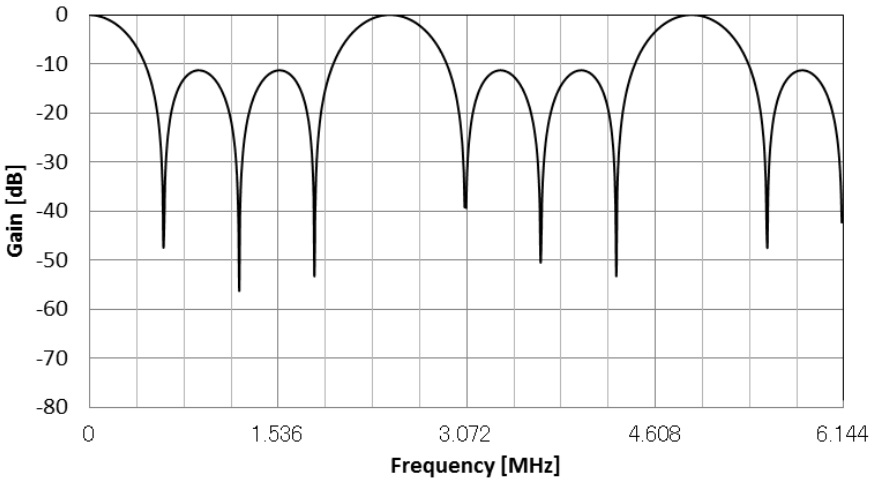


Figure 46. Mode5 FIR Filter

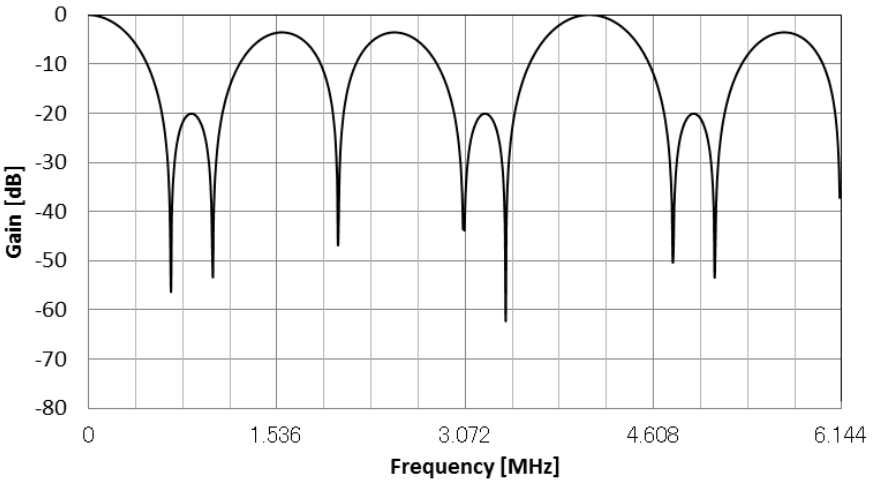


Figure 47. Mode6 FIR Filter

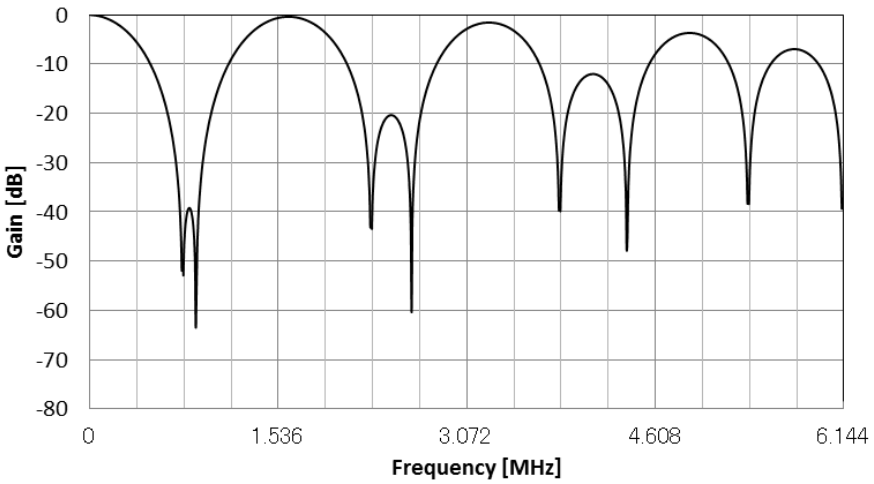


Figure 48. Mode7 FIR Filter

■ DAC Output (LOUT, ROUT pin)

1. When the PS pin = “L”(“H”), settings by registers(pins) shown below are valid.

LOUT and ROUT pins output VCOM voltage. The load impedance is 5kΩ (min.). When PMDAL/R bits = LOPS bit = “0”, the stereo line output enters power-down mode and the output is pulled-down to VSS1 by 100kΩ (typ). When the LOPS bit is “1”, stereo line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMDAL/R bits when LOPS bit = “0”. In this case, output signal line should be pulled-down by 20kΩ after AC coupled as Figure 49. Rise/Fall time is 300ms (max.) when C=1μF and R_L=10kΩ. When PMDAL/R bits = “1” and LOPS bit = “0”, the DAC output is in normal operation.

LOPS bit	PMDAL	Mode	LOUT pin	
0	0	Power-down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS1	
	1	Power-save	Rise up to VCOM	

Table 33. Lch DAC Output Mode Setting

LOPS bit	PMDAR	Mode	ROUT pin	
0	0	Power-down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS1	
	1	Power-save	Rise up to VCOM	

Table 34. Rch DAC Output Mode Setting

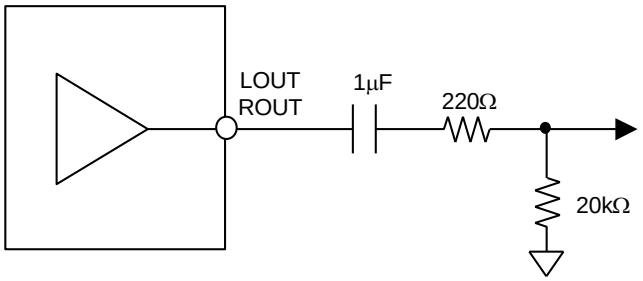


Figure 49. External Circuit of DAC Output (in case of using a Pop Noise Reduction Circuit)

[DAC Output Control Sequence (in case of using a Pop Noise Reduction Circuit)]

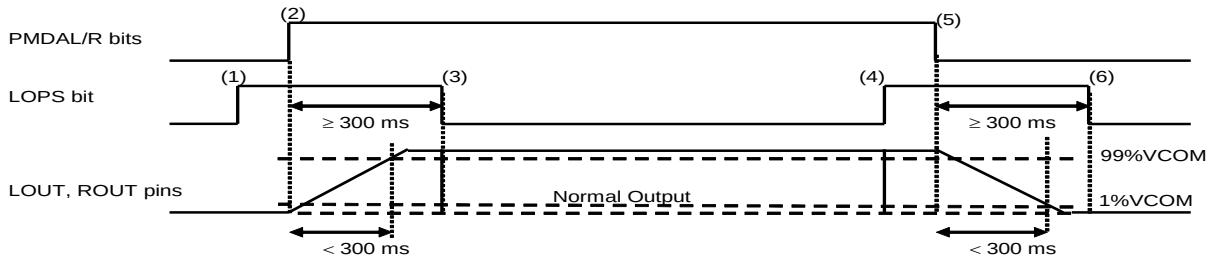


Figure 50. DAC Output Control Sequence (in case of using a Pop Noise Reduction Circuit)

(1) Set LOPS bit = "1". DAC output enters power-save mode.
(2) Set PMDAL/R bits = "1". DAC output exits power-down mode.
LOUT and ROUT pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) when C=1μF.
(3) Set LOPS bit = "0" after LOUT and ROUT pins rise up. Stereo line output exits power-save mode. Stereo line output is enabled.
(4) Set LOPS bit = "1". Stereo line output enters power-save mode.
(5) Set PMDAL/R bits = "0". Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to 1% of the common voltage. Fall time is 200ms (max 300ms) at C=1μF.
(6) Set LOPS bit = "0" after LOUT and ROUT pins fall down. Stereo line output exits power-save mode.

2. When the PS pin = "H", settings shown below are valid.

LOUT and ROUT pins output VCOM voltage. The load impedance is 5kΩ (min.). When PMDAL/R pins = LOPS pin = "L", the stereo line output enters power-down mode and the output is pulled-down to VSS1 by 100kΩ (typ). When the LOPS pin is "H", stereo line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMDAL/R pins. In this case, output signal line should be pulled-down by 20kΩ after AC coupled as Figure 51. Rise/Fall time is 300ms (max.) when C=1μF and R_L=10kΩ. When PMDAL/R pins = "H" and LOPS pin = "L", the stereo lineout is in normal operation.

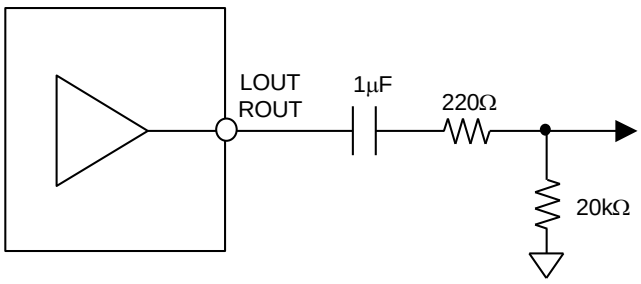


Figure 51. External Circuit of DAC Output (in case of using a Pop Noise Reduction Circuit)

[DAC Output Control Sequence (in case of using a Pop Noise Reduction Circuit)]

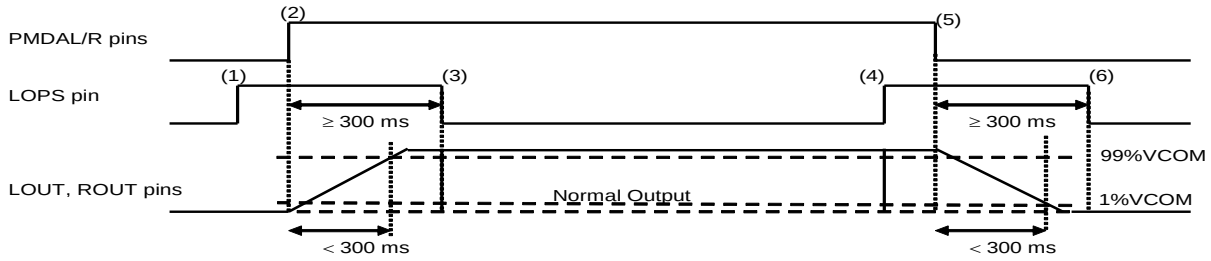


Figure 52. DAC Output Control Sequence (in case of using a Pop Noise Reduction Circuit)

(1) Set LOPS pin = “H”. DAC output enters power-save mode.
(2) Set PMDAL/R pin = “H”. DAC output exits power-down mode.
LOUT and ROUT pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) when C=1μF.
(3) Set LOPS pin = “L” after LOUT and ROUT pins rise up. Stereo line output exits power-save mode. Stereo line output is enabled.
(4) Set LOPS pin = “H”. Stereo line output enters power-save mode.
(5) Set PMDAL/R pin = “L”. Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to 1% of the common voltage. Fall time is 200ms (max 300ms) at C=1μF.
(6) Set LOPS pin = “L” after LOUT and ROUT pins fall down. Stereo line output exits power-save mode.

■ Control Sequence

1. Clock Set Up

When the AK4558 is in operation, the clocks must be supplied.

1-1. PLL Master Mode(PS pin= "L", CKS3-2 pins = "H H")

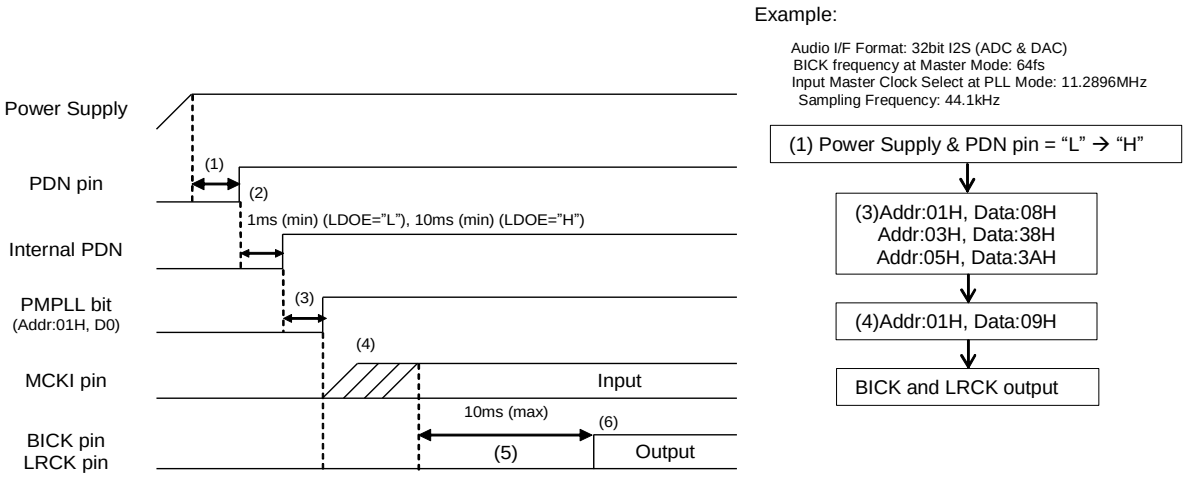


Figure 53. Clock Set Up Sequence (1)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4558.

(2) Control register settings become available in 10ms (min.) when LDOE pin = "H", or 1ms (min.) when LDOE pin = "L", after the PDN pin "L" → "H".

(3) DIF2-0, PLL3-0, FS3-0 and BCKO1-0 bits must be set during this period.

(4) PLL starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source. PLL lock time is 10ms (max). In this period, the AK4558 outputs BICK and LRCK as it is in EXT, Master mode if a clock is supplied to the MCKI pin during the period (3).

(5) The AK4558 starts outputting the LRCK and BICK clocks after the PLL became stable. Then normal operation starts.

1-2. PLL Slave Mode with External Clock (BICK pin, LRCK pin)
(PS pin= "L", CKS3-2 pins = "L L" or "L H" or "H L")

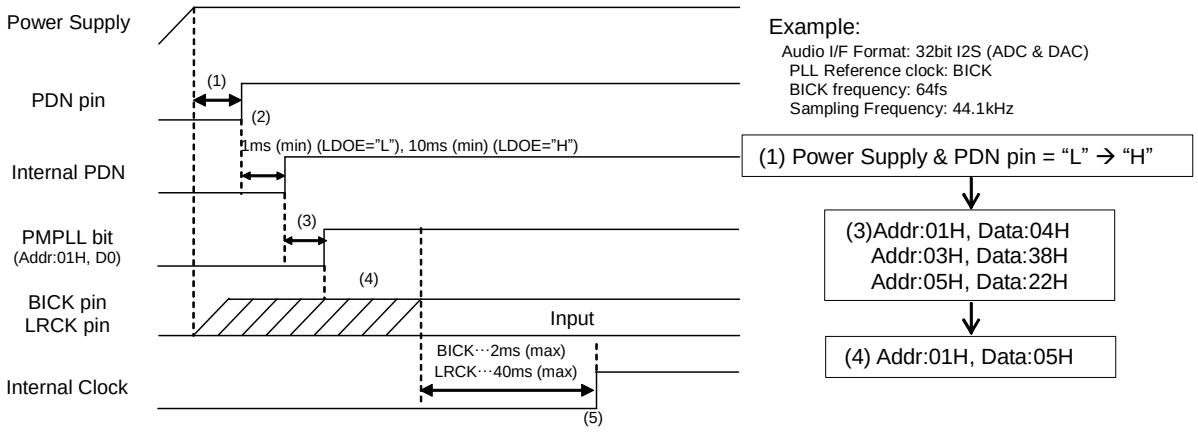


Figure 54. Clock Set Up Sequence (2)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4558.

(2) Control register settings become available in 10ms (min.) when LDOE pin = "H", or 1ms (min.) when LDOE pin = "L", after the PDN pin "L" → "H". The power-up time of VCOM will be 2ms (max.) after the PDN pin "L" → "H" if the external capacitor is 1μF±50%.

(3) DIF2-0, PLL3-0, FS3-0 and BCKO1-0 bits must be set during this period.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (BICK or LRCK pin) is supplied. PLL lock time is 2ms (max) when BICK is a PLL reference clock. PLL lock time is 40ms (max) when LRCK is a PLL reference clock.

(5) Normal operation starts after that the PLL is locked.

1-3. External Clock Mode (Slave Mode)
(CKS3-2 pins = “L L” or “L H” or “H L”)

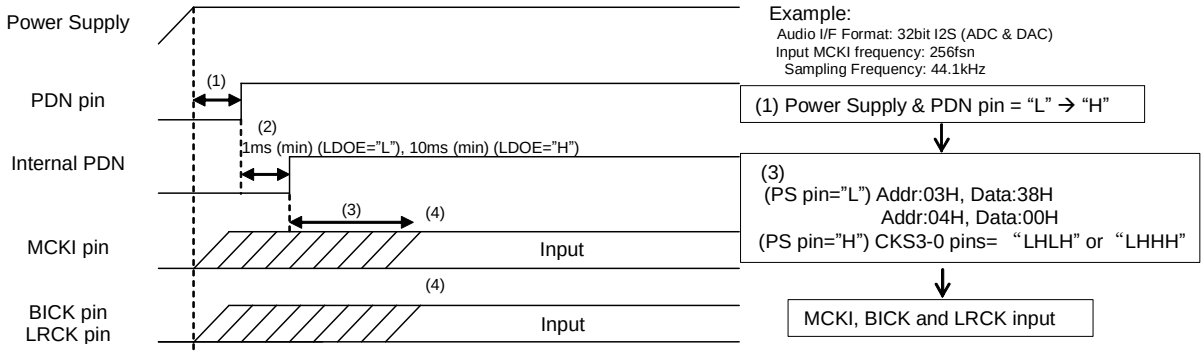


Figure 55. Clock Set Up Sequence (3)

<Sequence>

(1) After Power Up: PDN pin “L” → “H”
“L” time of 150ns or more is needed to reset the AK4558.

(2) Control register settings become available in 10ms (min.) when LDOE pin = “H”, or 1ms (min.) when LDOE pin = “L”, after the PDN pin “L” → “H”. The power-up time of VCOM will be 2ms (max.) after the PDN pin “L” → “H” if the external capacitor is 1μF±50%.

(3) DIF2-0, DFS1-0 and ACKS bits must be set during this period.

(4) Normal operation starts after MCKI, LRCK and BICK are supplied.

1-4. External Clock Mode (Master Mode)
(CKS3-2 pins = “HH”)

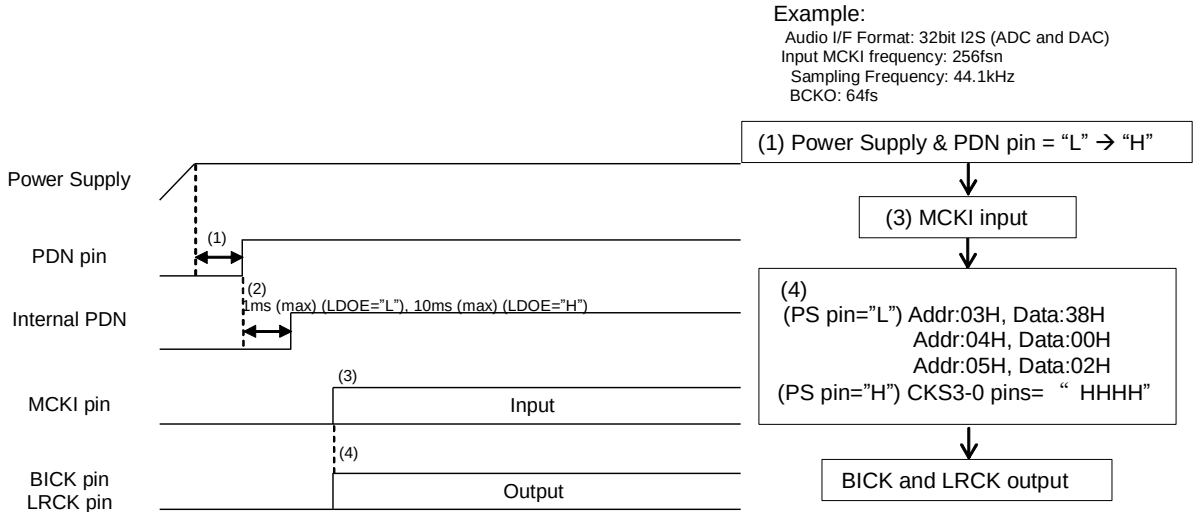


Figure 56. Clock Set Up Sequence (4)

<Sequence>

(1) After Power Up: PDN pin “L” → “H”
“L” time of 150ns or more is needed to reset the AK4558.

(2) Control register settings become available in 10ms (1ms)(min.) when LDOE pin= “H”(“L”) after the PDN pin “L” → “H”. The power-up time of VCOM will be 2ms (max.) after the PDN pin “L” → “H” if the external capacitor is 1μF±50%.

(3) Input MCKI.

(4) When PS pin = “L”, set DIF2-0, DFS1-0 MCKS1-0 and BCKO1-0 bits. When PS pin = “H”, set CKS pin. The AK4558 starts outputting LRCK and BICK.

2. ADC Output

2-1. PS pin = "L"

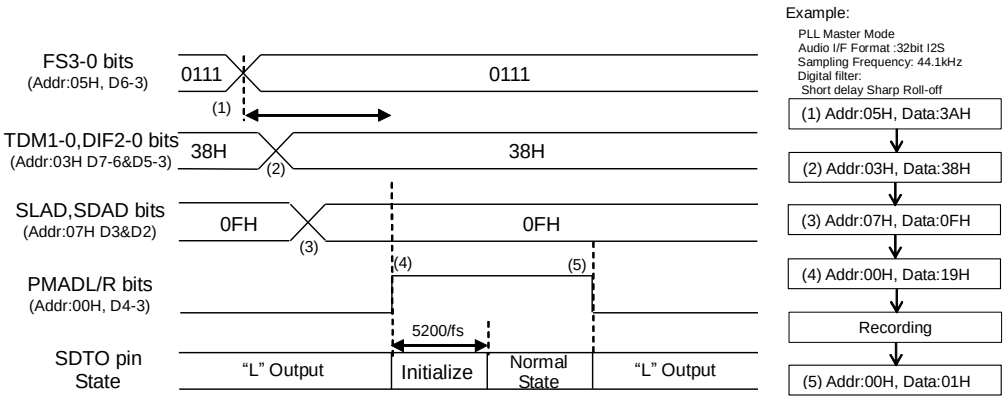


Figure 57. ADC Output Sequence (PS pin = "L")

<Sequence>
In the case of fs=44.1kHz
At first, clocks should be supplied according to "Serial Mode".
(1) Set up the sampling frequency (FS3-0 bits). The ADC must be powered-up in consideration of PLL lock time.
(2) Set up the audio format (Addr=03H).
(3) Set up the de-emphasis filter (Addr = 07H).
(4) Power up the ADC: PMADL = PMADR bits = "0" → "1"
Initialization cycle of the ADC is 5200/fs @Normal mode. The SDTO pin outputs "L" during initialization.
(5) Power down ADC: PMADL = PMADR bits = "1" → "0"

2-2. PS pin = "H"

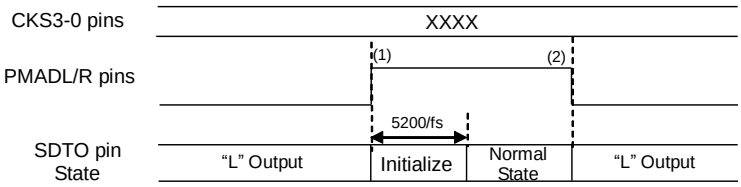


Figure 58.ADC Output Sequence (PS pin ="H")

<Sequence>
At first, operation mode should be set by CKS3-0 bits according to "Parallel Mode".
(1) Power up the ADC: PMADL pin = PMADR pin = "L" → "H"
Initialization cycle of the ADC is 5200/fs @Normal mode. The SDTO pin outputs "L" during initialization.
(2) Power down ADC: PMADL pin = PMADR pin = "H" → "L"

3. DAC Output

3-1. PS pin = “L”

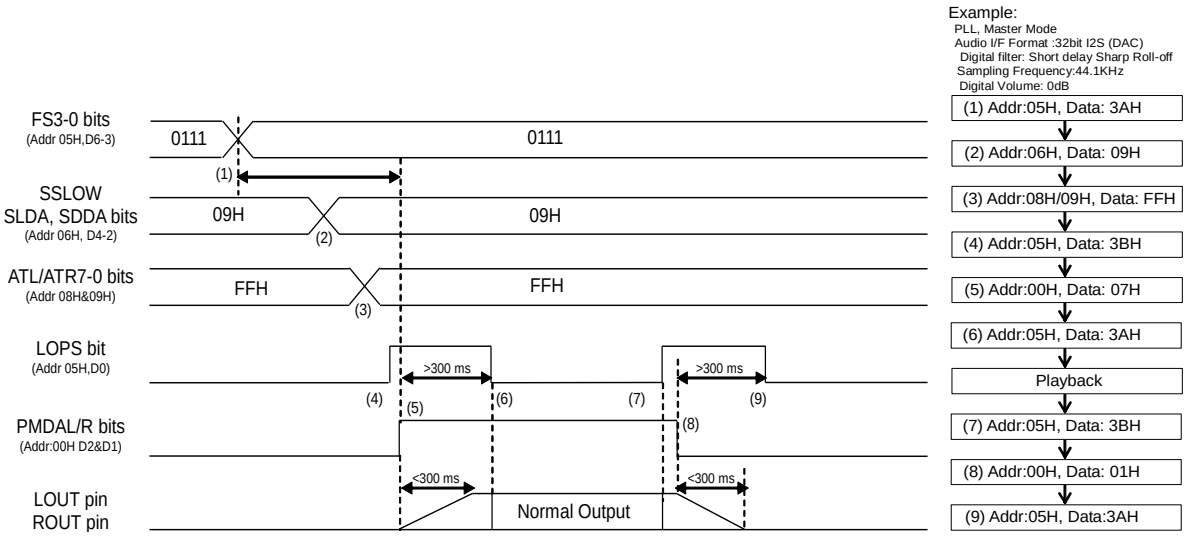


Figure 59. DAC Sequence (PS pin =”L”)

<Sequence>

Following is the example when fs=44.1k.

At first, clocks should be supplied according to “Clock Set Up” sequence.

(1) Set up the sampling frequency (FS3-0 bits). The DAC must be powered-up in consideration of PLL lock time.

(2) Set up the digital filter mode.

(3) Set up the digital output volume (Address = 08H, 09H).

(4) Set the DAC output to power-save mode: LOPS bit “0” → “1”

(5) Power up the DAC: PMDAL = PMDAR bits = “0” → “1”

Outputs of the LOUT and ROUT pins start rising. Rise time is 300ms (max.) when C = 1µF.

(6) Release power-save mode of the DAC output: LOPS bit = “1” → “0”

Set LOPS bit to “0” after the LOUT and ROUT pins output “H”. Sound data will be output from the LOUT and ROUT pins after this setting.

(7) Set the DAC output power-save mode: LOPS bit = “0” → “1”

(8) Power down the DAC: PMDAL = PMDAR bits = “1” → “0”

Outputs of the LOUT and ROUT pins start falling. Fall time is 300ms (max.) when C = 1µF.

(9) Release power-save mode of the DAC output: LOPS bit = “1” → “0”

Set LOPS bit to “0” after outputs of the LOUT and ROUT pins fall to “L”.

3-2. PS pin = “H”

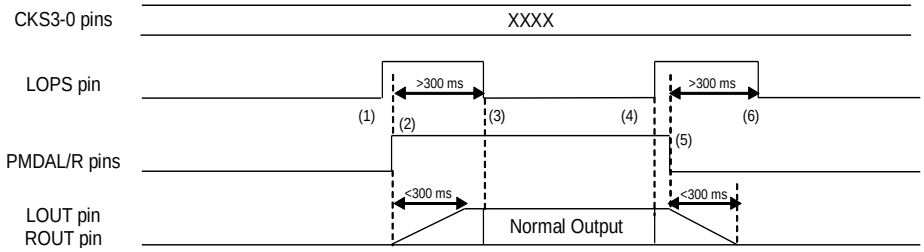


Figure 60. DAC Sequence (PS pin = “H”)

<Sequence>
At first, set operation mode by the CKS3-0 pins according to “Parallel Control Mode”.
In parallel mode, digital filter setting is Short delay Sharp Roll-Off Filter mode. Digital filter does not correspond to PLL and TDM mode.
(1) Set the DAC output to power-save mode: LOPS pin “L” → “H”
(2) Power up the DAC: PMDAL = PMDAR pins = “L” → “H”
Outputs of the LOUT and ROUT pins start rising. Rise time is 300ms (max.) when C = 1µF.
(3) Release power-save mode of the DAC output (LOPS pin = “H” → “L”) after the LOUT and the ROUT pins are risen up. Then data output is started from the LOUT and the ROUT pins.
(4) Set the DAC output to power-save mode: LOPS pin “L” → “H”
(5) Power down the DAC: PMDAL = PMDAR pins = “H” → “L”
Outputs of the LOUT and the ROUT pins go to low. The maximum fall time is 300 ms when C = 1 uF.
(6) Release power-save mode of the DAC output: LOPS pin = “H” → “L”
Set LOPS pin to “L” after output of the LOUT and ROUT pins fall to “L”.

4. Reset Function

When RSTN bit= “0” analog and digital blocks of the ADC are powered-down and digital block of DAC is powered-down, but the internal register are not initialized. The analog outputs go to VCOM voltage, and SDTO pin outputs “L”.

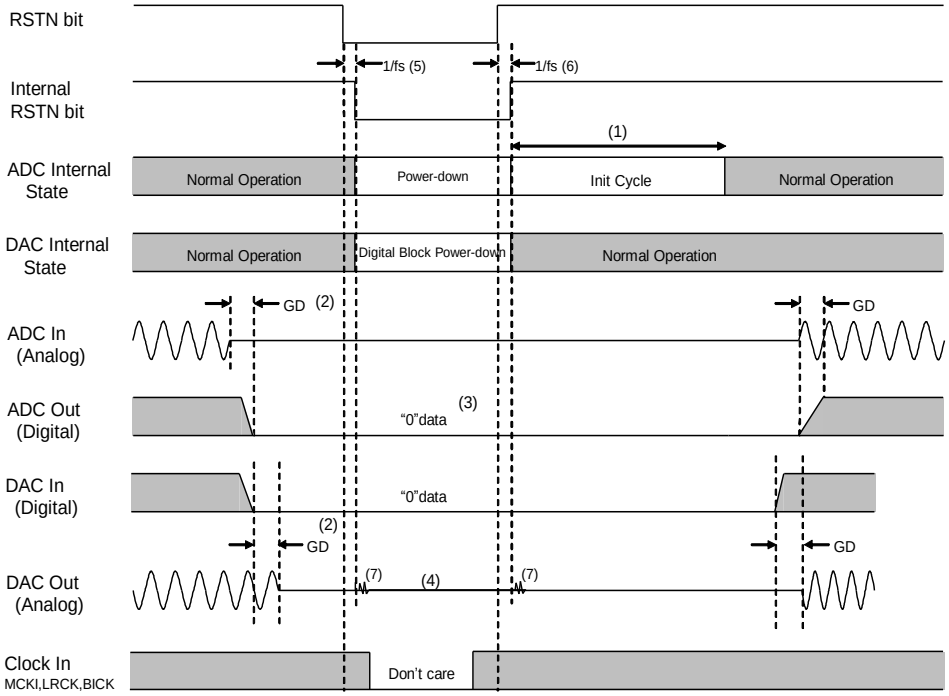


Figure 61. Reset Sequence

Note:

(1) The analog section of the ADC is initialized after exiting reset state.
The initializing cycle is 5200fs in Normal Speed Mode (DFS1-0 bits = “00”), 10000fs in Double Speed Mode (DFS1-0 bits = “01”) and 19200fs in Quad Speed Mode (DFS1-0 bits “10”). In this period, the ADC input voltage should be operating common voltage.

(2) Digital output corresponding to the analog inputs, and analog outputs corresponding to the digital inputs have group delay (GD).

(3) The ADC output is “0” data at power-down state.

(4) The DAC output is VCOM voltage at power-down state.

(5) There is a delay, 1/fs from writing RSTN bit = “0” to set the internal RSTN bit = “0”.

(6) There is a delay, 1/fs from writing RSTN bit = “1” to start an initialization cycle.

(7) Click noise occurs at the edges (“↑ ↓”) of the internal timing of RSTN. This noise is output even if “0” data is input. Mute the analog output externally if the click noise (7) adversely affect system performance.

5. Stop of Clock

Necessary clocks must be supplied when the AK4558 is in operation.

1. PLL Master Mode

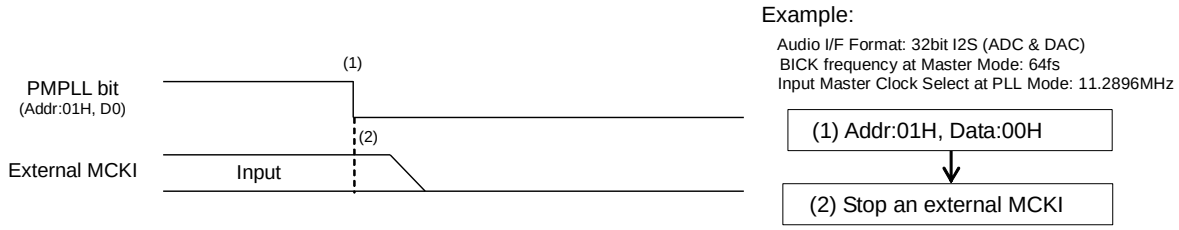


Figure 62. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop an external master clock.

2. PLL Slave Mode (BICK, LRCK pin)

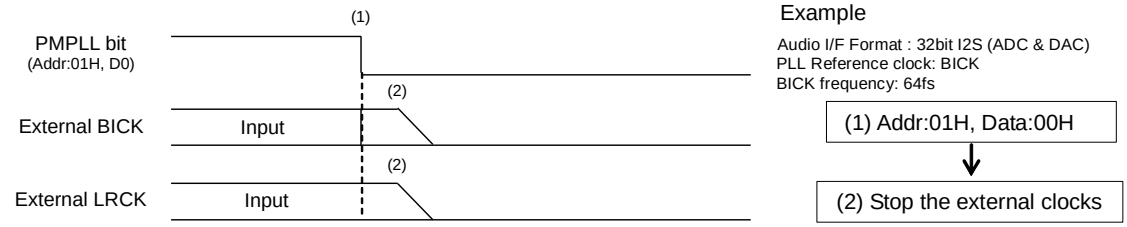


Figure 63. Clock Stopping Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external BICK and LRCK clocks

3. EXT Slave Mode

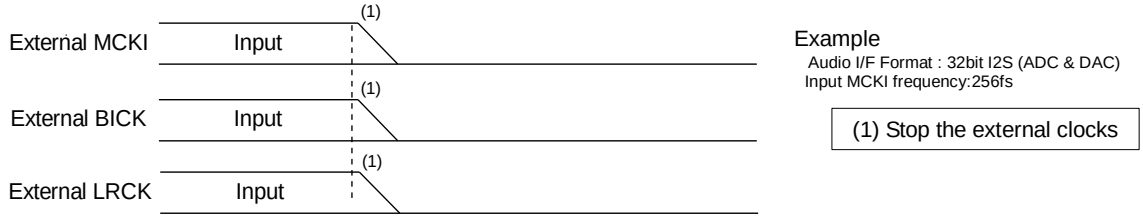


Figure 64. Clock Stopping Sequence (3)

<Example>
(1) Stop the external MCKI, BICK and LRCK clocks.

4. EXT Master Mode

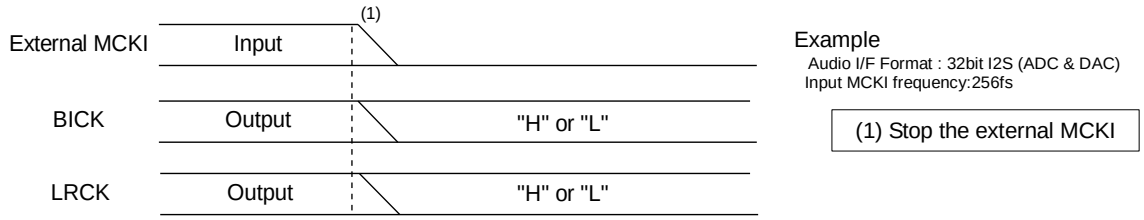


Figure 65. Clock Stopping Sequence (4)

<Example>

(1) Stop MCKI clock. BICK and LRCK are fixed to “H” or “L”.

6. System Reset

The AK4558 should be reset once by bringing the PDN pin to “L” upon power-up. Reference voltage such as VCOM is powered up by the PDN pin, and the internal timing starts as the internal circuit is powered up on MCKI and LRCK rising edge “↑”. The ADC and DAC blocks are in power down state until MCKI, LRCK and BICK are input.

7. Power down

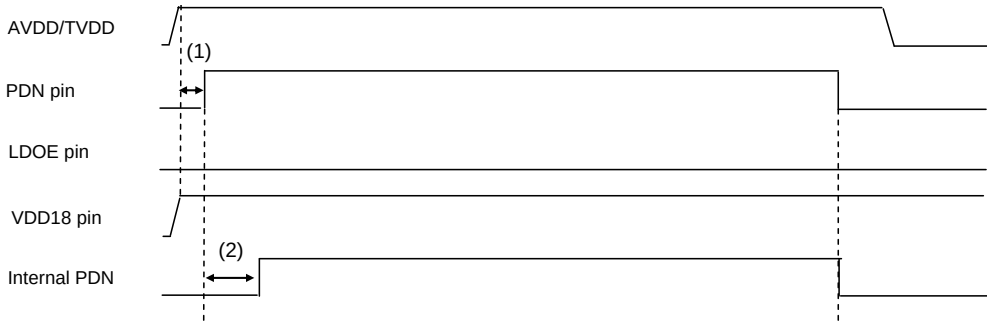


Figure 66. Power Down Sequence (LDOE pin= “L”)

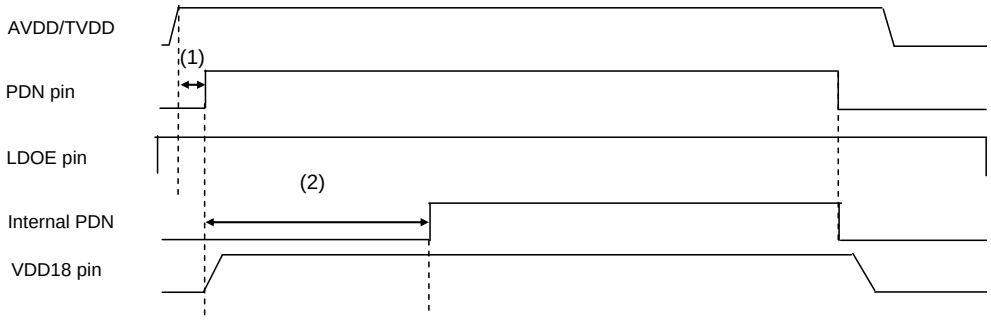


Figure 67. Power Down Sequence (LDOE pin= “H”)

Note:

(1) The PDN pin must be held to “L” for 150 ns after power up AVDD and TVDD.

(2) When the LDOE pin = “L”, the internal shutdown switch is ON after power up the AK4558. Internal circuit will be powered up after the shutdown switch is ON (1 ms max.). When the LDOE pin = “H”, the internal LDO is powered up after the AK4558 is powered up. The internal circuit will be powered up (10 ms max.) after the shutdown switch is ON following internal oscillator count-up.
During this period, digital output and digital in/output pins may output an instantaneous pulse (max. 1us). Therefore, referring the output of digital pins and data transmission with a device on the same 3-wire serial/I^2C bus as the AK4558 should be avoided in this period to prevent system errors.

■ Serial Control Interface

I²C-bus Control Mode (PS pin = "L")

Functions of the AK4558 are controlled by registers or pins. The register writing is executed via I²C bus. The chip address is determined by the state of the CAD0 and CAD1 inputs. Setting the PDN pin = "L" initializes the registers to their default values. Writing "0" to the RSTN bit can initialize the internal timing circuit, but the register values will not be initialized.

* A control register writing is not available when the PDN pin = "L".

The AK4558 supports the fast-mode I²C-bus (max: 400kHz). Pull-up resistors at the SDA and SCL pins must be connected to the voltage that is equal to or less than (TVDD+03)V.

1. WRITE Operations

Figure 68 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 74). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1 and CAD0 (device address bit). These bits identify the specific device on the bus. The hard-wired input pins (CAD1 and CAD0) set these device address bits (Figure 69). If the slave address matches that of the AK4558, the AK4558 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 75). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4558. The format is MSB first, and those most significant 1bit is fixed to zero (Figure 70). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 71). The AK4558 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 74).

The AK4558 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4558 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds "09H" prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 76) except for the START and STOP conditions.

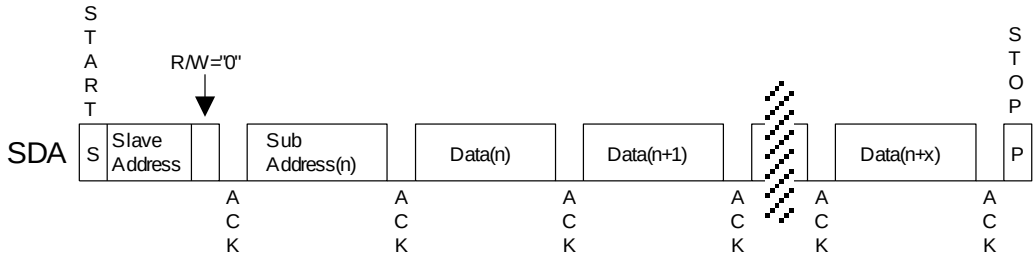


Figure 68. Data Transfer Sequence in I²C Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

Figure 69. The First Byte (CAD1 and CAD0 are set by pin settings)

0	0	0	A4	A3	A2	A1	A0

Figure 70. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 71. Byte Structure after The Second Byte

1. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4558. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 09H prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK4558 supports two basic read operations: Current Address Read and Random Address Read.

2-1. Current Address Read

The AK4558 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next Current Read operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4558 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4558 ceases the transmission.

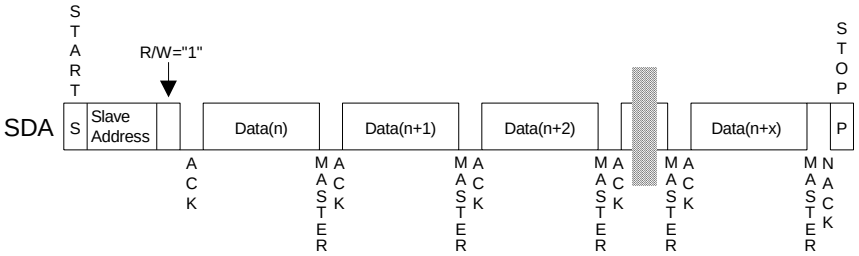


Figure 72. Current Address Read

2-2. Random Address Read

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4558 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4558 ceases the transmission.

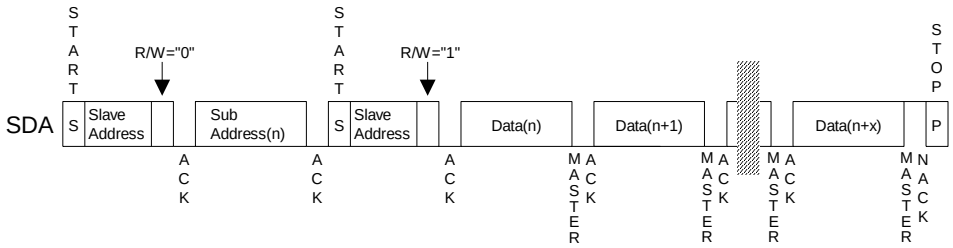


Figure 73. Random Address Read

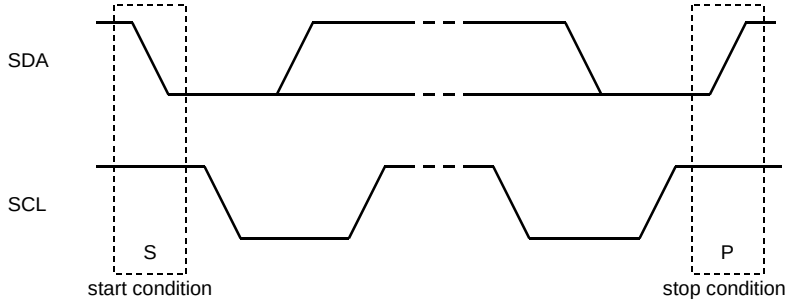


Figure 74. Start Condition and Stop Condition

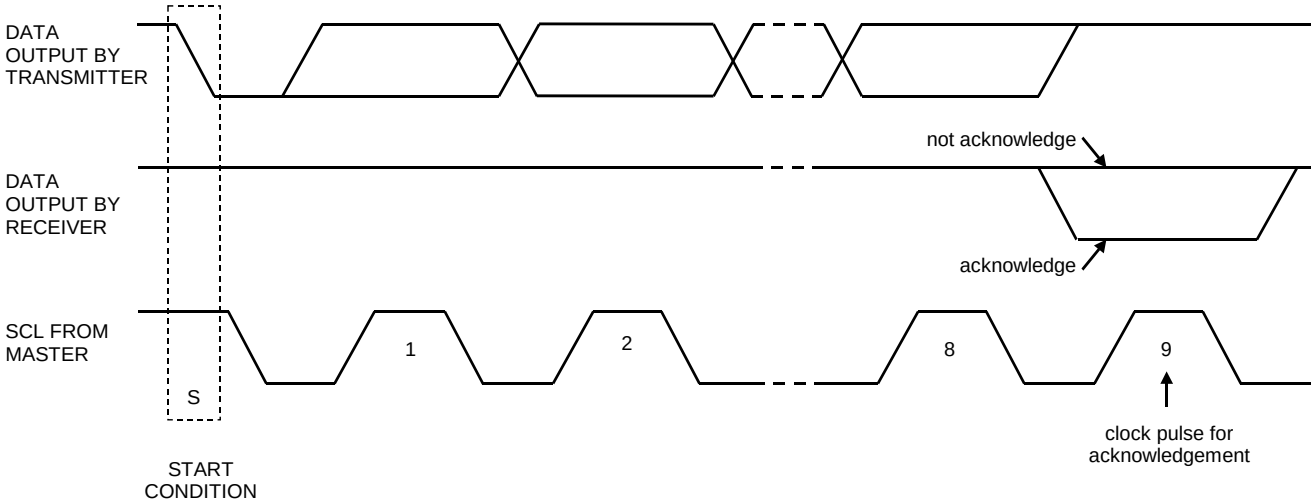


Figure 75. Acknowledge (I^2C Bus)

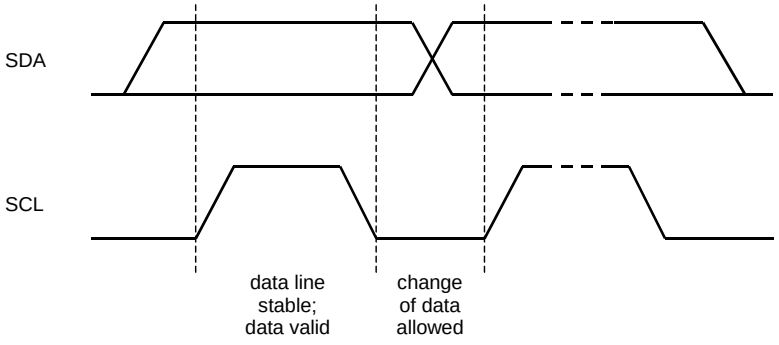


Figure 76. Bit Transfer (I^2C Bus)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	0	PMADR	PMADL	PMDAR	PMDAL	RSTN
01H	PLL Control	0	0	0	PLL3	PLL2	PLL1	PLL0	PMPLL
02H	DAC TDM	0	0	0	0	0	0	SDS1	SDS0
03H	Control 1	TDM1	TDM0	DIF2	DIF1	DIF0	ATS1	ATS0	SMUTE
04H	Control 2	0	0	0	MCKS1	MCKS0	DFS1	DFS0	ACKS
05H	Mode Control	0	FS3	FS2	FS1	FS0	BCKO1	BCKO0	LOPS
06H	Filter setting	FIRDA2	FIRDA1	FIRDA0	SLDA	SDDA	SSLOW	DEM1	DEM0
07H	HPF Enable, Filter setting	0	0	0	0	SLAD	SDAD	HPFER	HPFEL
08H	LOUT Volume Control	ATL7	ATL6	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
09H	ROUT Volume Control	ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

Note 42. Address 0AH and 1FH are a read only register. The bits defined as 0 must contain a “0” value. When the PDN pin goes to “L”, the registers are initialized to their default values. When RSTN bit goes to “0”, the internal timing is reset, but registers are not initialized to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	0	PMADR	PMADL	PMDAR	PMDAL	RSTN
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

RSTN: Internal Timing Reset
0: Reset Register values are not reset.
1: Normal Operation (default)

PMDAL/R: DAC L/Rch Power Management
0: DAC L/Rch Power Down (default)
1: Normal Operation

PMADL/R: ADC L/Rch Power Management
0: ADC L/Rch Power Down (default)
1: Normal Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	PLL Control	0	0	0	PLL3	PLL2	PLL1	PLL0	PMPLL
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	0

PMPLL: PLL Power Management
0: EXT Mode and Power down (default)
1: PLL Mode and Power up

PLL3-0: PLL Reference Clock Select (Table 16)
Default: “0010” (BICK pin=64fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	DAC TDM	0	0	0	0	0	0	SDS1	SDS0
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	0	0	0

SDS1-0: DAC TDM Data Select (Table 24)
Default: “00”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Control 1	TDM1	TDM0	DIF2	DIF1	DIF0	ATS1	ATS0	SMUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	1	0	0	0

SMUTE: Soft Mute Enable
0: Normal Operation (default)
1: All DAC outputs are soft muted.

ATS1-0: Transition Time Setting of Digital Attenuator (Table 31)
Default: “00”

DIF2-0: Audio Interface Format Mode Select (Table 23)
Default: “111” (32bit I2S)

TDM1-0: TDM Format Select (Table 23, Table 25, Table 26)
Default: “00” (Stereo Mode)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Control 2	0	0	0	MCKS1	MCKS0	DFS1	DFS0	ACKS
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	0

ACKS: Automatic Clock Recognition Mode
0: Disable, Manual Setting Mode (default)
1: Enable, Auto Setting Mode
When ACKS bit = “1”, master clock frequency is detected automatically. In this case, the setting of DFS1-0 bits is ignored. When ACKS bit = “0”, DFS1-0 bits set the sampling speed mode. The MCKI frequency of each mode is detected automatically.

DFS1-0: Sampling Speed Control (Table 8)
The setting of DFS1-0 bits is ignored when ACKS bit =“1”.

MCKS1-0: Master Clock Input Frequency Select (Table 9)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control	0	FS3	FS2	FS1	FS0	BCKO1	BCKO0	LOPS
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	1	0	1	0

LOPS: Power-save Mode of LOUT/ROUT
0: Normal Operation (default)
1: Power-save Mode

BCKO1-0: BICK Output Frequency Setting in Master Mode (Table 21)
Default: “01” (64fs)

FS3-0: Sampling Frequency (Table 17, Table 18)
Default: “0101”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Filter Setting	FIRDA2	FIRDA1	FIRDA0	SLDA	SDDA	SSLOW	DEM1	DEM0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	1	0	0	1

DEM1-0: De-emphasis response control for DAC (Table 22)
Default: “01”, OFF

SSLOW: Digital Filter Bypass Mode Enable
0: Roll-off filter (default)
1: Super Slow Roll-off Mode

SLDA: DAC Slow Roll-off Filter Enable (Table 28)
0: Sharp Roll-off filter (default)
1: Slow Roll-off Filter

SDDA: DAC Short delay Filter Enable (Table 28)
0: Normal filter
1: Short delay Filter (default)

FIRDA2-0: Out band noise eliminating Filters Setting (Table 32)
default: “001” (48kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	HPF Enable, Filter Setting	0	0	0	0	SLAD	SDAD	HPFER	HPFEL
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		Default	0	0	0	0	1	1	1

HPFEL/R: ADC HPF L/Rch Setting
0: HPF L/Rch OFF
1: HPF L/Rch ON (default)

SLAD: ADC Slow Roll-off Filter Enable (Table 27)
0: Sharp Roll-off filter (default)
1: Slow Roll-off Filter

SDAD: ADC Short delay Filter Enable (Table 27)
0: Normal filter
1: Short delay Filter (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	LOUT Volume Control	ATL7	ATL6	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATL 7-0: Attenuation Level (Table 30)
Default:FF(0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	ROUT Volume Control	ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATLR 7-0: Attenuation Level (Table 30)
Default:FF(0dB)

18. Recommended External Circuits

Figure 77 and Figure 78 show the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

■ Parallel Mode

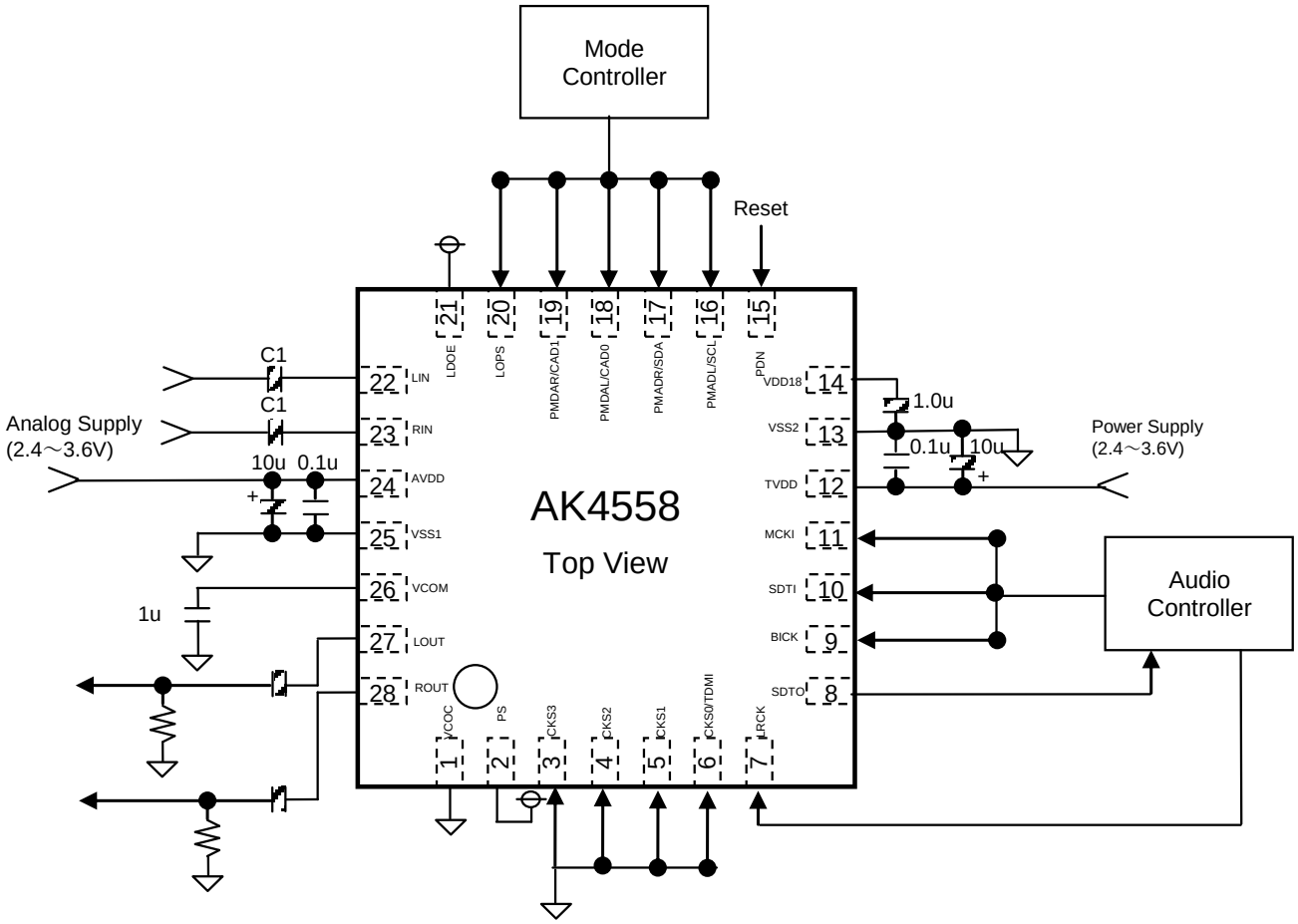


Figure 77. System Connection Diagram (PS pin= “H”, LDOE pin= “H”)

Note:

- VSS1 and VSS2 of the AK4558 must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- An AC coupling capacitor value of at least 10uF is recommended for the LIN and RIN pins to preserve low frequency response.

■ Serial Mode

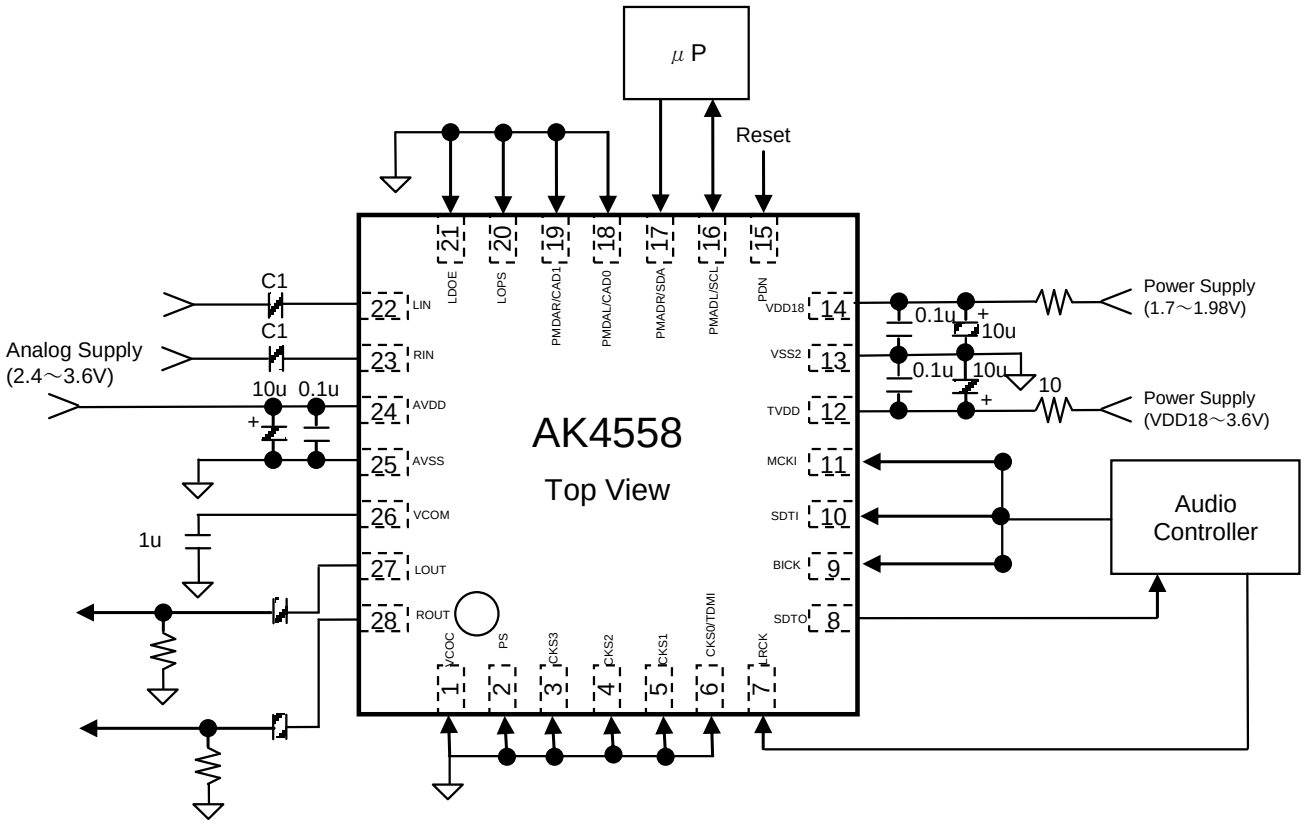


Figure 78. System Connection Diagram (PS pin= “L”, LDOE pin= “L”)

Note:

- VSS1 and VSS2 of the AK4558 must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- An AC coupling capacitor value of at least 10uF is recommended for the LIN and RIN pins to preserve low frequency response.

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to each AVDD and TVDD. AVDD is supplied from analog supply in system and TVDD is supplied from digital supply in system. Power lines of AVDD and TVDD should be distributed separately from the point with low impedance of regulator etc. The power up sequence between AVDD and TVDD is not critical. VSS1 and VSS2 must be connected to the same analog ground plane. Decoupling capacitors for high frequency should be placed as near as possible to the supply pin.

2. Voltage Reference

The voltage of AVDD sets the analog input/output range. Connect a 0.1μF ceramic capacitor between the AVDD pin and the VSS1 pin in parallel with a 10μF electric capacitor. VCOM is a signal ground for this device. A 1.0μF ceramic capacitor attached between the VCOM pin and the VSS1 pin eliminates the effects of high frequency noise. Do not connect the VCOM pin with an external circuit. No load current may be drawn from this pin. All signals, especially clocks, should be kept away from the AVDD, TVDD and VCOM pins in order to avoid unwanted noise coupling into the AK4558.

3. Analog Input

The ADC inputs is single-ended and biased to VCOM voltage (AVDD/2) internally by 8kΩ (typ @ fs=48kHz, 96kHz, 192kHz). The inputs signal range scales with AVDD nominally at 0.8 x AVDD Vpp (typ). The output code format is 2's complement. Input DC offset (including DC offset of the ADC itself) is canceled by an integrated high-pass filter.

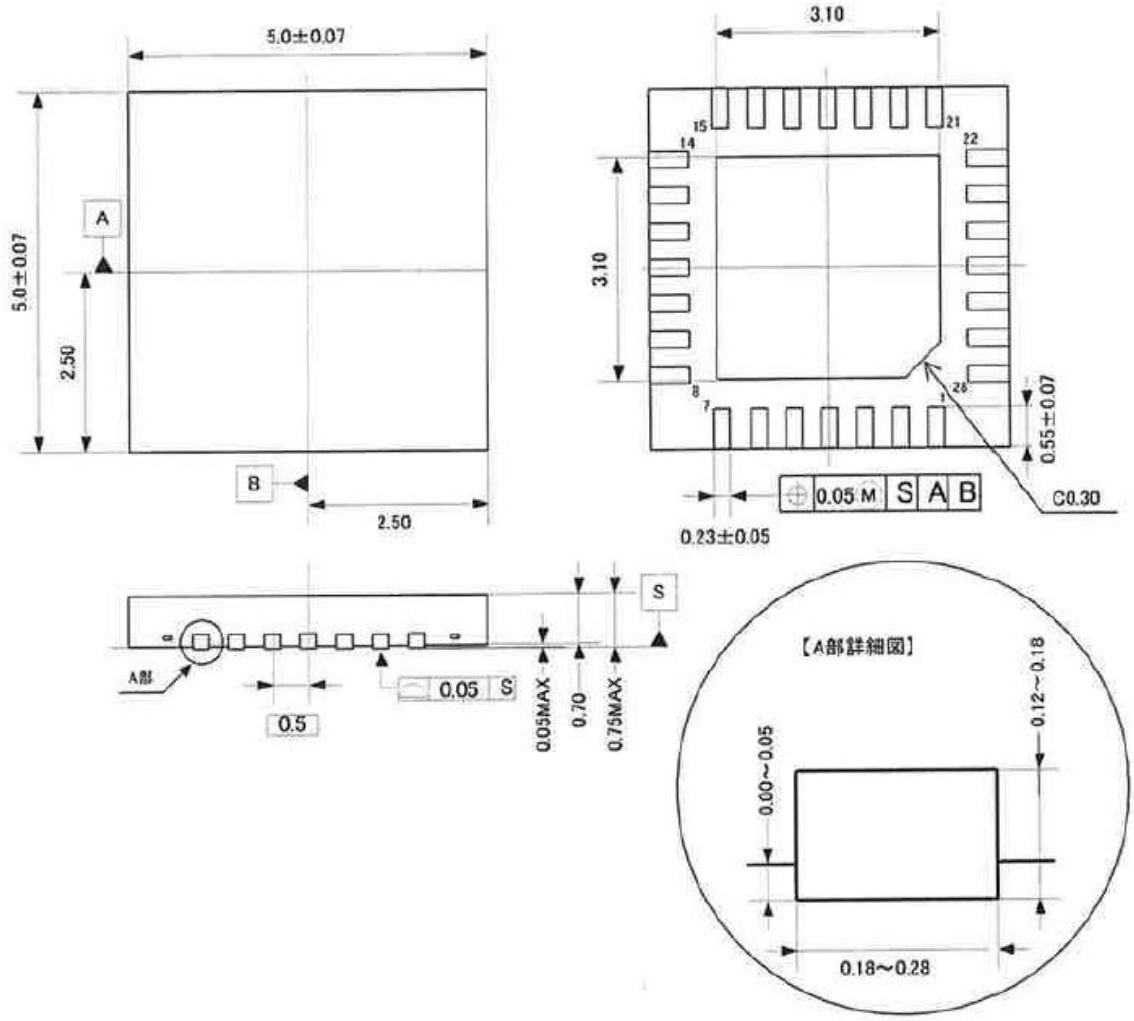
The AK4558 samples the analog input at 128fs (@fs=48kHz), 64fs (@fs=96kHz) or 32fs (@fs=192kHz). A digital filter removes the noise over the stopband attenuation level, except for a band of integral multiplication of the sampling frequency. The AK4558 has an integrated anti-alias RC filter in order to reduce the noise around the sampling frequency.

4. Analog Outputs

The DAC output is single-ended and output range is 0.76 x AVDD Vpp (typ) centered on VCOM. The input data format is two's compliment. The output voltage is positive full scale for 7FFFFFH (@24-bit data) and negative full scale for 800000H (@24-bit data). The ideal output is VCOM for 000000H (@24bit). The Out-of-Band noise (shaping noise) generated by the internal delta-sigma modulator should be attenuated by an external filter if the noise becomes problem.

DC offsets on analog outputs are eliminated by AC coupling since analog outputs has DC offset of VCOM.

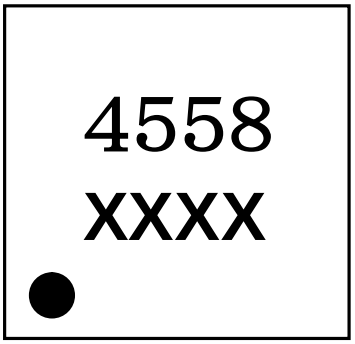
19. Package



■ Materials & Lead Finish

Package molding compound: Epoxy Resin
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

■ **Marking**



Marking Code: 4558
Pin #1 indication
XXXX: Date code (4 digit)

20. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
15/04/02	00	First Edition		
15/04/17	01	Error Correction	1	1. General Description AK4438 → AK4558
15/09/15	02	Description Addition	80	7. Power Down Description (2) was changed.
		Error Correction	86	Addr=04H D4: "RD" →RW"
			86	MCKS1-0: Default="01" → "10"
			86	Addr=05H: Register Name="Filter Setting" → "Mode Control"
			87	Addr=06H: Register Name="Mode Control" → "Filter Setting"

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