

**TrenchMOS™ transistor**  
**Logic level FET**

**PHT6N06LT**

**GENERAL DESCRIPTION**

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. The device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in DC-DC converters and general purpose switching applications.

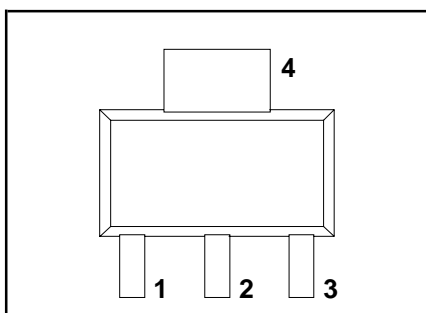
**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Drain-source voltage	55	V
$I_D$	Drain current (DC) $T_{sp} = 25\text{ °C}$	5.5	A
	Drain current (DC) $T_{amb} = 25\text{ °C}$	2.5	A
$P_{tot}$	Total power dissipation	8.3	W
$T_j$	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 5\text{ V}$	150	mΩ

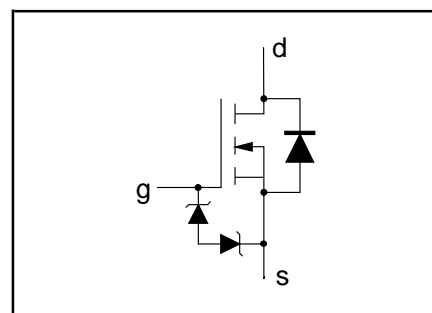
**PINNING - SOT223**

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

**PIN CONFIGURATION**



**SYMBOL**



**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-	-	55	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$V_{GS}$	Gate-source voltage	-	-	±13	V
$I_D$	Drain current (DC)	$T_{sp} = 25\text{ °C}$	-	5.5	A
		$T_{amb} = 25\text{ °C}$	-	2.5	A
$I_D$	Drain current (DC)	$T_{sp} = 100\text{ °C}$	-	3.8	A
		$T_{amb} = 100\text{ °C}$	-	1.75	A
$I_{DM}$	Drain current (pulse peak value)	$T_{sp} = 25\text{ °C}$	-	22	A
		$T_{amb} = 25\text{ °C}$	-	10	A
$P_{tot}$	Total power dissipation	$T_{sp} = 25\text{ °C}$	-	8.3	W
		$T_{amb} = 25\text{ °C}$	-	1.8	W
$T_{stg}, T_j$	Storage & operating temperature	-	- 55	150	°C

**ESD LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_C$	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

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### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j-amb}$	From junction to ambient	Mounted on PCB of Fig.17	-	70	K/W

### STATIC CHARACTERISTICS

$T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$ $T_j = -55^\circ\text{C}$	55 50	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$ $T_j = 150^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1.0 0.6	1.5 -	2.0 -	V V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 55\text{ V}; V_{GS} = 0\text{ V};$ $T_j = 150^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 5\text{ V}$ $T_j = 150^\circ\text{C}$	-	0.02	1	$\mu\text{A}$
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	$V_{GS} = \pm 1\text{ mA}$ $T_j = 150^\circ\text{C}$	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 5\text{ A}$ $T_j = 150^\circ\text{C}$	-	120	150	m $\Omega$
			-	-	277	m $\Omega$

### DYNAMIC CHARACTERISTICS

$T_{mb} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$g_{fs}$	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 5\text{ A}; T_j = 25^\circ\text{C}$	3	5	-	S
$Q_{g(tot)}$	Total gate charge	$I_D = 5\text{ A}; V_{DD} = 44\text{ V}; V_{GS} = 5\text{ V}$	-	4.5	-	nC
$Q_{gs}$	Gate-source charge		-	1	-	nC
$Q_{gd}$	Gate-drain (Miller) charge		-	2.5	-	nC
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	250	330	pF
$C_{oss}$	Output capacitance		-	65	80	pF
$C_{rss}$	Feedback capacitance		-	35	50	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 5\text{ A};$	-	11	17	ns
$t_r$	Turn-on rise time	$V_{GS} = 5\text{ V}; R_G = 10\ \Omega;$	-	38	60	ns
$t_{d\ off}$	Turn-off delay time		-	25	38	ns
$t_f$	Turn-off fall time	$T_j = 25^\circ\text{C}$	-	20	38	ns

### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = -55$  to  $175^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DR}$	Continuous reverse drain current	$T_{sp} = 25^\circ\text{C}$	-	-	5.5	A
$I_{DRM}$	Pulsed reverse drain current	$T_{sp} = 25^\circ\text{C}$	-	-	30	A
$V_{SD}$	Diode forward voltage	$I_F = 2\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.1	V
$t_{rr}$	Reverse recovery time	$I_F = 2\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	43	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{GS} = -10\text{ V}; V_R = 30\text{ V}$	-	0.16	-	$\mu\text{C}$

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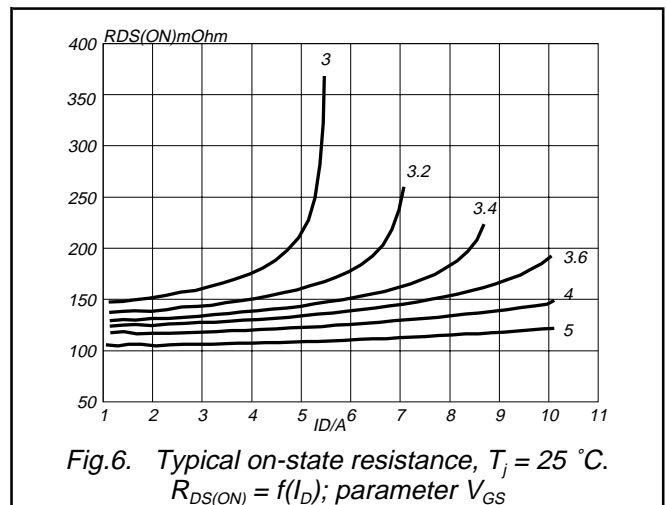
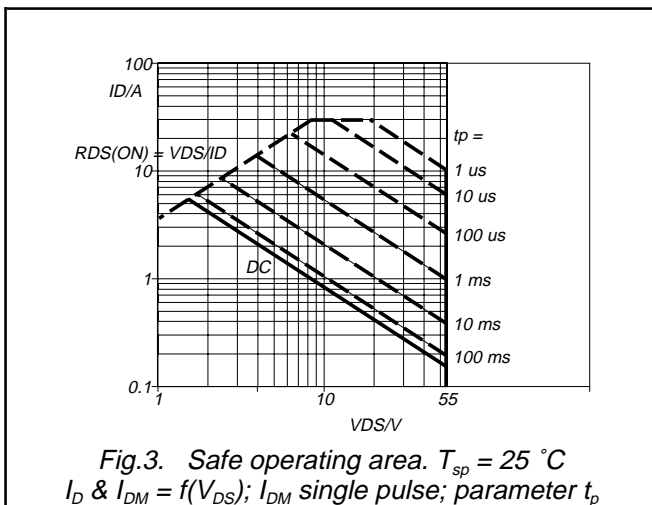
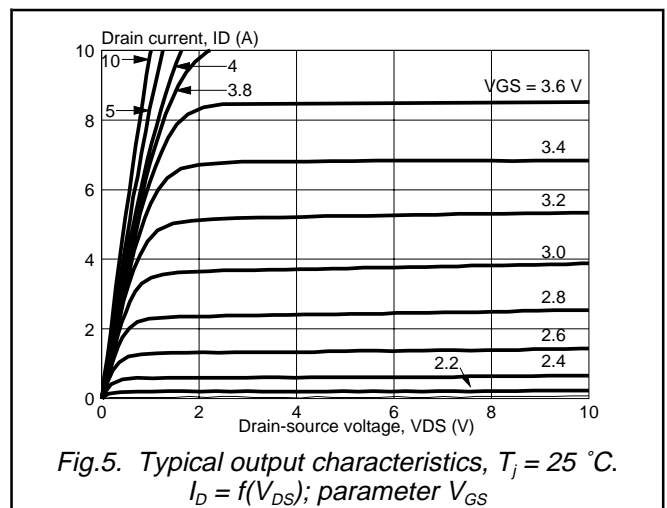
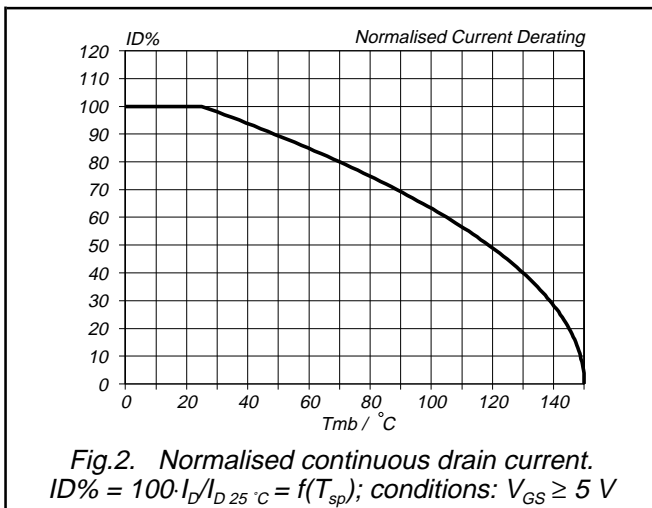
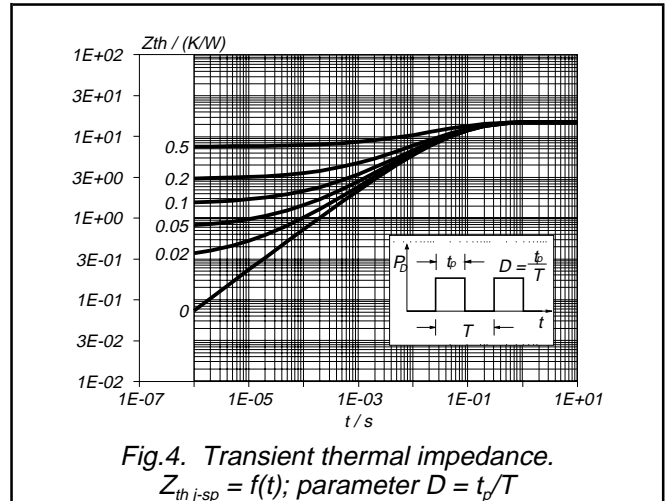
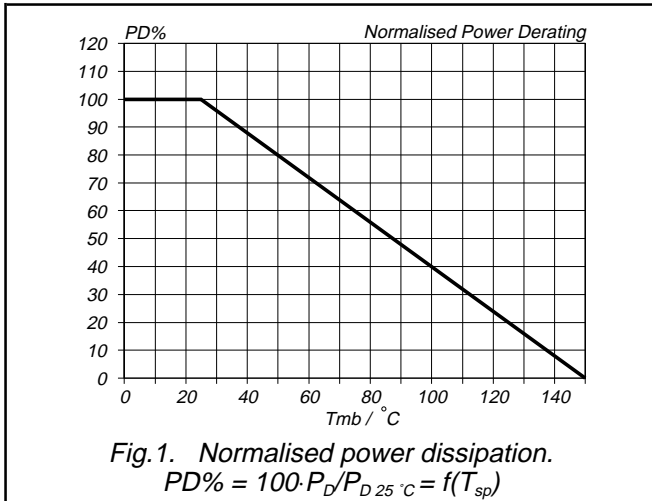
PHT6N06LT

**AVALANCHE LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$W_{DSS}$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 1.9 \text{ A}; V_{DD} \leq 25 \text{ V};$ $V_{GS} = 5 \text{ V}; R_{GS} = 50 \Omega; T_{sp} = 25 \text{ }^\circ\text{C}$	-	-	15	mJ

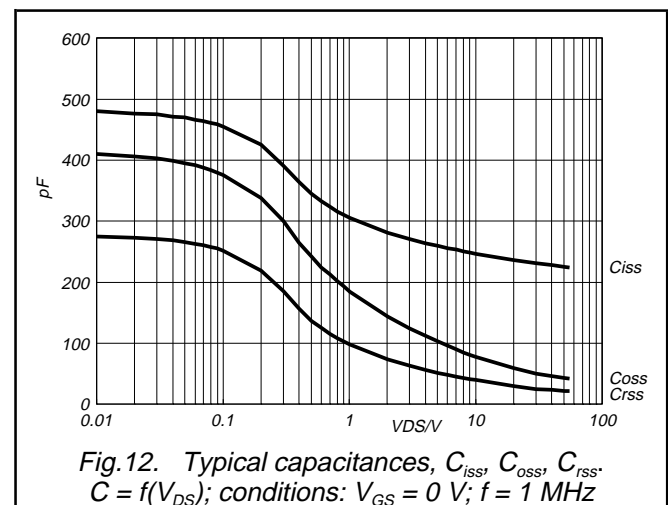
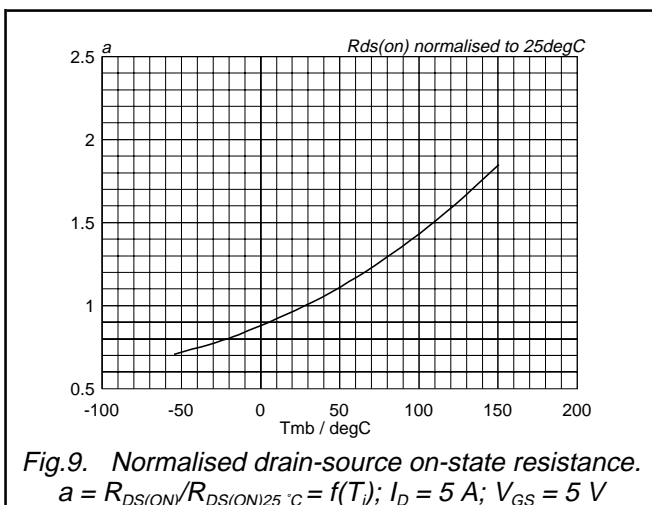
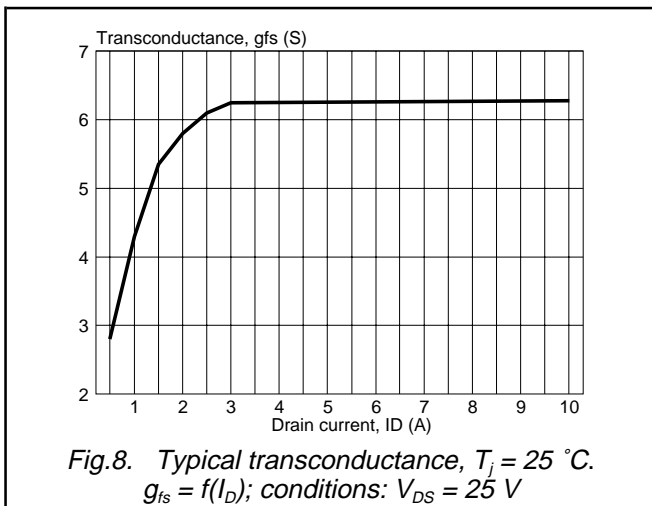
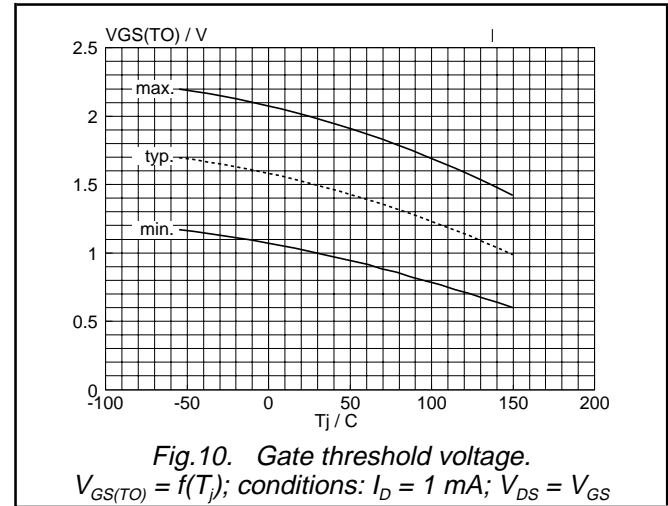
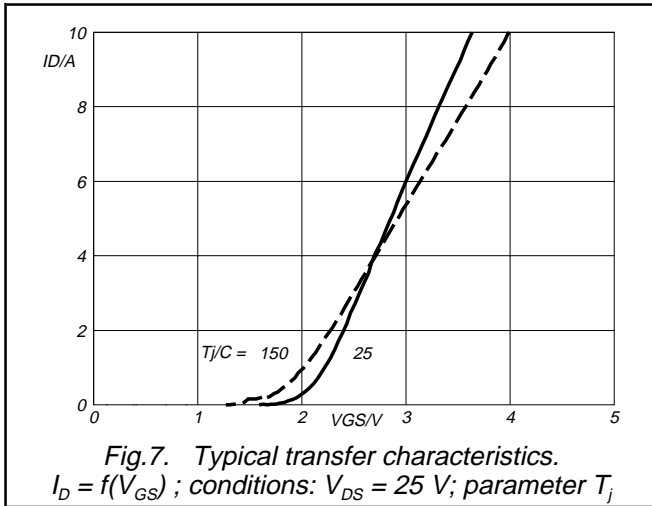
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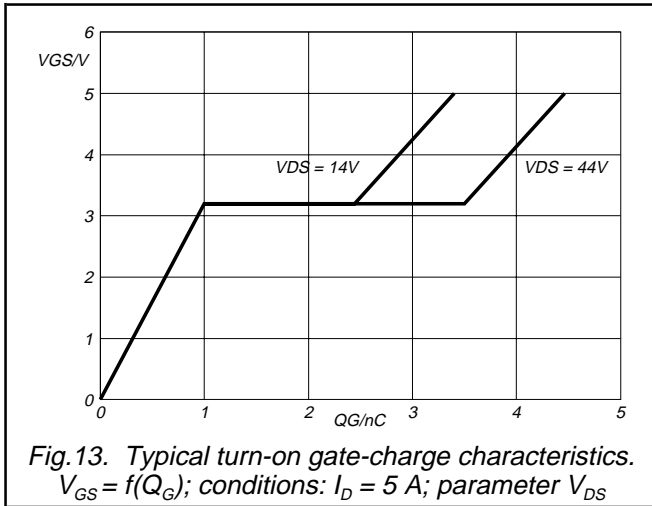


Fig.13. Typical turn-on gate-charge characteristics.  
 $V_{GS} = f(Q_G)$ ; conditions:  $I_D = 5 A$ ; parameter  $V_{DS}$

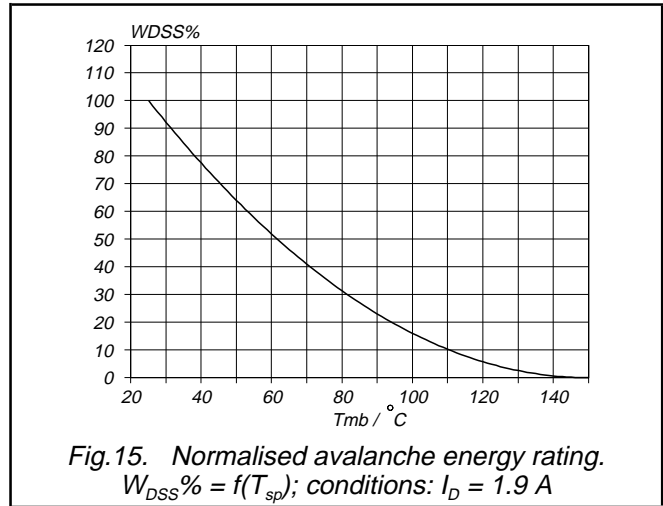


Fig.15. Normalised avalanche energy rating.  
 $W_{DSS}\% = f(T_{sp})$ ; conditions:  $I_D = 1.9 A$

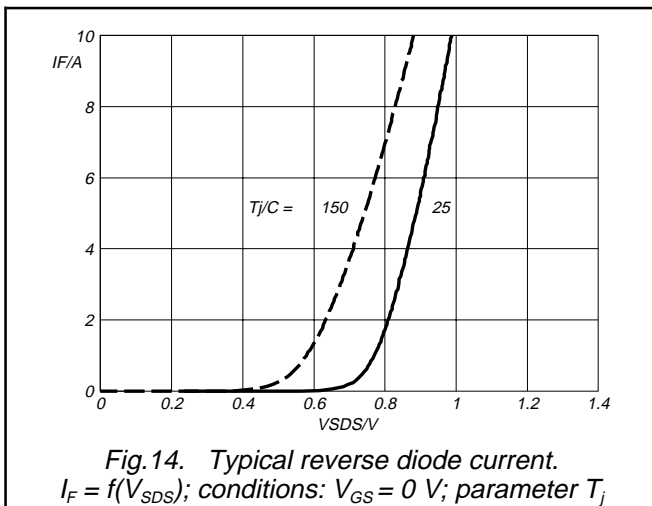


Fig.14. Typical reverse diode current.  
 $I_F = f(V_{SDS})$ ; conditions:  $V_{GS} = 0 V$ ; parameter  $T_j$

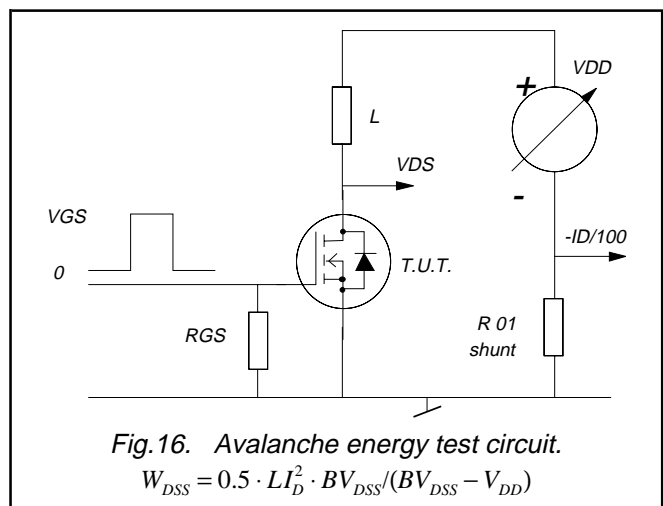
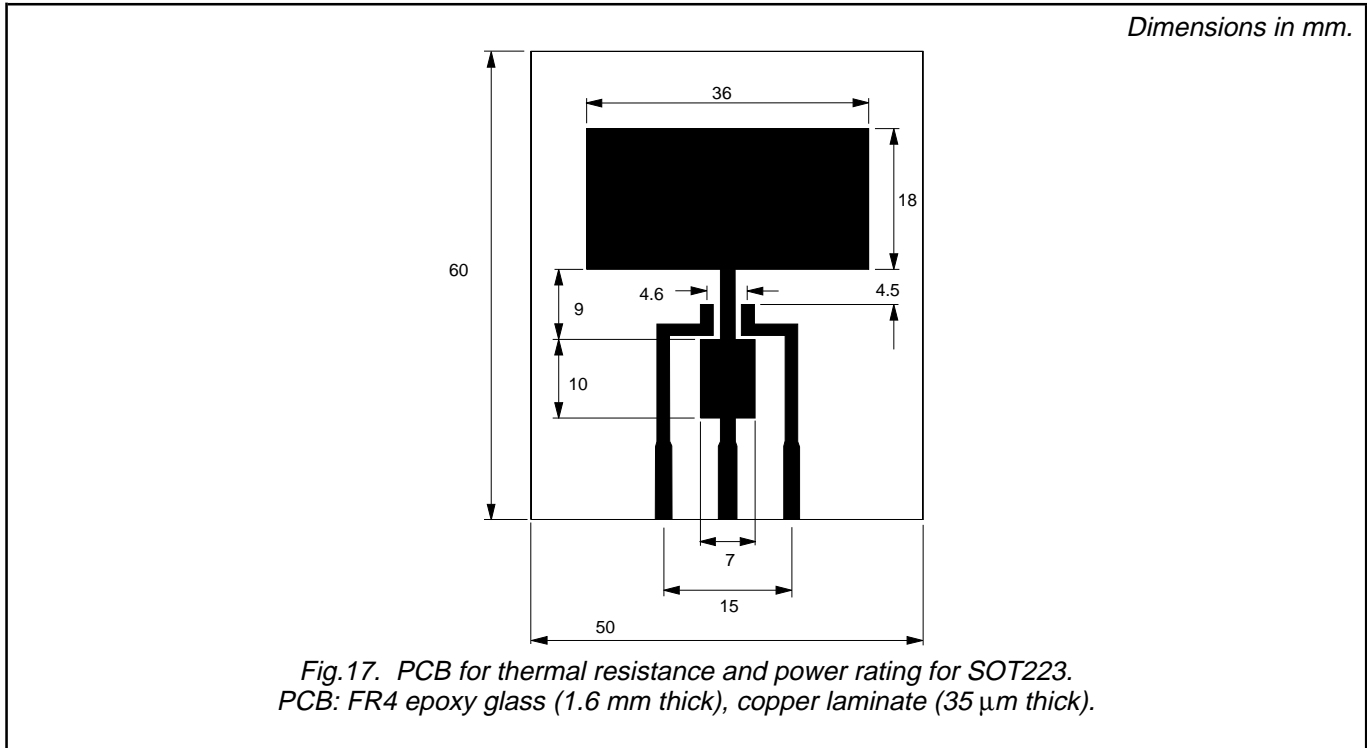


Fig.16. Avalanche energy test circuit.  
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

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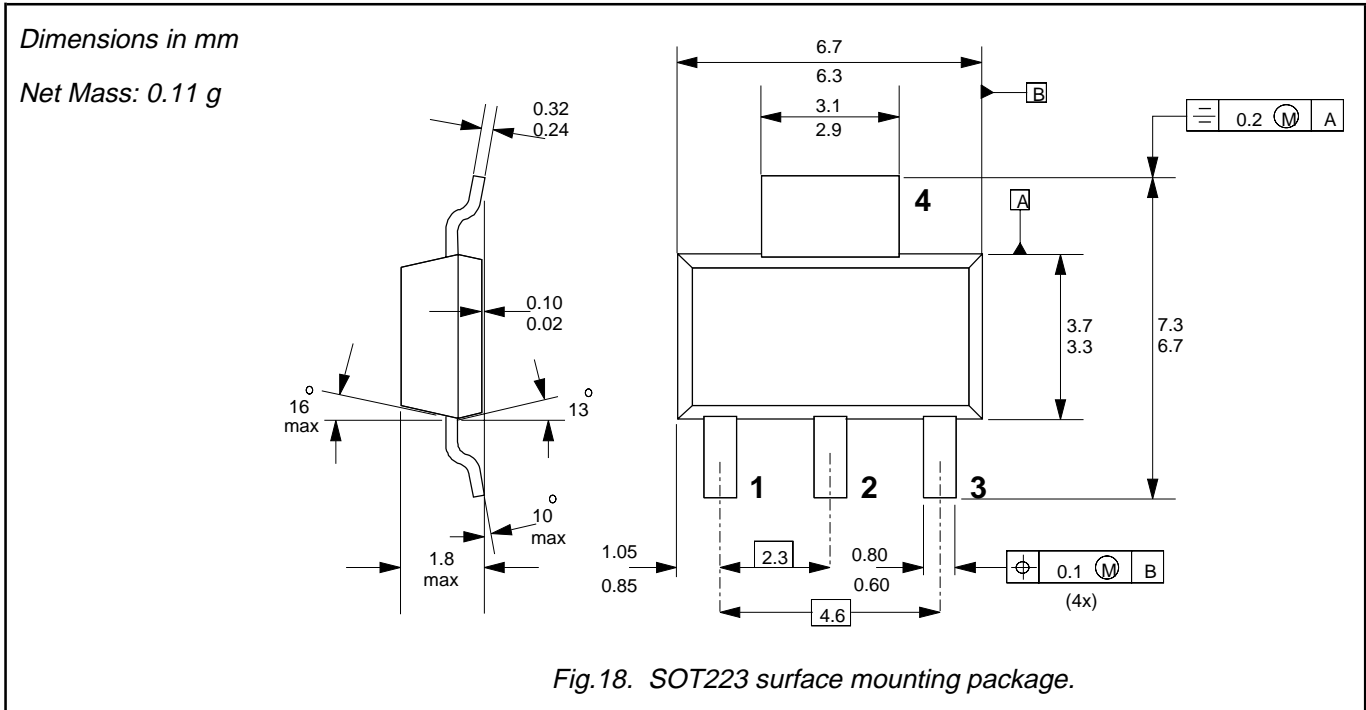
PRINTED CIRCUIT BOARD



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**MECHANICAL DATA**



**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".



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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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