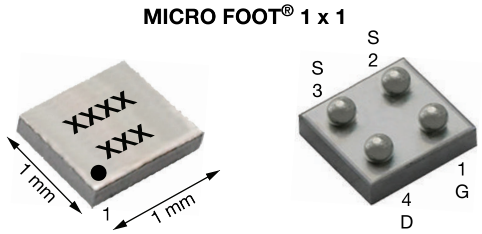
# P-Channel 8 V (D-S) MOSFET

## PRODUCT SUMMARY

| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) | $I_D$ (A) [a, e] | $Q_g$ (TYP.) |
|---|---|---|---|
| -8 | 0.064 at $V_{GS}$ = -4.5 V | -4.6 | 6.9 nC |
| | 0.076 at $V_{GS}$ = -2.5 V | -4.2 | |
| | 0.115 at $V_{GS}$ = -1.5 V | -3.4 | |
| | 0.180 at $V_{GS}$ = -1.2 V | -1.2 | |

**MICRO FOOT® 1 x 1**




Backside View    Bump Side View

**Marking Code:** xxxx = 8469

xxx = Date / lot traceability code

**Ordering Information**:

Si8469DB-T2-E1 (lead (Pb)-free and halogen-free)

## FEATURES

- TrenchFET® power MOSFET
- Ultra-Small 1 mm x 1 mm maximum outline
- Ultra-thin 0.548 mm maximum height
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

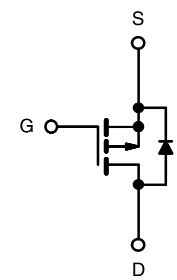
Pb-free

RoHS COMPLIANT

HALOGEN FREE

## APPLICATIONS

- Load switches, battery switches and charger switches in portable device applications
- Load switch for 1.2 V power line




P-Channel MOSFET

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, unless otherwise noted)

| PARAMETER | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -8 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 5 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $T_A$ = 25 °C | $I_D$ | -4.6 [a] | A |
| | $T_A$ = 70 °C | | -3.7 [a] | |
| | $T_A$ = 25 °C | | -3.6 [b] | |
| | $T_A$ = 70 °C | | -2.8 [b] | |
| Pulsed Drain Current | | $I_{DM}$ | -15 | |
| Continuous Source-Drain Diode Current | $T_A$ = 25 °C | $I_S$ | -1.4 [a] | |
| | $T_A$ = 25 °C | | -0.6 [b] | |
| Maximum Power Dissipation | $T_A$ = 25 °C | $P_D$ | 1.8 [a] | W |
| | $T_A$ = 70 °C | | 1.1[a] | |
| | $T_A$ = 25 °C | | 0.78 [b] | |
| | $T_A$ = 70 °C | | 0.5 [b] | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Package Reflow Conditions [c] | VPR | | 260 | |
| | IR/Convection | | 260 | |

## THERMAL RESISTANCE RATINGS

| PARAMETER | | SYMBOL | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [f, g] | t = 10 s | $R_{thJA}$ | 55 | 70 | °C/W |
| Maximum Junction-to-Ambient [h, i] | t = 10 s | | 125 | 160 | |

**Notes**

a. Surface mounted on 1" x 1" FR4 board with full copper, t = 10 s.
b. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 10 s.
c. Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering.
d. In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.
e. Based on $T_A$ = 25 °C.
f. Surface mounted on 1" x 1" FR4 board with full copper.
g. Maximum under steady state conditions is 100 °C/W.
h. Surface mounted on 1" x 1" FR4 board with minimum copper.
i. Maximum under steady state conditions is 190 °C/W.

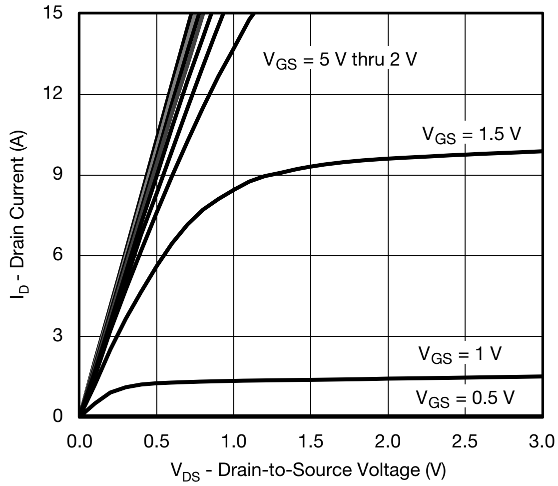
| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = -250 μA | -8 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D$ = -250 μA | - | -6.4 | - | mV/°C |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | - | 2.4 | - | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = -250 μA | -0.35 | - | -0.8 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 5 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -8 V, $V_{GS}$ = 0 V | - | - | -1 | μA |
| | | $V_{DS}$ = -8 V, $V_{GS}$ = 0 V, $T_J$ = 70 °C | - | - | -10 | |
| On-State Drain Current [a] | $I_{D(on)}$ | $V_{DS}$ ≤ -5 V, $V_{GS}$ = -4.5 V | -10 | - | - | A |
| Drain-Source On-State Resistance [a] | $R_{DS(on)}$ | $V_{GS}$ = -4.5 V, $I_D$ = -1.5 A | - | 0.052 | 0.064 | Ω |
| | | $V_{GS}$ = -2.5 V, $I_D$ = -1 A | - | 0.062 | 0.076 | |
| | | $V_{GS}$ = -1.5 V, $I_D$ = -0.3 A | - | 0.085 | 0.115 | |
| | | $V_{GS}$ = -1.2 V, $I_D$ = -0.3 A | - | 0.110 | 0.180 | |
| Forward Transconductance [a] | $g_{fs}$ | $V_{DS}$ = -4 V, $I_D$ = -1.5 A | - | 12 | - | S |
| **Dynamic [b]** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = -4 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 900 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 315 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 260 | - | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = -4 V, $V_{GS}$ = -4.5 V, $I_D$ = -1.5 A | - | 11 | 17 | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 0.85 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 2.5 | - | |
| Gate Resistance | $R_g$ | $V_{GS}$ = -0.1 V, f = 1 MHz | - | 6 | - | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = -4 V, $R_L$ = 2.7 Ω<br>$I_D$ ≅ -1.5 A, $V_{GEN}$ = -4.5 V, $R_g$ = 1 Ω | - | 15 | 30 | ns |
| Rise Time | $t_r$ | | - | 22 | 45 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 35 | 70 | |
| Fall Time | $t_f$ | | - | 17 | 35 | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | $T_A$ = 25 °C | - | - | -1.5 | A |
| Pulse Diode Forward Current | $I_{SM}$ | | - | - | -15 | |
| Body Diode Voltage | $V_{SD}$ | $I_S$ = -1.5 A, $V_{GS}$ = 0 V | - | -0.9 | -1.3 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $I_F$ = -1.5 A, dI/dt = 100 A/μs, $T_J$ = 25 °C | - | 25 | 50 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | - | 10 | 20 | nC |
| Reverse Recovery Fall Time | $t_a$ | | - | 10 | - | ns |
| Reverse Recovery Rise Time | $t_b$ | | - | 15 | - | |

**Notes**

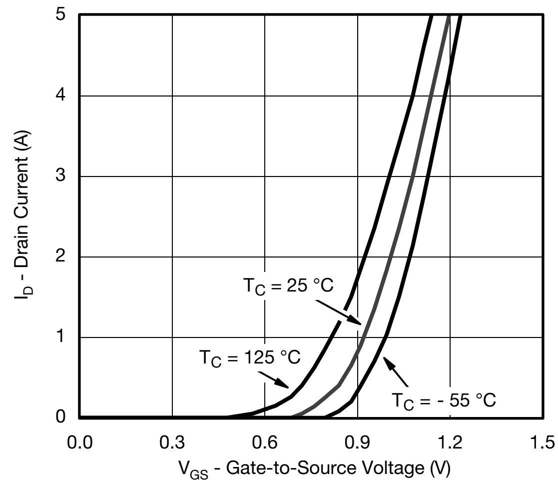
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

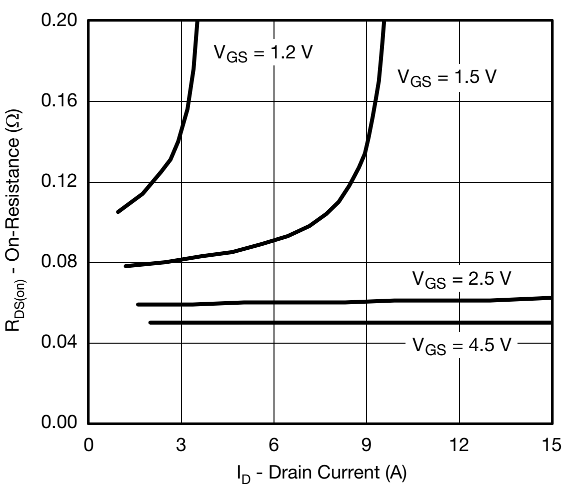
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



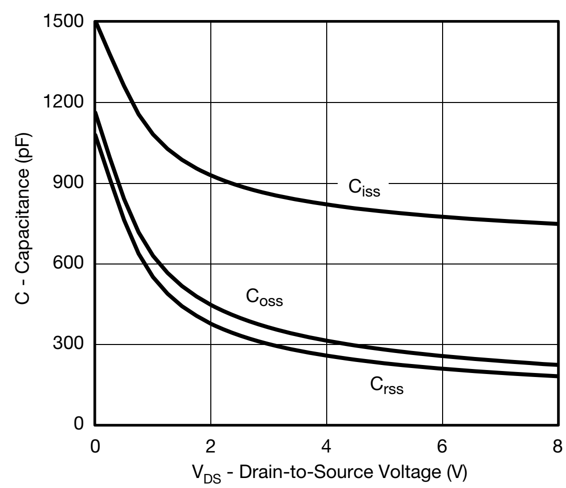

**Output Characteristics**



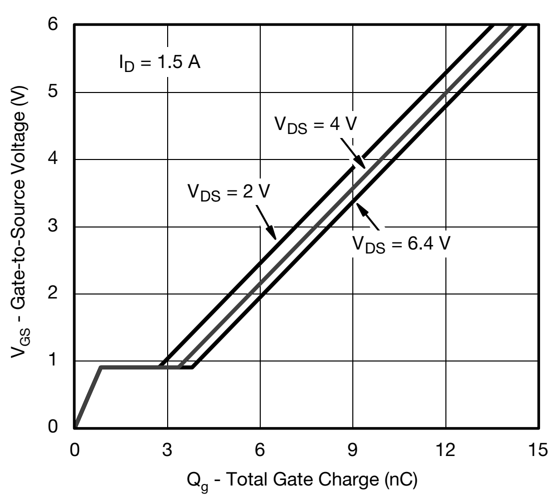

**Transfer Characteristics**



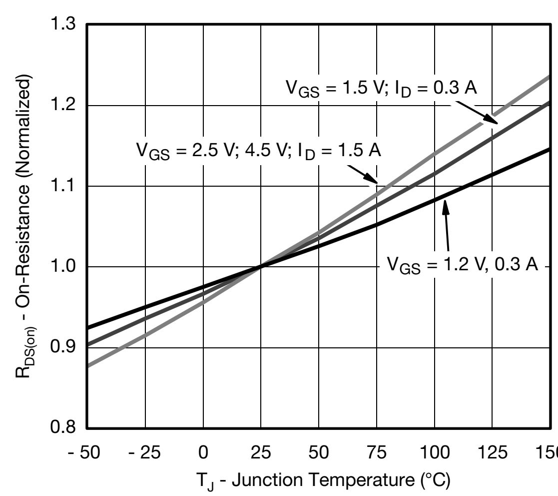

**On-Resistance vs. Drain Current and Gate Voltage**




**Capacitance**

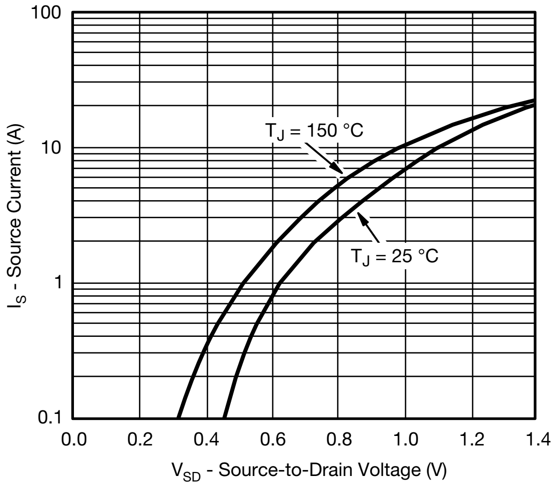



**Gate Charge**

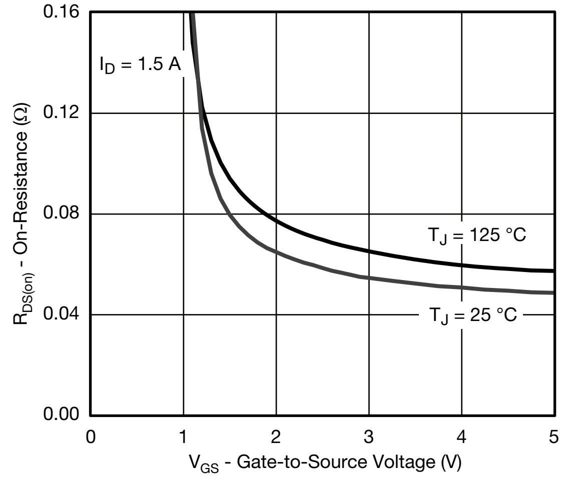



**On-Resistance vs. Junction Temperature**

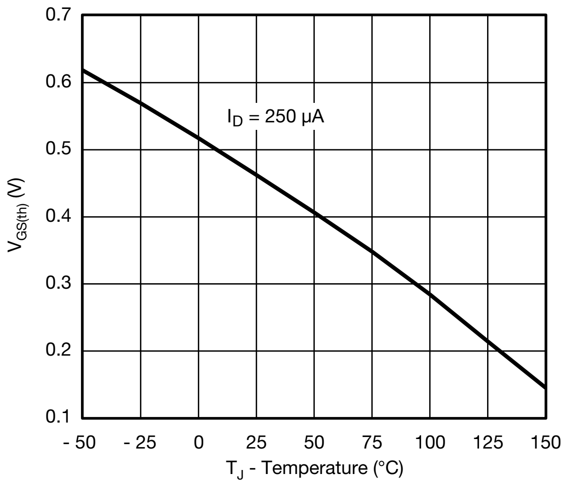
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



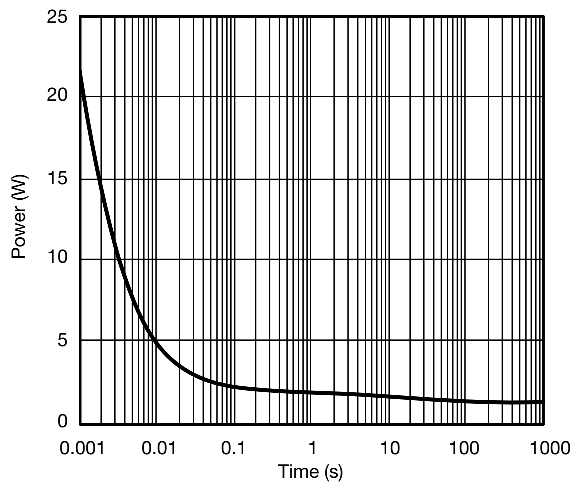

**Source-Drain Diode Forward Voltage**



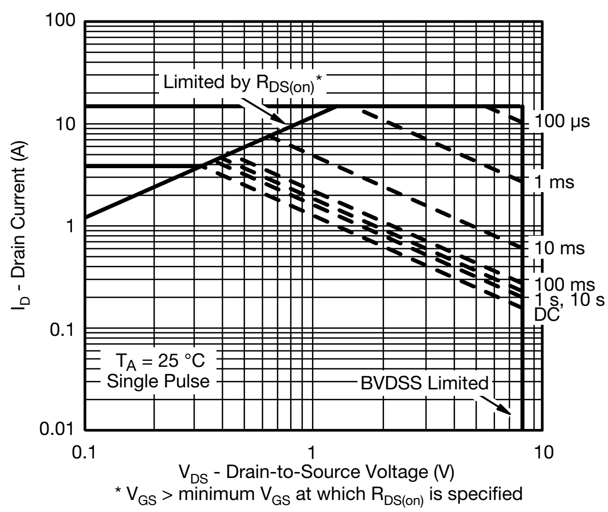

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**

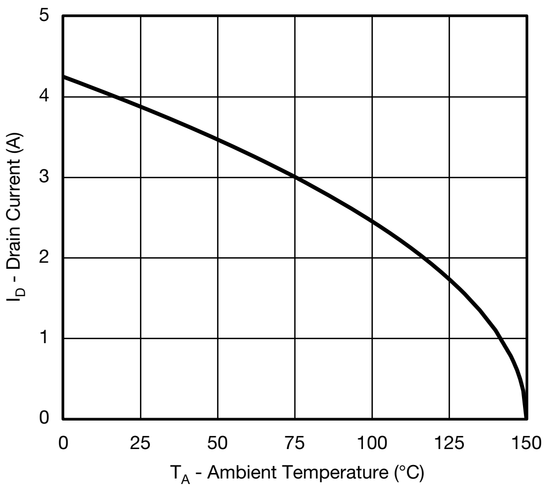



**Single Pulse Power, Junction-to-Ambient**

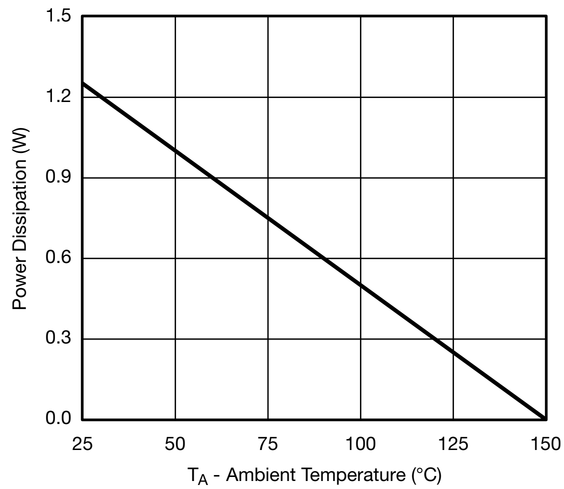



**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Current Derating** [a]




**Power Derating**

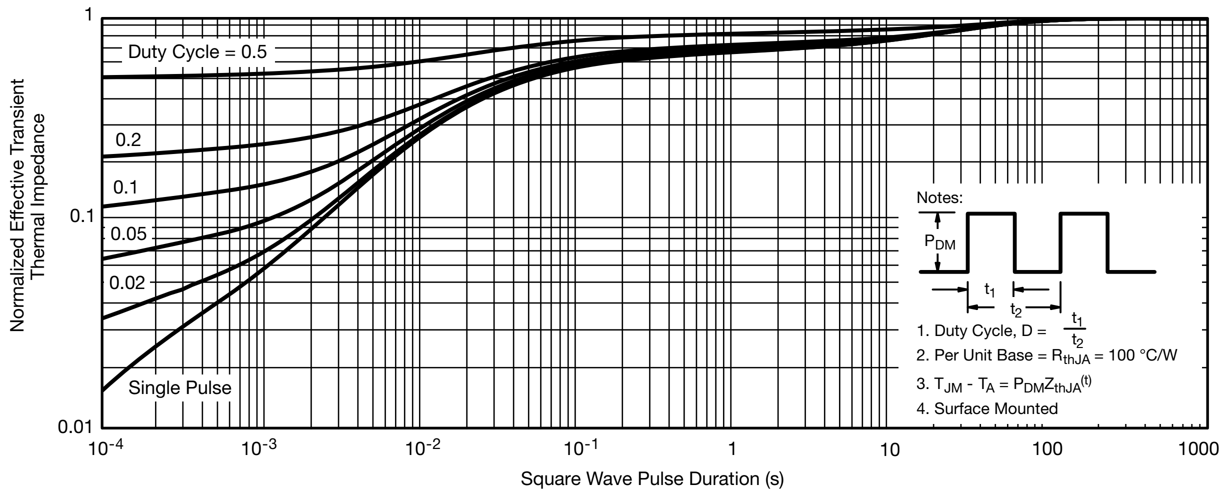
**Note**

- When mounted on 1" x 1" FR4 with full copper.

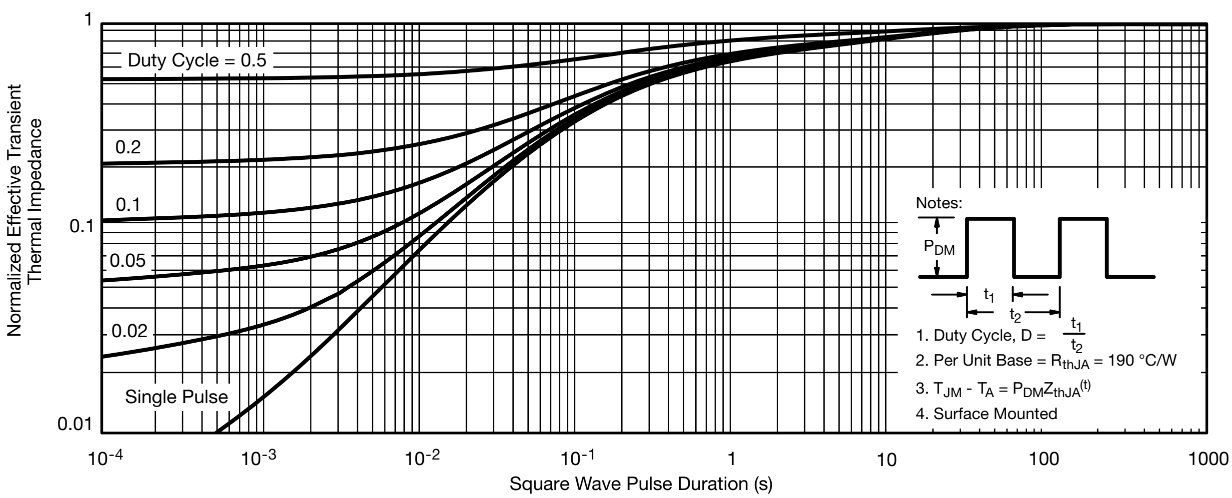
**Note**

a. The power dissipation $P_D$ is based on $T_J$ (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



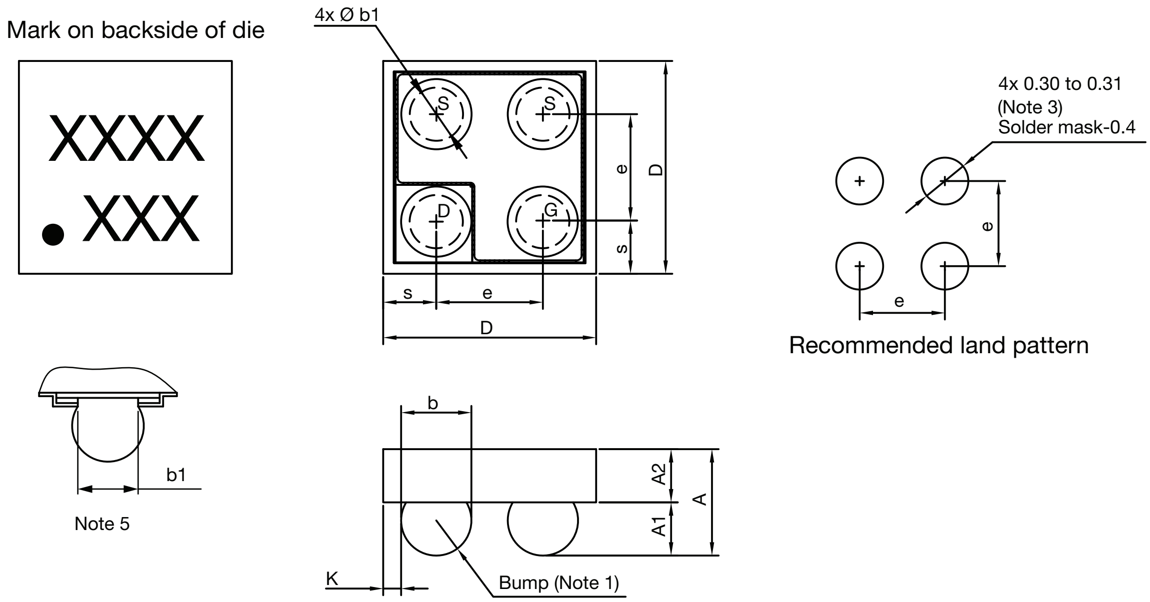

**Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Full Copper)**




**Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Minimum Copper)**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67091.*

# MICRO FOOT®: 4-Bumps
# (1 mm x 1 mm, 0.5 mm Pitch, 0.286 mm Bump Height)




**Notes**

1. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
2. Backside surface is coated with a Ti/Ni/Ag layer.
3. Non-solder mask defined copper landing pad.
4. Laser mark on the backside surface of die.
5. "b1" is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
6. • is the location of pin 1

| DIM. | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.458 | 0.504 | 0.550 | 0.0180 | 0.0198 | 0.0217 |
| A1 | 0.214 | 0.250 | 0.286 | 0.0084 | 0.0098 | 0.0113 |
| A2 | 0.244 | 0.254 | 0.264 | 0.0096 | 0.0100 | 0.0104 |
| b | 0.297 | 0.330 | 0.363 | 0.0117 | 0.0130 | 0.0143 |
| b1 | | 0.250 | | | 0.0098 | |
| e | | 0.500 | | | 0.0197 | |
| s | 0.210 | 0.230 | 0.250 | 0.0083 | 0.0091 | 0.0096 |
| D | 0.920 | 0.960 | 1.000 | 0.0362 | 0.0378 | 0.0394 |
| K | 0.029 | 0.065 | 0.102 | 0.0011 | 0.0026 | 0.0040 |

**Note**

- Use millimeters as the primary measurement.

ECN: T15-0176-Rev. A, 27-Apr-15
DWG: 6039

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