Honeywell

# HTADC12 High Temperature 12-Bit A/D Converter


The HTADC12 is a high temperature, single supply, 12-bit, 100kSPS, analog-to-digital converter with on-chip buffered voltage reference and an on-chip analog input buffer. The HTADC12 uses a Successive Approximation Register (SAR) architecture that does not require an input sample-and-hold amplifier to provide 12-bit resolution at 100 kSPS data rates over the full operating temperature range of -55°C to +225°C.

The HTADC12 is fabricated on a high temperature SOI-IV Silicon On Insulator (SOI) process with very low power consumption.

The input of the HTADC12 allows for easy interfacing to sensors for data conversion applications. The direct input supports 0V to 2.5V signals and includes an on-chip buffer to allow for full 5V input signals. The product is offered with both a serial and parallel digital output interface. The switched capacitor charge-redistribution DAC architecture does not require a sample-and-hold input stage.

It is well suited for both multiplexed systems that switch full-scale voltage levels in successive channels and also for sampling single-channel inputs at frequencies up to and well beyond the Nyquist rate. An internal clock is used to operate the HTADC12.

The digital output data is presented in straight binary output format. There are three output formats: 12 bit parallel, two 8 bit parallel, and serial.

## Features

- Monolithic 12-Bit, 100 kSPS A/D Converter
- Operating temperature range of -55°C to +225°C
- Single +5 V analog supply
- Built in high temperature voltage reference
- Buffered voltage reference output pin
- Built-in analog input buffer
- Straight binary output data
- Typical INL of +/- 0.5 LSB at 250°C
- Parallel 12-bit output or serial output
- Input flexibility to use internal reference or off-chip reference.

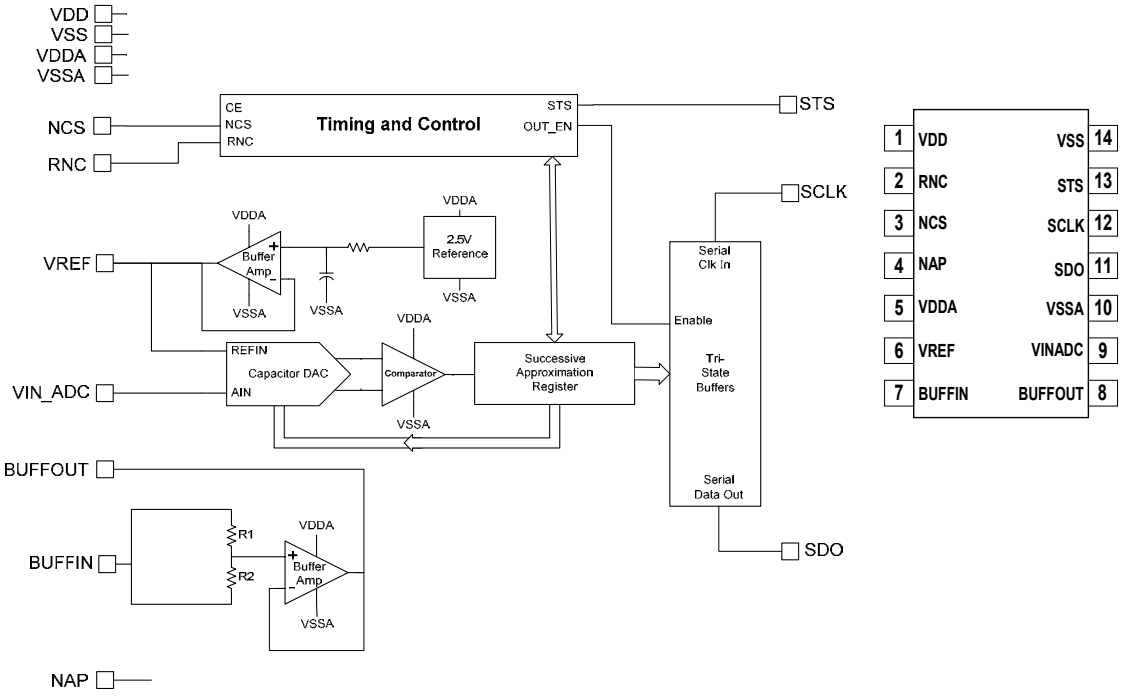
## High Temp and Ruggedized Package

The HTADC12 is packaged in a 14 or 28 lead ceramic DIP package.

## Low Power

The HTADC12, at 10 mW, consumes a fraction of the power of presently available ADCs in existing monolithic solutions.

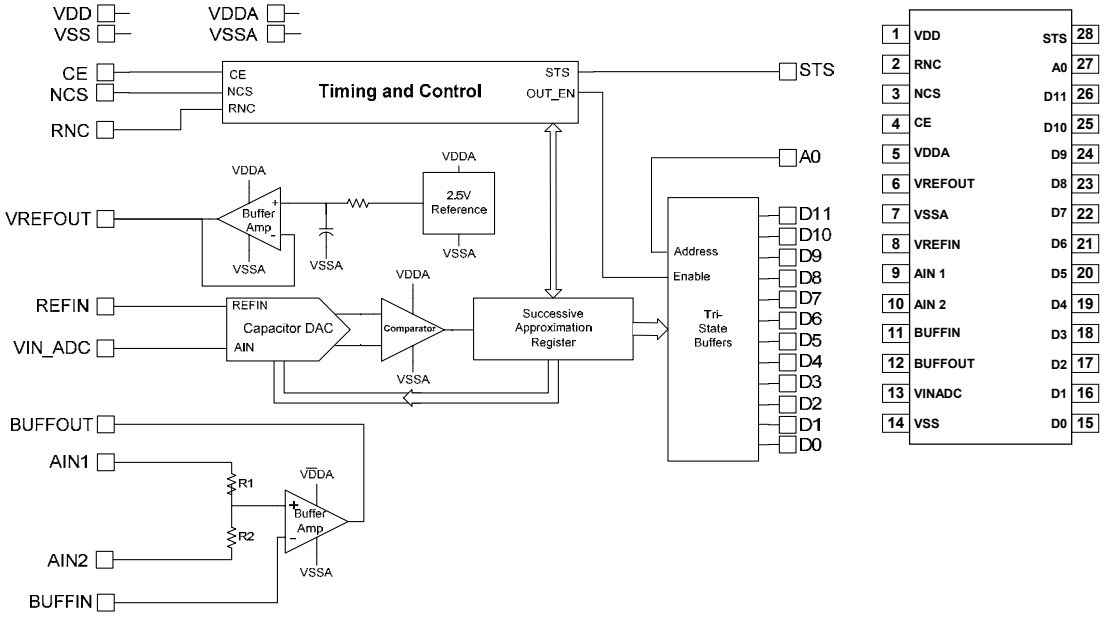
# 14 Lead Package Block and PIN Diagrams




| Pin Description | | |
|---|---|---|
| **Pin** | **Pin Name** | **Description** |
| 1 | VDD | 5V Digital Supply |
| 2 | RNC | Read/Not Convert Input – A high-to-low transition initiates an A-to-D conversion.<br>When held low, the outputs are in a high impedance mode. |
| 3 | NCS | Not Chip Select Input – A low input will select the chip and enable the outputs.<br>A high input will de-select the chip and place the outputs in a high impedance state. |
| 4 | NAP | Power down control (digital input). A low input for normal operation.<br>A high input for power down mode. |
| 5 | VDDA | 5V Analog Supply |
| 6 | VREF | VREF Buffered Output. Nominally 2.5V buffered output of on-chip voltage reference. This signal is also connected internally to the Capacitor DAC reference input. This signal should be left open on the board. |
| 7 | BUFFIN | Analog Buffer Amp Input – This is the input to the unity gain buffer amplifier. |
| 8 | BUFFOUT | Unity Gain Buffer Output. Unity gain buffer output based on the BUFFIN signal. |
| 9 | VIN ADC | ADC Signal Input. |
| 10 | VSSA | Analog Ground |
| 11 | SDO | Serial Data Output – Digital data output. This is a tri-state output driver.[1] |
| 12 | SCLK | Serial Clock Input – This signal is used to clock out the serial digital data. |
| 13 | STS | Status Output – A low signal indicates the conversion is complete and the data is available at the outputs.<br>A high signal indicates a conversion is in process. |
| 14 | VSS | Digital Ground |

*(1) The data outputs may be put into a high impedance state according to truth table.*

# 28 Lead Package Block and PIN Diagrams




| Pin Description | | |
|---|---|---|
| **Pin** | **Pin Name** | **Description** |
| 1 | VDD | 5V Digital Supply[2] |
| 2 | RNC | Read/Not Convert Input – A high-to-low transition initiates an A-to-D conversion.<br>When held low, the outputs are in a high impedance mode. |
| 3 | NCS | Not Chip Select Input – A low input will select the chip and enable the outputs.<br>A high input will de-select the chip and place the outputs in a high impedance state. |
| 4 | CE | Chip Enable Input – A high input will enable the chip and enable the outputs.<br>A low input will disable the chip and place the outputs in a high impedance state. |
| 5 | VDDA | 5V Analog Supply[2] |
| 6 | VREFOUT | VREF Buffered Output. Nominally 2.5V buffered output of on-chip voltage reference.<br>May be connected to VREFIN on the board. |
| 7 | VSSA | Analog Ground |
| 8 | VREFIN | Voltage Reference Input. May be connected to VREFOUT or to an external voltage reference. |
| 9 | AIN1 | Analog Input – Input to buffer amplifier |
| 10 | AIN2 | Analog Input – Input to buffer amplifier |
| 11 | BUFFIN | Analog Input – Input to negative terminal of the buffer amplifier |
| 12 | BUFFOUT | Analog Buffer Output |
| 13 | VIN | ADC Signal Input – Analog input signal |
| 14 | VSS | Digital Ground |
| 15 | DO | Data Output. D0 is the LSB. This is a tri-state output driver.[1] |
| 16-26 | D1 – D11 | Data Output. D1 – D11. These are tri-state output drivers.[1] |
| 27 | AO | Output Data Byte Select Input – The digital data can be output as a standard 12 bit parallel output or can be presented in two 8-bit bytes for use with 8 bit microprocessors.<br>The 8 bit bus will be aligned with D4 – D11.<br>When A0 is low, the digital data is output in a standard 12 bit format (D0 = LSB).<br>This will also represent the first byte (bits D4 – D11) for an 8 bit system.<br>When A0 is high, the second byte will be available at the output. D11 through D8 now contain the 4 LSB's of the 12-bit parallel data (D0 – D3). |
| 28 | STS | Status Output – A low signal indicates the conversion is complete and the data is available at the outputs.<br>A high signal indicates a conversion is in process. |

*(1) The data outputs may be put into a high impedance state according to truth table.*

*(2) These power supplies are required to be the same supply on the board. They cannot be independent supplies.*

# Signal Definition

### Analog Input Options

The analog input signal may be connected directly to the VIN ADC input or go through a buffer amplifier.

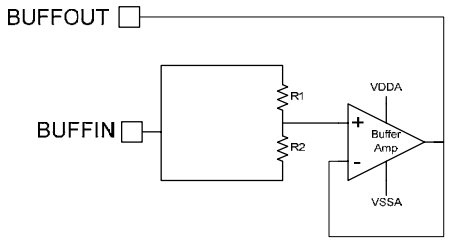
### Direct into VINADC

The input range can be from 0V to VREFIN. This input is nominally high impedance but should be driven by a low impedance source.

### Input Through Buffer Amp

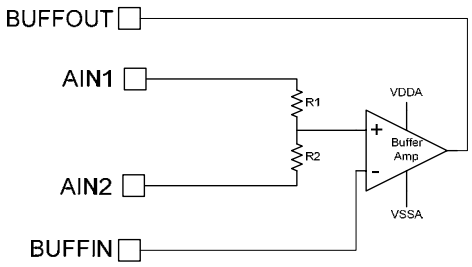
The HTADC12 has an integrated buffer amplifier which can be used to condition the input signal. The access to the amplifiers input pins and ability to create different circuits is dependent on the package option selected.

**14 Pin Package:** The buffer amplifier is configured as a unity gain amplifier with an input range of 0V to VREFIN. The output should then be connected directly to the VIN_ADC pin. R1 = R2 = 20k ohms.




**28 Pin Package:** With the 28 pin package, both input terminals and the output terminal of the amplifier are available. On the positive terminal, the AIN1 and AIN2 inputs are configured to allow the signal to be divided by 2 through a resistor divider (with either AIN1 or AIN2 connected to VSSA = 0V). This provides the ability to use signals from 0V to 5V. The negative input terminal and output are on separate pins allowing additional circuits to be created. The maximum output value shall be VREFIN. The internal resistor values are 20k ohms.

This output may then be connected to VIN ADC which has an input range of 0V to VREFIN (or 2.5V maximum). The output buffer may also be used as a unity-gain input buffer by applying the analog input to both AIN1 and AIN2.




### Tri-State Output Control

The digital outputs are tri-state drivers. They are controlled by the CE, NCS, and RNC. To have the outputs active, CE and RNC must be high and NCS must be low.

### RNC

The RNC signal is used to trigger an A-to-D Conversion by a high-to-low transition.

### STS

This signal is a status indicator for the validity of the output data. STS is high while a conversion is in progress.

### NAP

The NAP input may be used to put all analog circuitry except VREF into a low-current mode, saving power during inactive periods. Recovery time from NAP mode is <30µs. It is available only in the 14 pin DIP package.

| Absolute Maximum Rating[1] | | | | | |
|---|---|---|---|---|---|
| **Name** | **Parameter** | | **Min. Rating** | **Max. Rating** | **Units** |
| VDD | Supply Voltage[2] | | -0.5 | 6.0 | Volts |
| VPIN | Voltage on Any Pin[2] | | -0.5 | VDD+0.5 | Volts |
| TSTORE | Storage Temperature | | -55 | 300 | °C |
| IOUT | Average Output Current | | | 50 | mA |
| ESD | Electrostatic Discharge Protection Voltage[3] | | | 750 | V |
| PJC | Package Thermal Resistance (Junction-to-Case)<br>Package Thermal Resistance (Junction-to-Case) | 28 Pin DIP<br>14 Pin DIP | | 15 | °C/W |

*(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.*

*(2) Voltage referenced to VSS = 0V.*

*(3) Class 1 Electrostatic Discharge (ESD) input protection voltage per MIL-STD-883, Method 3015*

| Recommended Operating Conditions[1] | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Units** |
| VDD | Supply Voltage | 4.75 | 5.0 | 5.25 | Volts |
| TC | External Package Temperature | -55 | 25 | 225 | °C |
| Temp Op | Operating Temperature | -55 | | 225 | °C |
| VPIN | Voltage on Any Pin | -0.3 | | VDD +0.3 | Volts |
| VREFIN | Input Voltage Reference | 0.0V | | 2.5V | Volts |

*(1) Voltages referenced to VSS.*

| DC Electrical Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions[1] Limits:** | **Min.** | **Typ.** | **Max.** | **Units** |
| IDDA | VDDA Quiescent Current | NAP=0 (off), No external load on VREFOUT | | 2.5 | 5 | mA |
| IDD | VDD Quiescent Current | NAP=0 (off), No external load on VREFOUT | | 150 | 250 | µA |
| IDDA NAP | Quiescent Current VDDA | NAP=1 (on), No external load on VREFOUT | | 500 | 1000 | µA |
| IDD NAP | Quiescent Current VDD | NAP=1 (on), No external load on VREFOUT | | 150 | 250 | µA |
| IOZ | Output Tri-State Leakage | Output High Impedance | -5 | | +5 | uA |
| VIL | Low Level Input Voltage | Digital I/O signals | | | 20 | % of VDD (V) |
| VIH | High Level Input Voltage | Digital I/O signals | 80 | | | % of VDD (V) |
| VOH | High Level Output Voltage | Sourcing 4mA Current | VDD -0.5 | | | V |
| VOL | Low Level Output Voltage | Sinking 4mA Current | | | VSS + 0.5 | V |
| IIL | Input current at VIN=VSS | Digital I/O signals | -1 | | +1 | µA |
| IIH | Input current at VIN=VDD | Digital I/O signals | -1 | | +1 | µA |

*(1) Unless otherwise specified, specifications apply over the full operating temperature range from -55°C to 225°C, VDDA externally connected to VDD = 5V, VSSA externally connected to VSS = 0V.*

| Electrical Performance Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions[1] Limits:** | **Min.** | **Typ.** | **Max.** | **Units** |
| # of Bits | Resolution[2] | | | 12 | | Bits |
| INL | Integral Non-Linearity | | -2.8 | | +2.8 | LSB |
| DNL | Differential Non-Linearity | 28 Lead Package | -1.0 | | +1.8 | LSB |
| | | 14 Lead Package | -1.0 | | +1.96 | LBS |
| Offset | Offset Error | VIN value @ VOUT=Voltage equivalent to 0.0 (from Linear regression) LSB, T=25°C | -5 | 0 | +5 | LSB |
| OS_TC | Offset Error Tempco | VIN value @ VOUT=Voltage equivalent to 0.0 (from Linear regression) LSB, T=25°C | -5 | | +5 | ppm/°C |
| FS_ERR | Full Scale Calibration Error | Maximum Change in Full Scale Calibration VREFIN = 2.5V, T=25°C | -0.3 | | +0.3 | % of FS |
| FS_TC | FS Calibration Error Tempco | 28 Lead Package[5] Maximum Change in Full Scale Calibration VREFIN = 2.5V, T=25°C | -3 | | +3 | ppm/°C |
| | | 14 Lead Package[5] Maximum Change in Full Scale Internal VREFIN = 2.5V +/- 10mV, T=25°C | -7 | | +7 | ppm/°C |
| PSRA | Power Supply Rejection +4.75V ≤ VDDA ≤ 5.25V | Magnitude of Output Code | -1 | | 1 | LSB |
| PSRD | Power Supply Rejection +4.5V ≤ VDD ≤ 5.5V | Magnitude of Output Code | -1 | | 1 | LSB |
| VREFOUT | Reference Output Voltage | 55°C < T > 255°C | 2.49 | | 2.51 | V |
| ΔVRO-TIME | VREFOUT Drift with time | T = 255°C, .t = 1000 hours[2] | -3 | | +3 | mV |
| ΔVRo/ΔVDDA | VREFOUT Line Regulation-DC | VDDA = 5V ± 0.25V | -1 | | +1 | mV/V |
| ΔVRO/ΔIO | VREFOUT Load Regulation-DC | 0.0 mA ≤ Iout ≤ +8.0 mA[4] | | | 0.5 | mV/mA |
| VRN | VREFOUT Noise[2] | f = 0.1Hz to 10kHz | | 110 | | µV rms |
| TCONV | Conversion Time | | 9 | | 11.5 | µs |
| FSCLK | Serial Clock Frequency | $C_{load}$ = 10pF[3] | | | 40 | MHz |
| TWAKEUP | Wake-up time from NAP (ADC ready to convert) | | | 30 | | µs |
| VOSAA | Auxilliary Amplifier Input Offset Voltage | | -3 | ±1 | +3 | mV |
| BWAA | Auxilliary Amp Unity Gain Bandwidth[2] | $C_{load}$ = 40pf | 3 | 5 | | MHz |
| ΔR/R | Aux Amp Input Resistor Divider (/2) Matching[2] | | 0.1 | | +0.1 | % |

*(1) Unless otherwise specified, specifications apply over the full operating temperature range from -55°C to 225°C, VDDA externally connected to VDD = 5V, VSSA externally connected to VSS = 0V.*

*(2) Guaranteed by design.*

*(3) Maximum serial clock frequency listed is for a 10pF load on SDOUT. For greater capacitive loads, a lower clock frequency must be used. For $C_{load}$ = 100pF, Fsclk = 10 MHz is the recommended maximum.*

*(4) VREF_OUT can provide source current only.*

*(5) 28 Lead: This device is tested with an EXTERNAL Voltage Reference and therefore the reference is stable over temperature. Total Error = ADC error*

*14 Lead: This device uses the INTERNAL Voltage Reference and therefore impacts the overall FS TC of the ADC. Total Error = ADC error + Voltage Ref error*

# Functional Description

The A-to-D converter block consists of a 12-bit successive approximation analog-to-digital converter using an internal 12-bit capacitive charge re-distribution DAC. Conversions are initiated by a high-to-low transition on the RNC input. The analog input voltage range is from 0V to VREF_IN. While the conversion is in progress, the Status output (STS) is high and the parallel data outputs (D0 through D11) are in a high impedance state. When the conversion is complete, the data is made available on the parallel data output pins (D0 through D11). STS goes low approximately 1.5 clock cycles after the data is placed on the outputs, indicating that data is ready. A complete A/D conversion cycle requires 38 clock cycles. The nominal internal clock frequency is 4 MHz.

**ADC Clocking:** The internal A/D clock is nominally 4 MHz, and is approximately temperature and supply independent. At the nominal clock frequency the ADC throughput is approximately 100KSamples/sec.

**Voltage Reference Options:** The full-scale input range of the ADC is 0V to VREFIN. The 12-bit ADC has an internal, buffered reference source VREFOUT. VREFOUT is within 2.49V to 2.51V over all conditions (-55°C to +225°C). The reference buffer is designed to provide a low-impedance output capable of settling within the sampling time of the ADC when operated with the 4MHz clock.

**28 Pin Package:** To use this reference connect VREFOUT directly to VREFIN. Do not add decoupling capacitors at this connection. The capacitance on VREFOUT should be minimized. An external voltage reference may be used instead of the internal reference source. In that case, the external source may be connected directly to VREFIN and VREFOUT may be left un-connected.

**14 Pin Package:** VREFOUT is connected to VREFIN inside the package. No external reference can be used.

### ADC Converter Control

Four signals are used to control the ADC.

- Conversion Control: CE, NCS, and RNC
- Output Buffer Control: CE, NCS, and RNC
- Output Format: A0

### Conversion Control

It is recommended to use RNC as the signal to trigger the conversion and read functions. CE and NCS should be used as enables. Refer to timing diagrams.

However, the CE, NCS, and RNC have equivalent signal functions. A conversion can be initiated by a transition on the any of the control lines, as shown in the Truth Table.

Once a conversion is started, it can be terminated and restarted by reasserting the appropriate control lines.

**Truth Table**

| CE | NCS | RNC | A0 | Operation | Outputs |
|---|---|---|---|---|---|
| 0 | x | x | x | None | High Impedance |
| x | 1 | x | x | None | High Impedance |
| ⬆ | 0 | 0 | x | Initiate conversion | High Impedance |
| 1 | ⬇ | 0 | x | Initiate conversion | High Impedance |
| 1 | 0 | ⬇ | x | Initiate conversion | High Impedance |
| 1 | 0 | 1 | x | Enable serial output | Enabled |
| 1 | 0 | 1 | 0 | Enable 12-bit parallel output<br>(8 MSBs are read here when using 8-bit bus option) | Enabled |
| 1 | 0 | 1 | 1 | Enable 4 LSBs + 4 trailing zeroes, all super-imposed on 8 MSB outputs (8-bit bus option) | Enabled |

# Recommended Operating Modes

There are two main methods of operating the HTADC12, Open Loop and Closed Loop.

### Open Loop

The HTADC can also be used in an open loop mode in which the enable pins are held at a steady value and conversions are triggered by RNC. The output data is available and read when STS goes low. To trigger another conversion, only RNC has to be driven low.

*(1) CE is held high and NCS is held low.*

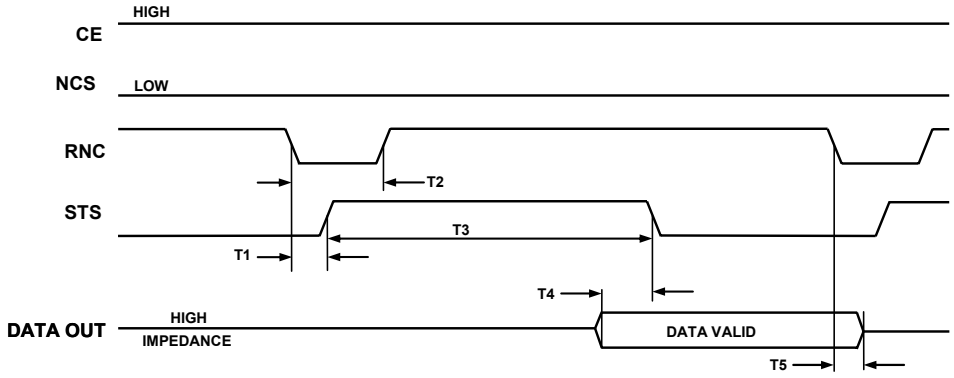
*(2) RNC is pulsed from a high to a low value which starts the conversion. RNC returns high before the conversion is completed.*

*(3) The STS signal will then go to a high value.*

*(4) When the conversion is complete, STS will go low indicating the data is available on the output bus.*

*(5) The next conversion is started with another pulse on the RNC line.*

| Open Loop Timing Diagram | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Units** |
| T1 | STS Delay From RNC | | | 100 | ns |
| T2 | Low RNC Pulse Width | 20 | | | ns |
| T3 | Conversion Time | 9 | 10 | 11.5 | µs |
| T4 | STS Delay After Data Buffer Turn-On | 50 | 80 | 110 | ns |
| T5 | High Z Delay After Disable | | | 20 | ns |



### Closed Loop – Processor Controlled

This mode requires control the input enable pins CE, NCS, and RNC. The STS signal will be used to notify the processor that a conversion is complete. The processor then changes the state of RNC to read the output data.

Assuming that CE is high and NCS is low, a typical conversion sequence might thus be:

*(1) CE and NCS are set to activate the device.*

*(2) RNC is then changed from a high to a low value which starts the conversion.*

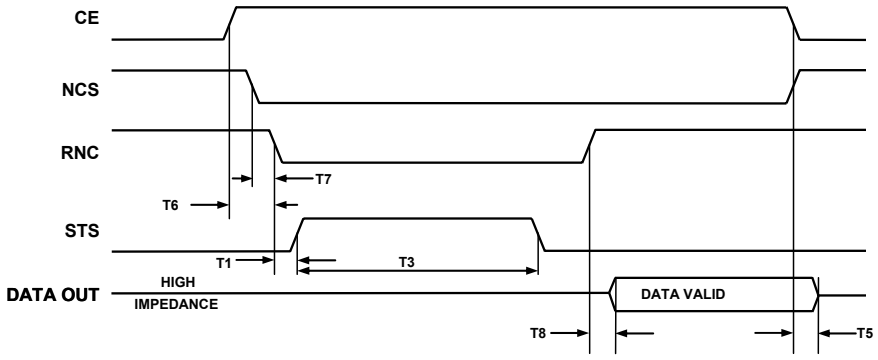
*(3) The STS signal will then go to a high value.*

*(4) When the conversion is complete, STS will go low. This will be detected by the processor/controller.*

*(5) The controller then sets RNC back to a high level and the signaling the data can be read at the outputs.*

*(6) Following the read, CE and NCS are then set to disable the device and putting the outputs into a high impedance state.*

| Closed Loop Timing Diagram | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Units** |
| T7 | Setup Time NCS To RNC | 0 | 5 | | ns |
| T6 | Setup Time CE To RNC | 0 | 5 | | ns |
| T1 | STS Delay From RNC | | | 100 | ns |
| T3 | Conversion Time | 9 | 10 | 11.5 | µs |
| T8 | READ Delay After Enable | | | 20 | ns |
| T5 | High Z Delay After Disable | | | 20 | ns |



**Data Output Formats:** There are three output formats: 12 bit parallel, two 8 bit parallel, and serial.

**28 Pin Package:** The parallel data can be presented as either 12 straight binary bits or configured for a "two-byte READ" for use with 8 bit processor busses.

**12-Bit Data Readout in 8-Bit Systems:** The HTADC12's 12-bit parallel data output can be read out by an 8-bit system in two 8-bit bytes. In this mode, the 8 MSB bit positions of the 12-bit output are utilized as the 8-bit bus.

Address control of the byte of interest is handled by the logic state of the A0 control line.

- When A0=0, the output data assumes its normal 12-bit format with bits D11-D4 of the 12-bit word forming the 1st data byte.
- When A0=1, bits D3-D0 followed by 4 logic zeroes are superimposed onto the 8 MSB bit positions, forming the 2nd data byte.

**Serial Output Control (14 Pin Package):** Conversions in the serial output mode are initiated identically to the parallel output mode described above. The serial data output, SDO, is enabled identically as well.

Valid data becomes available at SDO immediately at the end of the conversion cycle (slightly prior to STS). Data is output MSB first, and advances one bit position with each SCLK falling edge.

**Serial Output Timing Diagram**

| Data Output Pins | Data Output Values AO = 0 (READ bits D4 – D11) | AO = 1 (READ bits D0 – D3) |
|---|---|---|
| D11 | D11 | D3 |
| D10 | D10 | D2 |
| D9 | D9 | D1 |
| D8 | D8 | D0 |
| D7 | D7 | "0" |
| D6 | D6 | "0" |
| D5 | D5 | "0" |
| D4 | D4 | "0" |
| D3 | D3 | D3 |
| D2 | D2 | D2 |
| D1 | D1 | D1 |
| D0 | D0 | D0 |

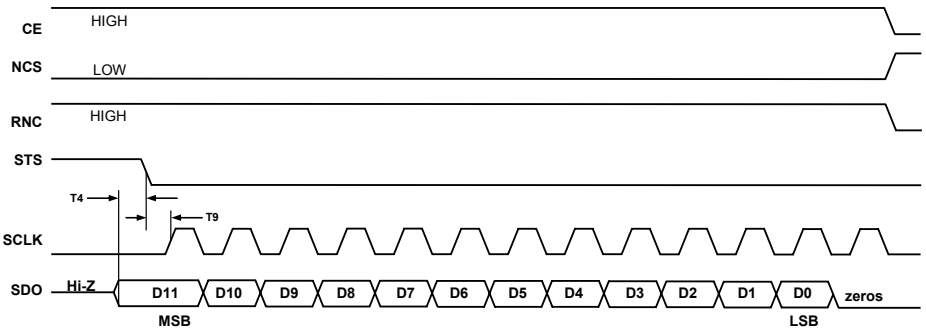
8 Bit Bus

Rising SCLK edges may be used to clock serial data into the master.

SCLK activity occurring other than when SDO is properly enabled for read is ignored.

**Serial Output Timing Diagram**

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| T4 | STS Delay After Data Buffer Turn-On | 50 | 80 | 110 | ns |
| T9 | Rising Edge of First Clock | 0 | | | ns |



# Switching Time

Delay time to achieve settled data when switching between the two data bytes will be dependent on the amount of load capacitance present on the output drivers. A general guideline for estimating the delay is given by the formula

$TD = 4.0\ ns + 0.25\ ns/pF \times C_L$

where TD is the delay time in ns, and $C_L$ is the capacitive load on each output driver in pF.

TD represents the total time required for an output driver's voltage level to fall to 10% of its previous logic high value, or to rise to 90% of its logic high value from a logic low, after A0 is asserted.

| Switching Time | |
|---|---|
| **Cload (pF)** | **Approximate TD (ns)** |
| 10 | 6.5 |
| 50 | 32.5 |
| 100 | 65.0 |

# Grounding and Decoupling

### Analog and Digital Grounding

Proper grounding is essential in any high speed, high-resolution system. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power schemes. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. While the HTADC12 features separate analog and digital power and ground pins, it should be treated as an analog component. The VSSA and VSS pins must be joined together directly under the HTADC12. A solid ground plane under the A/D is acceptable if the power and ground return currents are carefully managed. Alternatively, the ground plane under the A/D may contain serrations to steer currents in predictable directions where cross coupling between analog and digital would otherwise be unavoidable.

### Analog and Digital Driver Supply Decoupling

The HTADC12 features separate analog and digital supply and ground pins, helping to minimize digital corruption of sensitive analog signals.

In general, VDDA, the analog supply, should be decoupled to VSSA, the analog common, as close to the chip as physically possible.

# Reliability

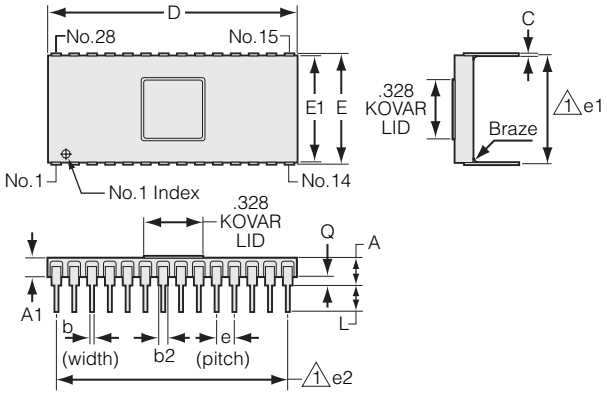
Honeywell understands the stringent reliability requirements that high temperature systems require and has extensive experience in reliability testing on programs of this nature. Reliability attributes of the SOI process were characterized by testing specially designed structures to evaluate failure mechanisms including hot carriers, electro-migration, and time-dependent dielectric breakdown. The results are fed back to improve the process to ensure the highest reliability products.

# Package Outline Dimensions (Inches)

### 28 Lead Package

4. EAR99 – This document does not contain technology or technical data as defined in EAR Part 772.
3. This case outline is based on package 58032697. The package number is printed in ceramic passte on the top surface.
2. Edges of package may be chamfered to prevent chipping.

1. Measured at stand off.

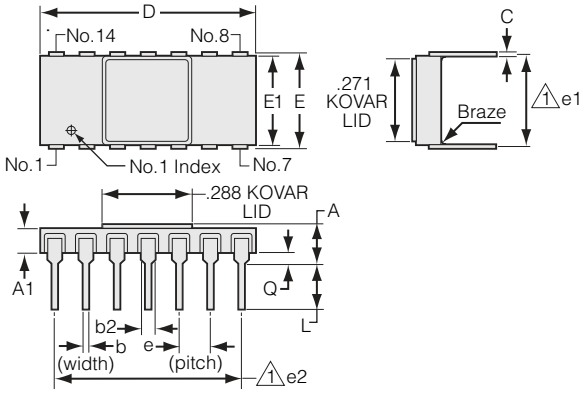



| 28 Lead Package | | | |
|---|---|---|---|
| **Symbol** | **Min.** | **Nom.** | **Max.** |
| A | .135 | .156 | .178 |
| A1 | .085 | .095 | .105 |
| b | .016 | .018 | .020 |
| b2 | .048 | .050 | .052 |
| C | .009 | .010 | .012 |
| D | 1.386 | 1.400 | 1.414 |
| E | .600 | .610 | .620 |
| E1 | .584 | .594 | .604 |
| e | .095 | .100 | .105 |
| e1 | --- | (6.00) | --- |
| e2 | 1.295 | 1.300 | 1.305 |
| L | --- | .150 Typ. | --- |
| Q | .040 | .050 | .060 |

### 14 Lead Package

4. EAR99 – This document does not contain technology or technical data as defined in EAR part 772.
3. This case outline is based on package 58032696. The package number is printed in ceramic paste on the top surface.
2. Edges of package may be chamfered to prevent chipping.

1. Measured at stand off.




| 14 Lead Package | | | |
|---|---|---|---|
| **Symbol** | **Min.** | **Nom.** | **Max.** |
| A | .107 | .126 | .146 |
| A1 | .072 | .080 | .088 |
| b | .016 | .018 | .020 |
| b2 | .045 | .047 | .049 |
| C | .008 | .010 | .012 |
| D | .692 | .700 | .708 |
| E | .300 | .310 | .320 |
| E1 | .285 | .295 | .305 |
| e | .095 | .100 | .105 |
| e1 | --- | (.300) | --- |
| e2 | .595 | .600 | .605 |
| L | --- | .150 Typ. | --- |
| Q | .025 | .035 | .045 |

### Ordering Information

| H | T | ADC | 12 | DCA |
|---|---|---|---|---|
| Source | Process | Part Type | Number of bits | Package |
| H = Honeywell | T = Hi Temp SOI | ADC = Analog to Digital Converter | | DCA = 28 pin DIP<br>DCB = 14 Pin DIP |

### Find Out More

For more information on Honeywell's High Temperature Electronics visit us online at www.honeywell.com/hightemp, or contact us at 800-323-8295 or 763-954-2474. Customer Service Email: ps.customer.support@honeywell.com.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