PI7C8150A: 32-bit 2-Port PCI-to-PCI Bridge

PRODUCT FEATURES

- 32-bit / 66MHz primary and secondary ports
- Compliant with the following specifications:
  - *PCI Local Bus Specification, Revision 2.2*
  - *PCI-to-PCI Bridge Architecture Specification, Revision 1.1*
  - *Advanced Configuration Power Interface* (ACPI) *Specification*
  - *PCI Power Management Specification, Revision 1.0*
- Concurrent primary and secondary port operation
- Provides internal arbitration for one set of 9 secondary bus masters
  - Programmable 2-level priority arbiter
  - Disable control to allow use of an external arbiter
- Supports posted write buffers in both directions (downstream and upstream)
- Two 128-byte FIFO's for delay transactions
- Two 128-byte FIFO's for posted memory transactions
- Enhanced address decoding
  - 32-bit I/O address range
  - 32-bit memory-mapped I/O address range
  - VGA addressing and VGA palette snooping
  - ISA-aware mode for legacy support in the first 64KB of I/O address range
- IEEE 1149.1 JTAG interface support
- 3.3V core; 3.3V and 5V PCI I/O interface
- Packages
  - 208-pin QFP
  - 256-pin PBGA
- Available in 66MHz and 33MHz
- Intel 21150 compatible

PRODUCT DESCRIPTION

The PI7C8150A is a 2-port PCI-to-PCI Bridge designed to be fully compliant with the *PCI Local Bus Specification, Revision 2.2.* Both the primary and secondary ports are specified to run at 32-bit and up to 66MHz.

The PI7C8150A supports synchronous bus transactions between devices on the primary bus and the secondary bus. The two buses can operate in concurrent mode, resulting in added increase in system performance. Concurrent bus operation off-loads and isolates traffic on a single bus by allowing a master and target on the same bus to communicate with each other while the other bus is busy.

The *PCI Local Bus Specification* denotes loading restrictions on the PCI bus. The PI7C8150A allows designers to expand the loading capability by adding a second PCI bus. On motherboards, more PCI slots or devices can then be added on this second PCI bus. On add-in cards, more than one device can now reside on the add-in card (*PCI Local Bus Specifications* specify that each add-in card may only have one device because there may only be one connection per PCI signal in the add-in card connector).

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE
PI7C8150AMA	66 MHz	208-FQFP
PI7C8150AMA-33	33 MHz	208-FQFP
PI7C8150AND	66 MHz	256-PBGA
PI7C8150AND-33	33 MHz	256-PBGA

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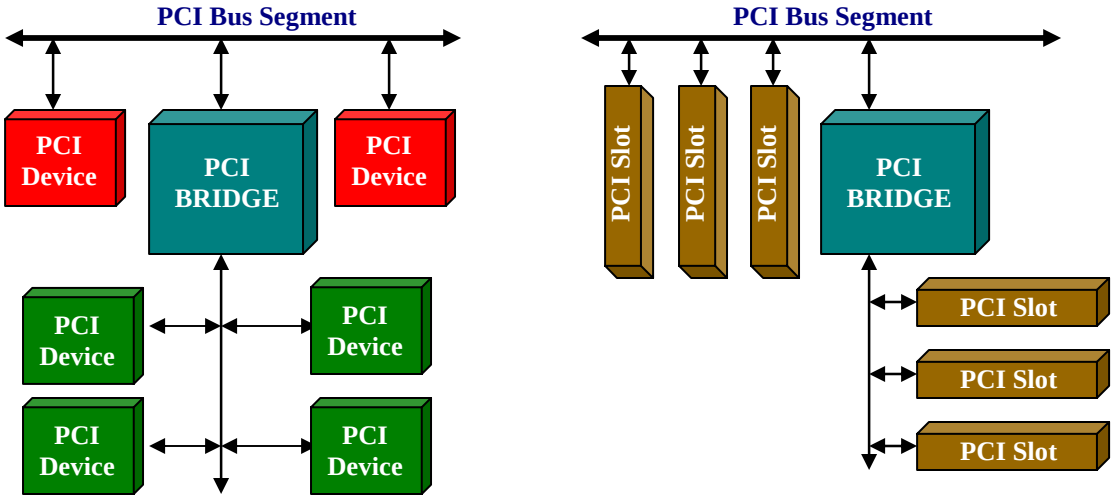
PI7C8150A PIN INFORMATION

P_AD[31:0] ←→	PRIMARY BUS INTERFACE	SECONDARY BUS INTERFACE	←→ S_AD[31:0]
P_CBE[3:0] ←→			←→ S_CBE[3:0]
P_PAR ←→			←→ S_PAR
P_FRAME_L ←→			←→ S_FRAME_L
P_IRDY_L ←→			←→ S_IRDY_L
P_DEVSEL_L ←→			←→ S_DEVSEL_L
P_TRDY_L ←→			←→ S_TRDY_L
P_STOP_L ←→			←→ S_STOP_L
P_LOCK_L →			←→ S_LOCK_L
P_IDSEL →			← S_IDSEL
P_REQ_L ←			← S_REQ[8:0]_L
P_GNT_L →			→ S_GNT[8:0]_L
P_SERR_L ←			← S_SERR_L
P_PERR_L ←→			←→ S_PERR_L
P_RESEST_L →			→ S_RESEST_L
P_VIO →			← S_VIO
P_CLK →	CLOCK INTERFACE	MISCELLANEOUS INTERFACE	← MS0
S_CLKIN →			← MS1
MSK_IN →			← S_CFN_L
S_CLKOUT[9:0] →			←→ GPIO[3:0]
			← BPCCE
P_M66EN →	CONTROL INTERFACE	JTAG INTERFACE	← TMS
S_M66EN ←→			← TCK
CFG66 →			← TDI
			→ TDO
			← TRST_L

APPLICATION EXAMPLE

BUS EXPANSION

A PCI Bus Segment has electrical loading limitations and/or slot limitations. A PCI Bridge can expand the PCI Bus Ssegment to enable more loads or slots to be added to the



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