# EMIF06-SD03F3

## 6-line IPAD™, EMI filter and ESD protection for SD card

## Features

- ESD protection (IEC standard)
- EMI Filtering
- Level translator
- Signal conditionning
- Integrated power supply with:
  - Thermal shutdown (TSD)
  - Under voltage lockout (UVLO)
  - Short-circuit current limitation ($I_{SC}$)
  - Power on/off feature with Enable pin

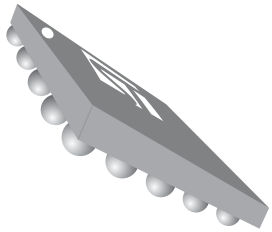
### Benefits

- EMI Low-pass-filter and ESD protection (up to 15 kV on external pins)
- Integrated pull up resistors prevent bus floating
- 50 MHz clock frequency compatible with $C_{line}$< 40 pF
- Lead-free package in 400 µm pitch
- Low power consumption
- Very low PCB space consumption
- High reliability offered by monolithic integration
- Reduction of parasitic elements thanks to CSP integration

### Complies with the following standards:

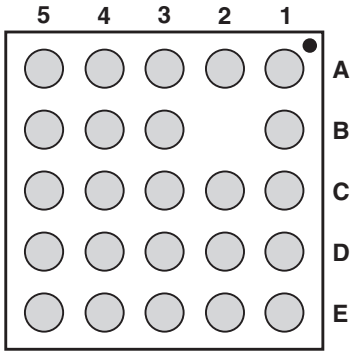
- IEC 61000-4-2, Level 4: External pins
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- HBM IEC 61340-3-1: All pins
  - 2 kV (air discharge)
  - 2 kV (contact discharge)

TM: IPAD is a trademark of STMicroelectronics.



**Flip Chip**
**(24 bumps)**

**Figure 1. Pin configuration (bump side)**




## Applications

- Removable memory cards in mobile phones, communication systems, and portable applications
- Memory cards compliant with: SD (standard and high speed), MiniSD, µSD and MMC/Trans-flash standards

## Description

The EMIF06-SD03F3 is a highly integrated device, based on IPAD technology, combining the 5 functions described under *Features*.

# Contents

# 1 Functional description

### A SIDE (Host-CPU) pin list:

$V_{ccA}$, Enable, Dat123.dir, CMD.dir, CMD.h, CLK.h, CLK -f, Dat0.dir, Dat0.h, Dat1.h, Dat2.h, Dat3.h, $V_{bat}$

### B SIDE (SD-Card) pin list:

WP, CD, $V_{ccB}$, CMD-B, CLK-B, Dat0-B, Dat1-B, Dat2-B, Dat3-B

**Table 1. Pin definition**

| Pin name | Bump | Type | Side | Description |
|---|---|---|---|---|
| $V_{ccA}$ | B3 | Power input | A | Power supply (1.8v) |
| $V_{ccB}$ | B4 | Power output | B | Power supply (internally generated, 2.9 V) |
| $V_{bat}$ | A4 | Power input | A | Battery power supply |
| GND | C4 | Ground | - | Ground |
| GND | C3 | Ground | - | Ground |
| Enable | C2 | Input | A | Internal power supply enable |
| CMD.dir | A2 | Input | A | Command direction |
| CMD.h | D2 | IO | A | A side command |
| CLK.h | C1 | Input | A | Clock input |
| CLK-f | E2 | Output | A | Clock feedback |
| Dat0.dir | A3 | Input | A | Data direction |
| Dat0.h | D1 | IO | A | Data host |
| Dat123.dir | E3 | Input | A | Data direction |
| Dat1.h | E1 | IO | A | Data host |
| Dat2.h | A1 | IO | A | Data host |
| Dat3.h | B1 | IO | A | Data host |
| WP | E4 | Input to CPU | A | Write protect |
| CD | D3 | Input to CPU | A | Card detect |
| CMD-B | D4 | IO | B | Command direction |
| CLK-B | C5 | Output | B | Clock output |
| Dat0-B | D5 | IO | B | Data SD |
| Dat1-B | E5 | IO | B | Data SD |
| Dat2-B | A5 | IO | B | Data SD |
| Dat3-B | B5 | IO | B | Data SD |

*Note: In Table 5, 6, 7, and 10, collective names are used for groups of pins. The names used are:*

**.dir = CMD.dir, Dat0.dir, Dat123.dir*
**.h = CMD.h, CLK.h, Dat0.h, Dat1.h, Dat2.h, Dat3.h*
**-B = CMD-B, CLK-B, Dat0-B, Dat1-B, Dat2-B, Dat3-B*
*$V_{iA}$ = All A side input pins*
*$V_{iB}$ = All B side input pins.*

**Table 2. Function table**

| Command signals | | | | A side signals direction | | | | | B side signal direction | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Enable | CMD. dir | Dat0.dir | Dat123.dir | CMD.h | CLK.h | CLK-f | Dat0.h | Dat1.h Dat2.h Dat3.h | CMD-B | CLK-B | Dat0-B | Dat1-B Dat2-B Dat3-B |
| H | H | X | X | IN | IN | OUT | X | X | OUT | OUT | X | X |
| H | L | X | X | OUT | IN | OUT | X | X | IN | OUT | X | X |
| H | X | H | X | X | IN | OUT | IN | X | X | OUT | OUT | X |
| H | X | L | X | X | IN | OUT | OUT | X | X | OUT | IN | X |
| H | X | X | H | X | IN | OUT | X | IN | X | OUT | X | OUT |
| H | X | X | L | X | IN | OUT | X | OUT | X | OUT | X | IN |
| L | X | X | X | X | X | Z | X | X | L* | Z | L* | L* |

*Note: 1 When A side signals direction is INPUT, SD-CARD is WRITTEN by CPU-Host (i.e B side signals direction is OUTPUT)*
*When A side signals direction is OUTPUT, SD-CARD is READ by CPU-Host (i.e B side signals direction is INPUT)*

*2 For B side signals when Enable = L:*
** Defined by internal pull-down (see Figure 3 for pins CMD.B and data bus Dat[0…3].B)*

**Figure 2. Configuration**

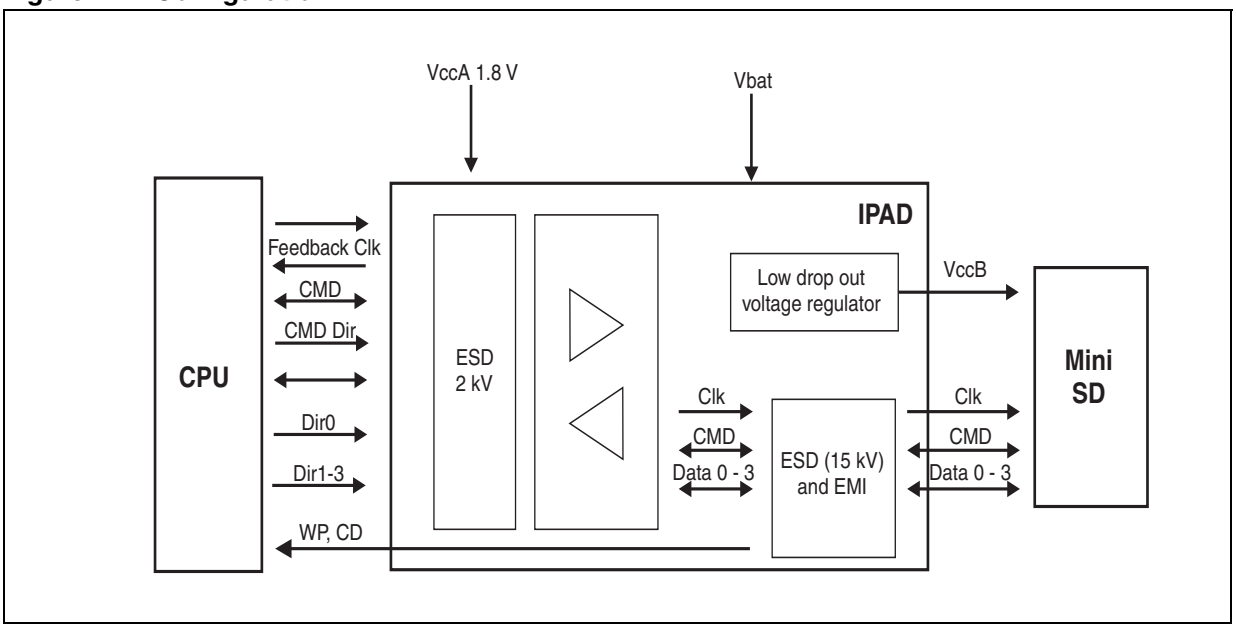
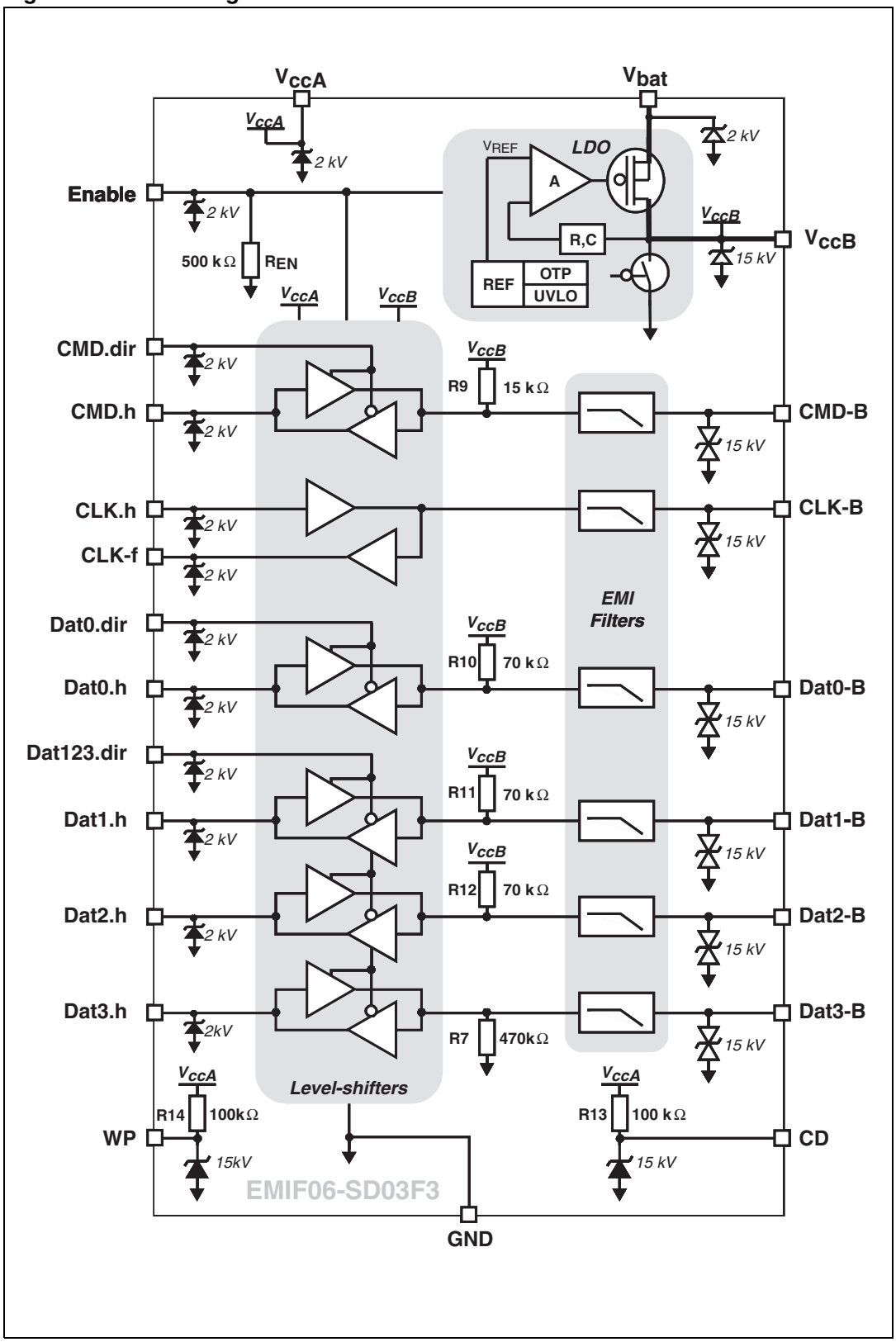


**Figure 3. Block diagram**



# 2 Characteristics

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| ESD | **A SIDE (Host-CPU)**<br>**All pins: HBM IEC61340-3-1**<br>$V_{ccA}$, Enable, Dat123.dir, CMD.dir, CMD.h, CLK.h, CLK -f, Dat0.dir, Dat0.h, Dat1.h, Dat2.h, Dat3.h, $V_{bat}$ | Air discharge<br>Contact discharge | 2<br>2 | kV |
| | **B SIDE (SD-Card)**<br>**External pins : IEC 61000-4-2, level 4**<br>$V_{ccB}$, CMD-B, CLK-B, Dat0-B, Dat1-B, Dat2-B, Dat3-B, WP, CD | Air discharge<br>Contact discharge | 15<br>8 | |
| $T_{jmax}$ | Maximum junction temperature | | 150 | °C |
| $R_{th\ (j-a)}$ (1) | Thermal resistance from junction to ambient<br>Board: Epoxy FR4, copper thickness = 40 µm, 4 layers | | 64 | °C/W |
| $P_{dmax}$ | Maximum power dissipation:<br>$P_{dmax}$= ($T_{jmax}$ - $T_{aopmax}$)/ Rth (j-a) | | 1 | W |
| $T_{stg}$ | Storage temperature range | | -55 to +150 | °C |
| Voltage | $V_{bat}$, $V_{ccB}$, Enable | | -0.3 to 5.5V | V |
| | CMD-B, CLK-B, Dat0-B, Dat1-B, Dat2-B, Dat3-B | | -0.3 to $V_{ccB}$ + 0.3 | |
| | $V_{ccA}$ | | -0.3 to 3.3 | |
| | Dat123.dir, CMD.dir, CMD.h, CLK.h, CLK -f, Dat0.dir, Dat0.h, Dat1.h, Dat2.h, Dat3.h, WP, CD | | -0.3 to $V_{ccA}$+0.3 | |

1. $V_{ccB}$ is an internally generated power supply, no external voltage should be applied on this pin other than a current clamp. The thermal resistance depends on printed circuit board layout. To dissipate the heat efficiently away from Flip Chip bumps, it is better to make copper planes the largest possible as well as considering thermal vias usage.

**Table 4. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{ccA}$ | Power supply | | 1.62 | 1.8 | 1.92 | V |
| $V_{bat}$ | Battery power supply | | 3.1 | - | 5 | V |
| $I_{out}$ | $V_{ccB}$ output current | | 0.10 | 100 | 200 | mA |
| $C_{bat}$ | External battery capacitance | Ceramic capacitor | - | 2.20 | - | µF |
| $C_{out}$(1) | External output capacitance | $T_a$ = -40 °C to +85 °C, $V_{bias}$ = 0 V to 3.3 V Multi-layer ceramic capacitor type like: C20RX7R1C225K | 1.4 (-35%) | 2.20 | 3.0 (+35%) | µF |
| ESR(2) | Equivalent series resistance for $C_{out}$ | F = 1 Hz to 10 MHz Multi-layer ceramic capacitor type like: C2012X7R1C225KT | - | 3 | 200 | mΩ |
| $T_{aop}$ | Ambient operating temperature | | -30 | 25 | 85 | °C |
| $T_{jop}$ | Juntion operating temperature | | -30 | 25 | 125 | °C |
| $P_{dop}$ | Maximum power dissipation | $P_{dop} = (T_{jop} - T_{aop})/R_{th\ (j-a)}$ | - | - | 625 | mW |
| Enable | Enable input voltage | | 0 | - | $V_{ccA}$ | V |
| External pins (without WP and CD) | CMD-B, CLK-B, Dat0-B, Dat1-B, Dat2-B, Dat3-B | | 0 | - | $V_{ccB}$ | V |
| Internal pins (except Enable, with WP and CD) | WP, CD, Dat123.dir, CMD.dir, CMD.h, CLK.h, CLK-f, Dat0.dir, Dat0.h, Dat1.h, Dat2.h, Dat3.h | | 0 | - | $V_{ccA}$ | V |

1. $C_{out}$ = 2.2 µF is minimum allowable capacitance value to guarantee LDO stability
2. Values for ESR include the $V_{ccB}$ - $C_{out}$ resistance path and $C_{out}$ - GND resistance path. These resistance paths need to be minimized in PCB design.

**Table 5. LDO - current levels in recommended operating conditions**

| Symbol | Parameter | Test conditions(1) | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{Q\_OFF}$ | Quiescent current consumption $I_{ccA\_OFF}$ | $V_{EN}$ = 0.4 V, $V_{bat}$ = 3.4 V, $V_{ccA}$ = 1.92 V<br>*.dir, *.h, *-B = GND, WP = CD = $V_{ccA}$<br>All other pins floating | | - | - | 1 | µA |
| | Quiescent current consumption $I_{bat\_OFF}$ | $V_{EN}$ = 0.4 V, $V_{bat}$ = 5 V, $V_{ccA}$ = 1.92 V<br>*.dir, *.h, *-B = GND<br>All other pins floating | | - | - | 1 | µA |
| $I_{Q\_ON}$ | Quiescent current consumption (Ground pin current) $I_{bat}$ + $I_{ccA}$ | Level shifter disactivated<br>*.dir = 0 V, $V_{bat}$ = 3.4 V<br>$V_{EN}$ = $V_{ccA}$ = $V_{CLK.h}$ = 1.8 V<br>All other pins floating | $I_{out}$ = 100 µA | - | 160 | 220 | µA |
| | | | $I_{out}$ = 50 mA | - | 320 | 375 | µA |
| | | | $I_{out}$ = 100 mA | - | 470 | 550 | µA |
| | | | $I_{out}$ = 200 mA | - | 750 | 900 | µA |

1. See *Note: on page 3* for definition of collective names of pins, for example *.dir

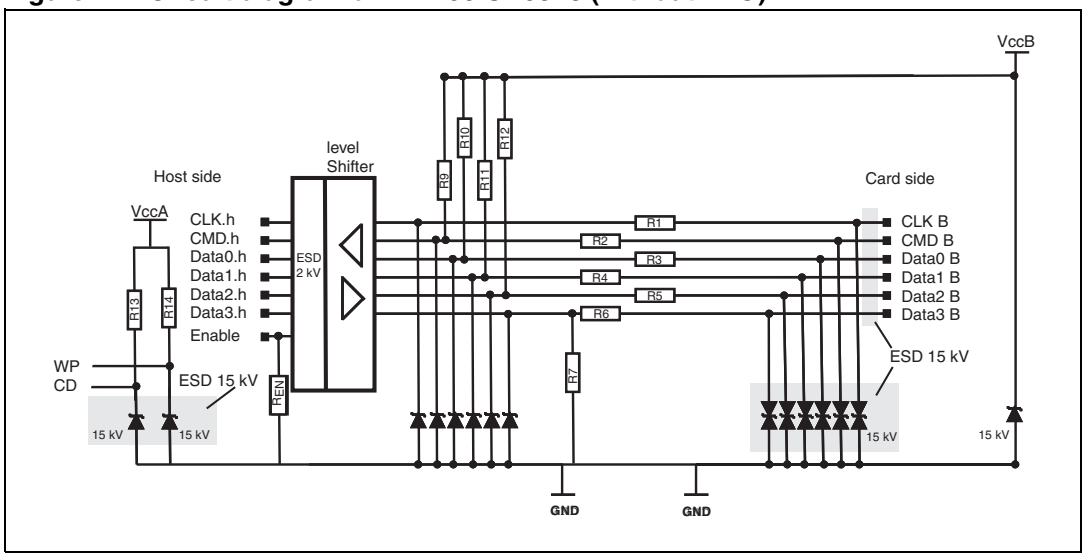
**Table 6. Level shifter - current levels in recommended operating conditions**

| Symbol | Parameter | Test conditions(1) | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{ccA\_ON}$ | Quiescent current on $V_{ccA}$ | $V_{EN}$ = $V_{ccA}$ = 1.92 V, $V_{bat}$ = 3.4 V<br>*.dir = $V_{ccA}$, ViA = *.h = $V_{ccA}$ | - | 3 | 10 | µA |
| $I_{ccB\_ON}$ | Quiescent current on $V_{ccB}$ | $V_{EN}$ = $V_{ccA}$ = 1.92 V, $V_{bat}$ = 3.4 V<br>*.dir = 0 V, $V_{ccB}$ = 3.05 V, ViB = $V_{ccB}$ | - | 15 | 30 | µA |

1. See *Note: on page 3* for definition of collective names of pins, for example *.dir

# 3 Passive integration and low pass filter

**Figure 4. Circuit diagram of EMIF06-SD03F3 (without LDO)**




*Note: $V_{BR}$ in 14 V technology for pins: CMD-B, CLK-B, Dat0-B, Dat1-B, Dat2-B, Dat3-B, WP, CD*
*$V_{BR}$ in 8 V technology for pins: Vcc-B, CLK.h, CLK-f, CMD.h, Dat0.h, Dat1.h, Dat2.h, Dat3.h*

**Table 7. Components**

| Symbol | Parameter | Test conditions(1) | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{in-A}$ | Input capacitance for A side | $V_{bat}$ = 3.4 V, *.dir = $V_{EN}$ = $V_{ccA}$<br>F = 1 MHz, $V_{dc}$ = 0 V, ±30 mV, $V_{AC}$ = 30mV | - | 5 | 10 | pF |
| $C_{in-B}$ | Input capacitance for B side | $V_{bat}$ = 3.4 V, *.dir = GND, $V_{EN}$ = $V_{ccA}$<br>F = 1 MHz, $V_{dc}$ = 0 V, ±30 mV, $V_{AC}$ = 30mV | - | 25 | 35 | pF |
| $C_{EMIF}$ | Capacitance seen on B side from EMIF filter | | - | 15 | - | pF |
| R1, R2, R3, R4, R5, R6(2) | EMIF resistors(3) | $T_j$ = 25 °C | - | 40 | - | Ω |
| $R_{line}$ | Line resistance | at 20 mA | 40 | 50 | 60 | Ω |
| R10, R11, R12 | EMIF resistors(4) | $T_j$ = 25 °C | 49 | 70 | 91 | kΩ |
| R9 | EMIF resistor(4) | $T_j$ = 25 °C | 10.5 | 15 | 19.5 | kΩ |
| R7 | EMIF resistor(4) | $T_j$ = 25 °C | 329 | 470 | 611 | kΩ |
| R13 | EMIF resistor(4) | $T_j$ = 25 °C | 70 | 100 | 130 | kΩ |
| R14 | EMIF resistor(4) | $T_j$ = 25 °C | 70 | 100 | 130 | kΩ |
| $R_{EN}$ | resistor(4) | $T_j$ = 25 °C | - | 500 | - | kΩ |

1. See *Note: on page 3* for definition of collective names of pins, for example *.dir
2. These values are guaranteed by design and statistical process control.
3. 20% tolerance in resistance value
4. 30% tolerance in resistance value

**Figure 5. Frequency response with level shifters internally bypassed(1)**

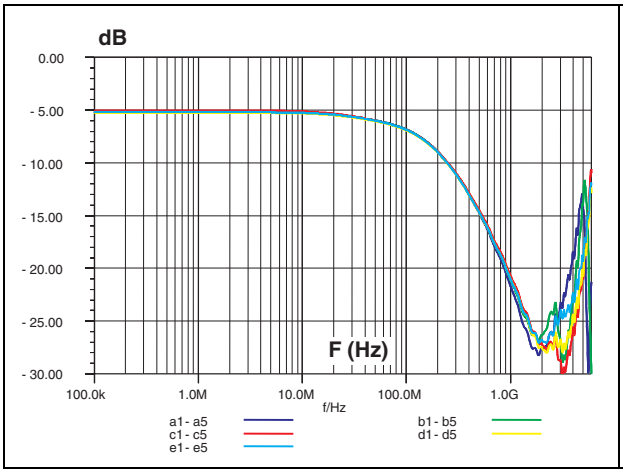
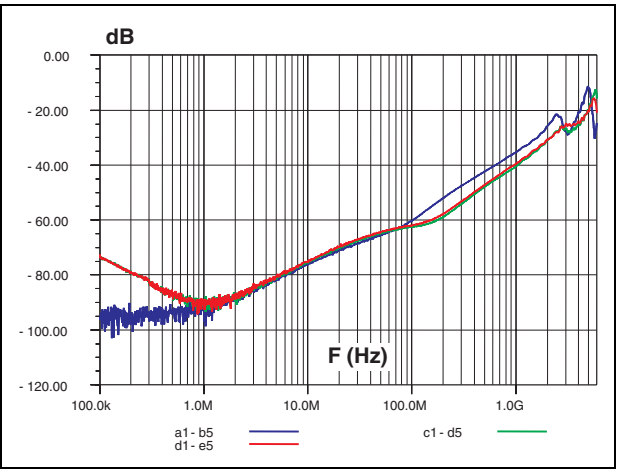



**Figure 6. Crosstalk response with level shifters internally bypassed(1)**




1. Measurement in 50 Ω environment

# 4 Data transmission

All values in the tables below are guaranteed across the operating temperature and voltage range unless otherwise specified.

**Table 8. DC voltage levels on host side**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IHA}$ | High level input voltage | | 0.65 x $V_{ccA}$ | $V_{ccA}$ | - | V |
| $V_{ILA}$ | Low level input voltage | | 0 | 0 | 0.35 x $V_{ccA}$ | V |
| $V_{OHA}$ | High level output voltage | $I_{oh}$ = -6 mA | $V_{ccA}$ - 0.45 | - | - | V |
| $V_{OLA}$ | Low level output voltage | $I_{ol}$ = 7 mA | - | 0 | 0.45 | V |

**Table 9. DC voltage levels on SD side**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IHB}$ | High level input voltage | | 0.7 x $V_{ccB}$(1) | $V_{ccB}$ | - | V |
| $V_{ILB}$ | Low level input voltage | | - | 0 | 0.3 x $V_{ccB}$(1) | V |
| $V_{OHB}$ | High level output voltage | $I_{oh}$ = -8 mA | $V_{ccB}$(1) - 0.7 | 2.9 | - | V |
| $V_{OLB}$ | Low voltage output voltage | $I_{ol}$ = 8 mA | - | 0 | 0.7 | V |

1. $V_{ccB}$ is defined in power supply block.

**Table 10. DC current levels**

| Symbol | Parameter | Test conditions(1) | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{LH}$ | Leakage current on host pin | $V_{EN}$ = *.dir = $V_{ccA}$ = 1.92 V, $V_{iA}$ = $V_{ccA}$ or GND, $V_{bat}$ = 3.4 V | - | - | 5 | µA |
| $I_{LSD}$ | Leakage current on SD pin | $V_{bat}$ = 3.4 V, $V_{CLK.h}$ = $V_{ccA}$, $V_{CMD}$ = $V_{Dat0}$ = $V_{Dat1}$ = $V_{Dat2}$ = $V_{ccB}$ $V_{Dat3}$ = *.dir = GND | - | - | 5 | µA |
| $I_{SCH}$ | Short circuit current on host side | SD input = H, host= 0 V SD input = 0 V, host = $V_{ccA}$ = 1.8 V *.dir = 0 V, $V_{bat}$ = 3.4 V, $T_j$ = 25 °C | - | 25 | - | mA |
| $I_{SCSD}$ | Short circuit current on SD side | Host input = H, SD = 0 V Host input= L, SD = $V_{ccB}$, $T_j$ = 25 °C *.dir = $V_{ccA}$ = 1.8 V, $V_{bat}$ = 3.4 V | - | 60 | - | mA |

1. See *Note: on page 3* for definition of collective names of pins, for example *.dir

**Figure 7. Symbol definitions of $t_{plh}$, $t_{phl}$, $t_r$ and $t_f$ for AC characteristics in *Table 11***

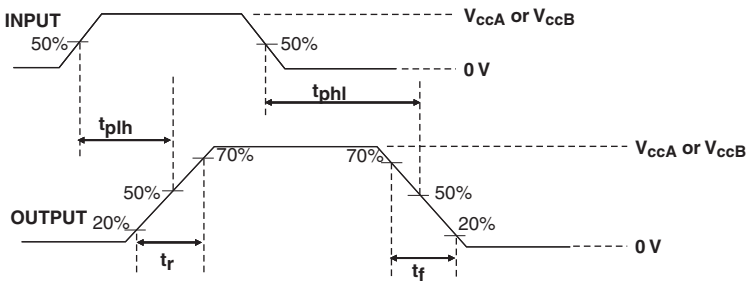



**Table 11. AC characteristics(1)**

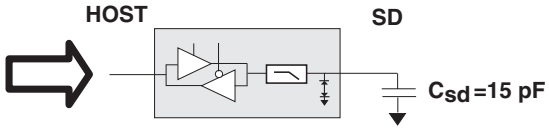
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{phl}$ | Propagation delay hl from host to SD | *Section 4.1* | - | 3.5 | 6 | ns |
| $t_{plh}$ | Propagation delay lh from host to SD | | - | 3.5 | 6 | |
| $t_{phl}$ | Propagation delay hl from SD to host | *Section 4.2* | - | 3 | 6 | ns |
| $t_{plh}$ | Propagation delay lh from SD to host | | - | 3 | 6 | |
| $t_r$ | Rise time from host to SD | *Section 4.1* | - | 1.5 | 3 | ns |
| | Rise time from SD to host | *Section 4.2* | - | 0.5 | 2 | |
| $t_f$ | Fall time from host to SD | *Section 4.1* | - | 1.9 | 3 | ns |
| | Fall time from SD to host | *Section 4.2* | - | 0.5 | 2 | |
| $t_{skew}$ | Delay differences from host to SD | *Section 4.1*,*Section 4.3* | -1.0 | 0 | 1.0 | ns |
| $t_{skew.f}$ | $t_{skew}$ delay from SD to host | *Section 4.2*, *Section 4.4* | -1.5 | 0 | 1.5 | ns |
| $t_{p\_clkf}$ | Propagation delay for CLK feedback | | - | 6.5 | 12 | ns |
| $t_{r\_clkf}$ | Rise time for CLK feedback | *Section 4.2* | - | 0.5 | 2 | ns |
| $t_{f\_clkf}$ | Fall time for CLK feedback | *Section 4.2* | - | 0.5 | 2 | ns |

1. $T_{aop}$ -30 to 85 °C, $I_{out}$ = 1 mA, $C_{bat}$ = 2.2 µF, $C_{out}$ = 2.2 µF

## 4.1 Test circuit from host to SD

Test circuit from host to SD is shown in *Figure 8*. Timings are measured for the whole line cell (shifter + EMI + ESD) on an external load $C_{sd}$ = 15 pF (board capacitance 5 pF + SD card capacitance 10 pF).

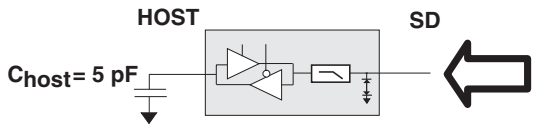
**Figure 8. Test circuit from host to SD**



## 4.2 Test circuit from SD to host

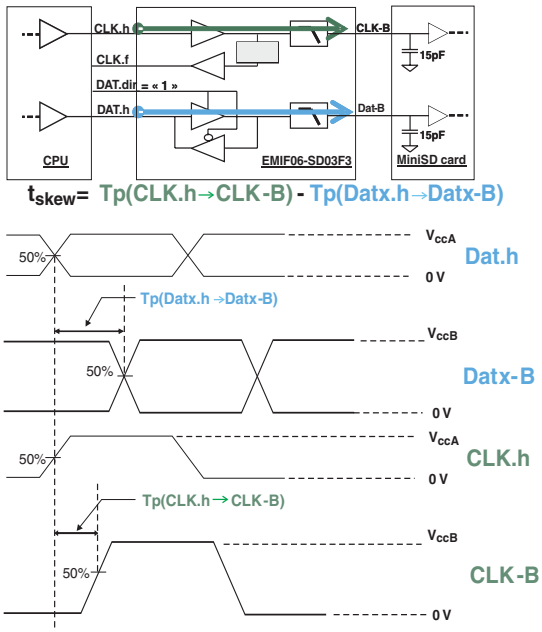
Test circuit from SD to host is shown in *Figure 9*. Timings are measured for the whole line cell (shifter + EMI + ESD) on an external load $C_{host}$ = 5 pF (board capacitance + host capacitance).

**Figure 9. Test circuit from SD to host**



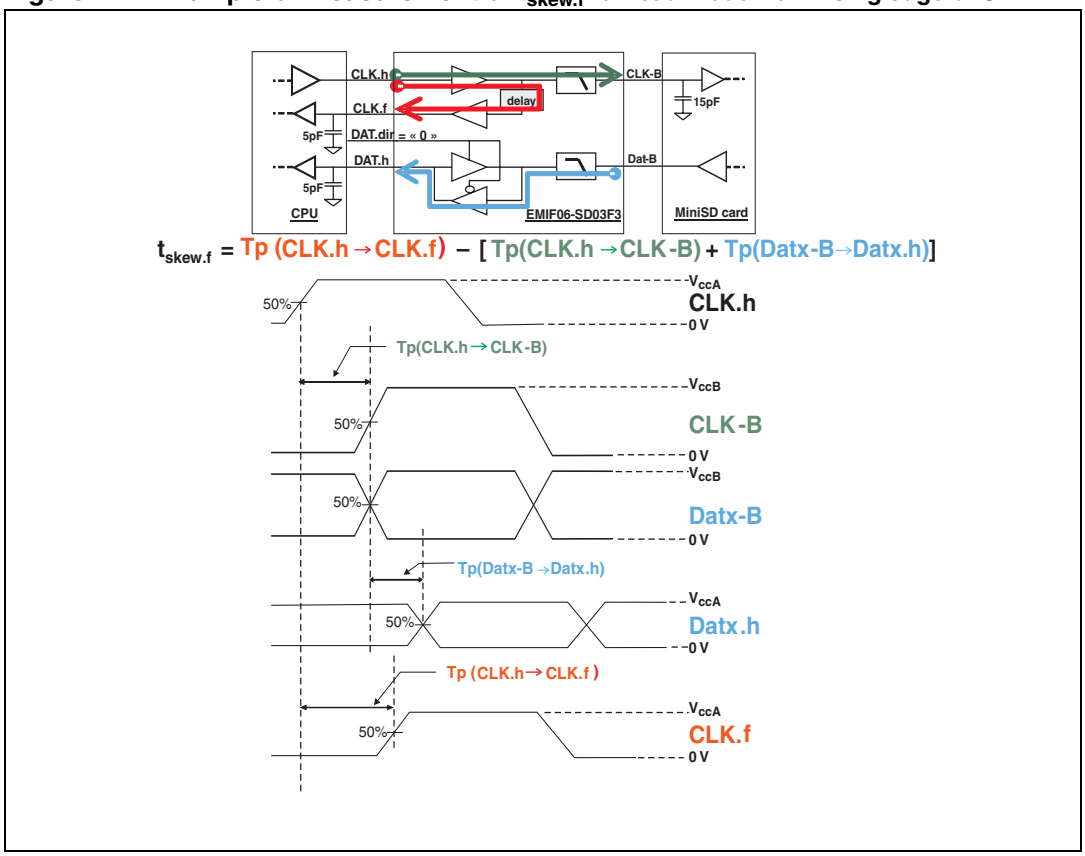

## 4.3 Measurement of $t_{skew}$ (host to SD) from rising edge CLK.h

**Figure 10. Example of measurement of $t_{skew}$ (host to SD) from rising edge of CLK.h**



## 4.4 Measurement of $t_{skew.f}$ (read mode) from rising edge CLK.h

**Figure 11. Example of measurement of $t_{skew.f}$ for read mode from rising edge of CLK.h**




Datx.h = Dat0.h, Dat1.h, Dat2.h, Dat3.h, CMD.h

Datx-B = Dat0-B, Dat1-B, Dat2-B, Dat3-B, CMD.B

# 5 Low drop out voltage regulator

**Figure 12. Low drop out voltage regulator**

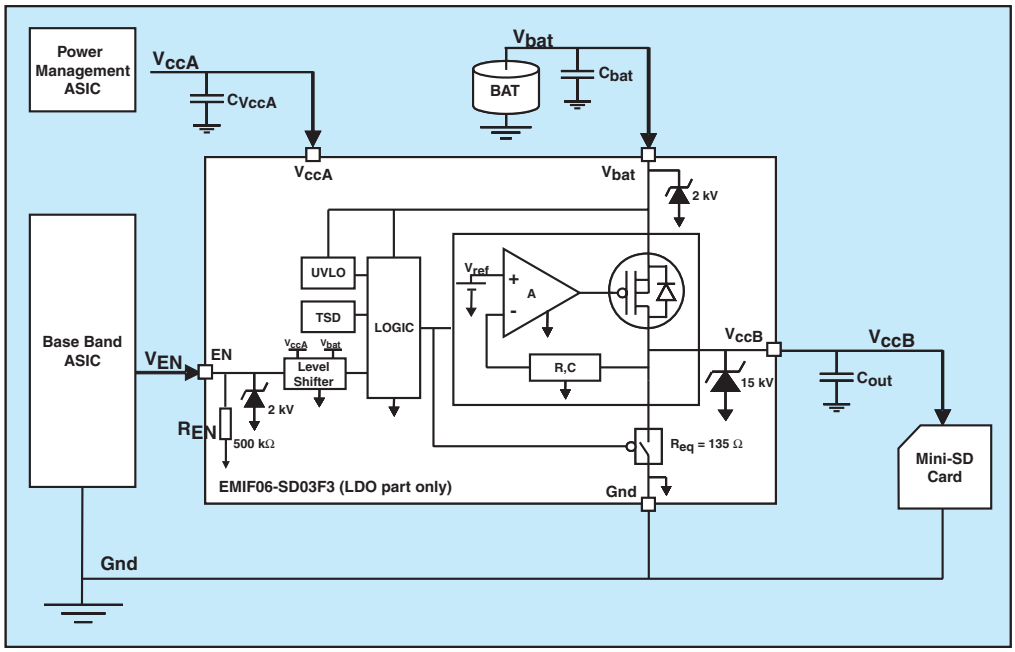


**Table 12. Static parameters, $V_{EN} = V_{ccA}$ unless otherwise specified(1)**

| Symbol | Parameter | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{out}$ | Regulated output voltage ($V_{ccB}$) | $V_{bat}$ = 3.4 V, $I_{out}$ = 100 mA, $T_j$ = 25 °C | | 2.81 (-3%) | 2.90 | 2.99 (+3%) | V |
| | | $V_{bat}$ = 3.4 V, $I_{out}$ = 100 mA, $T_j$ = -30 to 125 °C | | 2.81 (-3%) | - | 2.99 (+3%) | V |
| | | $V_{bat}$ = 3.1 to 5 V, $I_{out}$ = 0.1 to 200 mA, $T_j$ = -30 to 125 °C | | 2.75 (-5%) | - | 3.05 (+5%) | V |
| LiR | Line regulation | $V_{bat}$ = 3.4 to 5 V (*Section 5.1*), $I_{out}$ = 100 mA, $T_j$ = 25 °C | | - | 3 | 20 | mV |
| LdR | Load regulation | $V_{bat}$ = 3.4 V, $I_{out}$ = 1 to 200 mA (*Section 5.2*), $T_j$ = 25 °C | | - | 50 | 100 | mV |
| $V_{DO}$ | Dropout voltage | $V_{out}$(nom) - 100 mV (*Section 5.3*), $T_j$ = -30 to 85 °C | $I_{out}$ = 50 mA | - | 25 | 37 | mV |
| | | | $I_{out}$ = 100 mA | - | 50 | 75 | mV |
| | | | $I_{out}$ = 200 mA | - | 100 | 150 | mV |
| $I_{SC}$ | Short circuit current limitation | $V_{bat}$ = 5 V, $V_{out}$ = 0 V, $T_j$ = 25 °C | | - | 500 | - | mA |
| TSD | Thermal shutdown temperature | $V_{bat}$ = 3.4 V | Shutdown (Temp ↑) | - | 150 | - | °C |
| | | | Reset (Temp ↓) | - | 130 | - | °C |
| | | | Hysteresis | - | 20 | - | °C |
| UVLO | Under voltage lockout | $T_j$ = -30 to 125 °C | Shutdown ($V_{bat}$ ↓) | 2.3 | 2.5 | 2.7 | V |
| | | | Reset ($V_{bat}$ ↑) | 2.35 | 2.55 | 2.75 | V |
| | | | Hysteresis | - | 50 | - | mV |

1. Level shifter disactivated, *.dir = 0, CLK.h = $V_{ccA}$ , all other pins floating.

**Table 13. Dynamic parameters ($V_{EN}$ = $V_{ccA}$ unless otherwise specified)**

| Symbol | Parameter | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| LiTr | Line transient peak voltage | $V_{bat}$ = 3.4 V ↑↓ 4 V, $t_{tr}$ = 30 µs, $I_{out}$ = 200 mA<br>$T_j$ = 25 °C (*Section 5.1*)<br>$C_{out}$ = 2.2 µF, ESR = 5 mΩ | | - | 4.2 | - | mV |
| LdTr | Load transient peak voltage | $I_{out}$ = 1 mA ↑↓ 200 mA, $t_{tr}$ = 10 µs, $V_{bat}$ = 3.4 V<br>$T_j$ = 25 °C (*Section 5.2*)<br>$C_{out}$ = 2.2 µF, ESR = 5 mΩ | | - | 9 | - | mV |
| PSRR | Power supply rejection ratio | $V_{bat}$ = 3.4 V, $I_{out}$ = 100 mA,<br>$T_j$ = 25 °C, $C_{out}$ = 2.2 µF,<br>ESR = 5 mΩ | F = 1 kHz | - | 45 | - | dB |
| | | | F = 10 kHz | - | 35 | - | dB |
| $t_{start}$ | Settling time | $V_{out}$ ↑ 95% Nom, $V_{bat}$ = 5 V, $I_{out}$ = 200 mA<br>$T_j$ = -30 °C to 125 °C, $C_{out}$ = 2.2 µF,<br>Enable L → H | | - | 30 | 200 | µs |
| $t_{stop}$ | Discharge time | $V_{out}$ ↓ 10% Nom, $V_{bat}$ = 3.4 V, $I_{out}$ = 1 mA<br>$T_j$ = 25 °C, $C_{out}$ = 2.2 µF, Enable H → L | | - | 600 | - | µs |

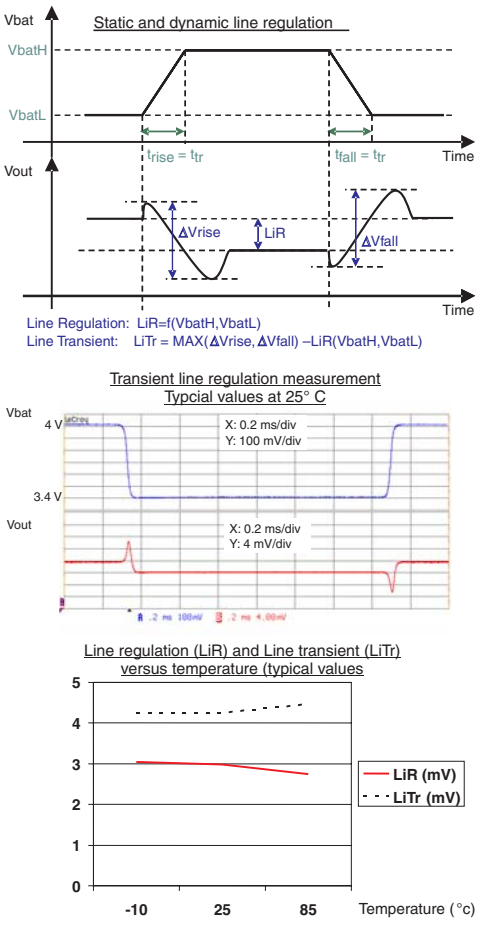
## 5.1 Line regulation and transient line regulation

The line regulation (LiR) is a static variable that indicates the change in the output voltage of the voltage controller $\Delta V_{out}$ (at constant load) when there is a change $\Delta V_{bat}$ at the input voltage. By contrast the line transient response (LiTr) represents dynamic peak value to be observed during the change in input voltage

Thermal effects due to changes in the junction temperature are circumvented with pulsed voltage during the test and are to be taken into account separately.

The figure shows the boundary conditions for $t_{rise}$, $t_{fall}$, and $\Delta V_{bat}$ to be taken as the basis of the measurement of the line transient response without additional decoupling of the supply voltage by a buffer capacity $C_{bat}$. The values defined in the specification apply, however, only in the case of decoupling of the supply voltage with such a capacity $C_{bat}$, as a result of which the values for $t_{rise}$ and $t_{fall}$ are influenced to some extent.

**Figure 13. Line regulation and transient line regulation**



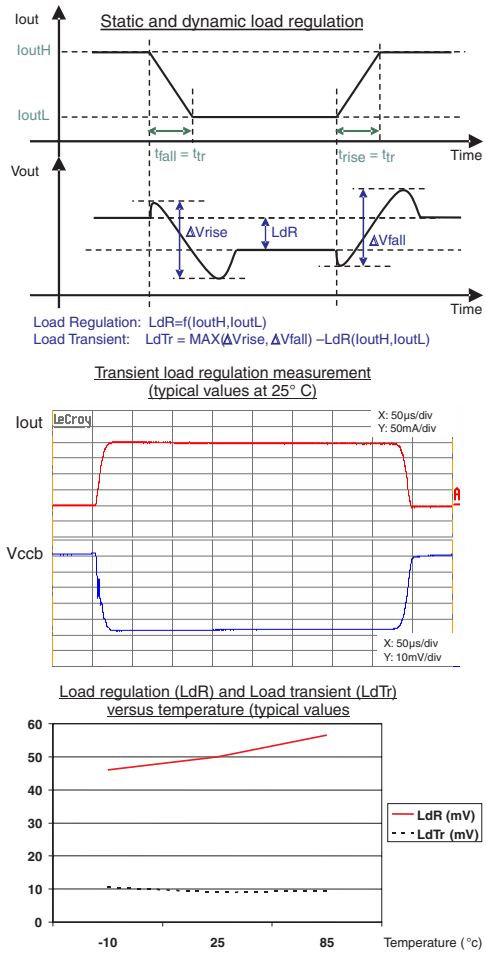
## 5.2 Load regulation and transient load regulation

The load regulation (LdR) is a static variable that indicates the change in output voltage of the voltage controllor $\Delta V_{out}$ (at constant input voltage) in the event of a change in the load current $\Delta I_{out}$. By contrast the load transient response (LdTr) represents the dynamic peak value to be observed during load variation.

Thermal effects due to changes in the junction temperature are circumvented by testing with pulsed load and are to be taken into account separately.

The figure shows the boundary conditions for $t_{rise}$, $t_{fall}$, and $\Delta I_{out}$ to be taken as the basis for the measurement of the load transient response.

**Figure 14. Load regulation and transient load regulation**

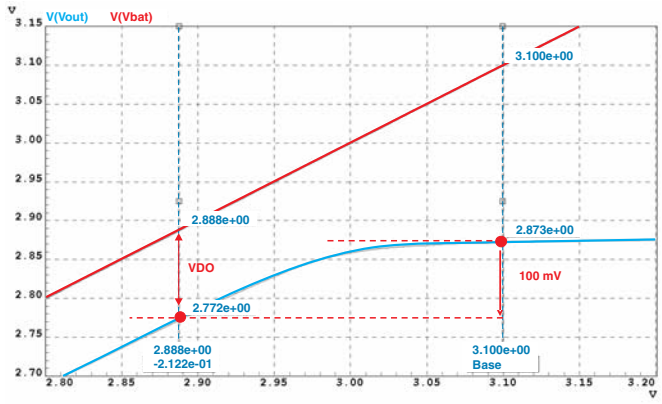


## 5.3 Dropout definition

The dropout voltage ($V_{DO}$) is measured by decreasing the input voltage till the output voltage will drop by 100 mV compared to the output voltage measured at the specified minimum supply voltage (3.1 V).

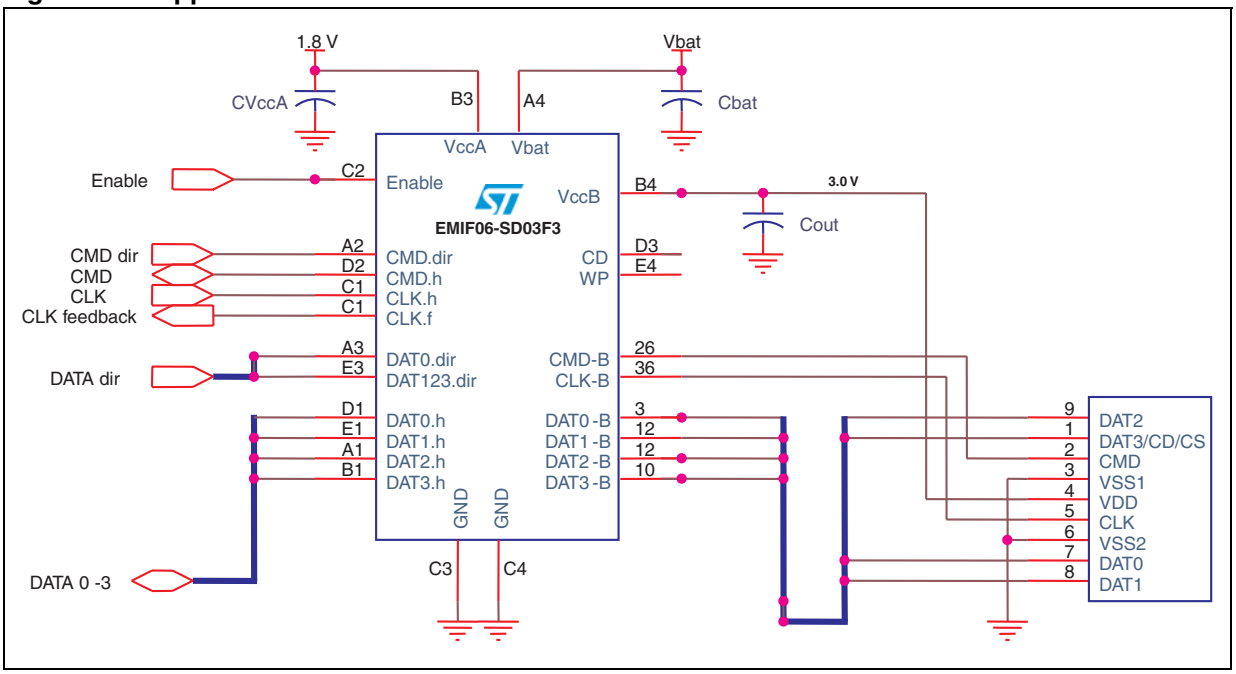
Worst case for dropout is maximum die temperature and maximum current load. This is done statically.

**Figure 15. Dropout definition**



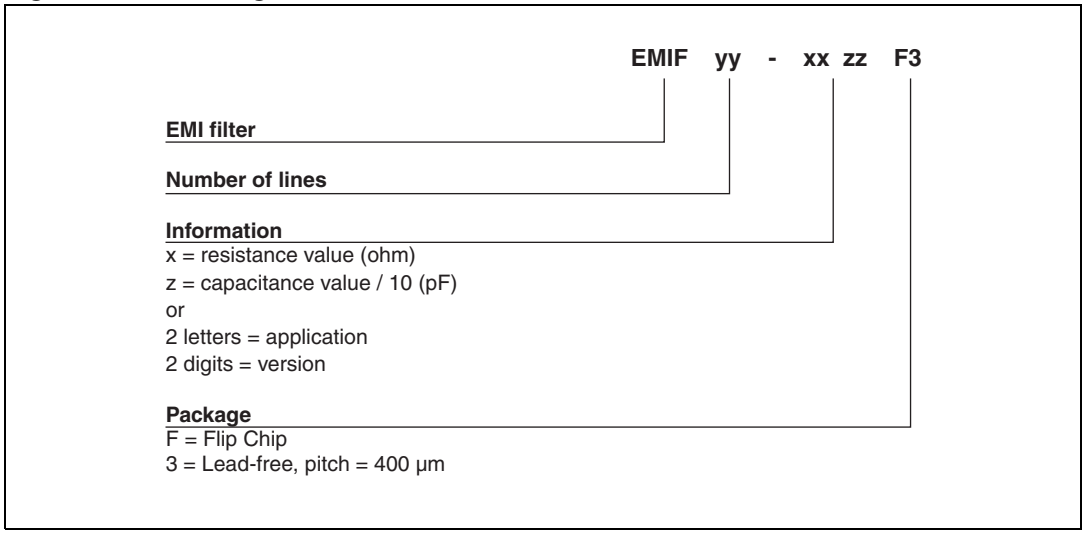

# 6 Application schematic

**Figure 16. Application schematic**



# 7 Ordering information scheme

**Figure 17. Ordering information scheme**




# 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

**Figure 18. Flip Chip dimensions**

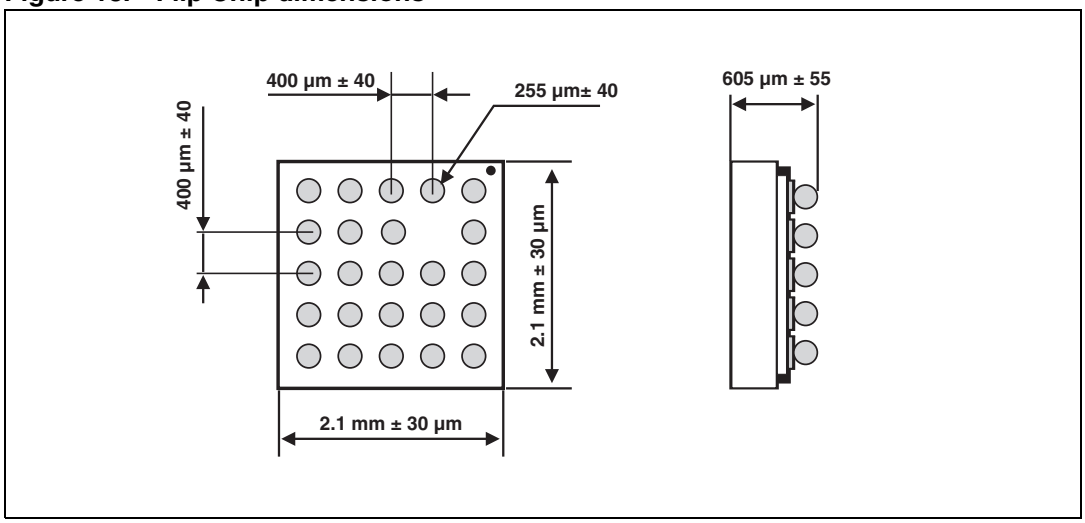


**Figure 19. Footprint recommendations**

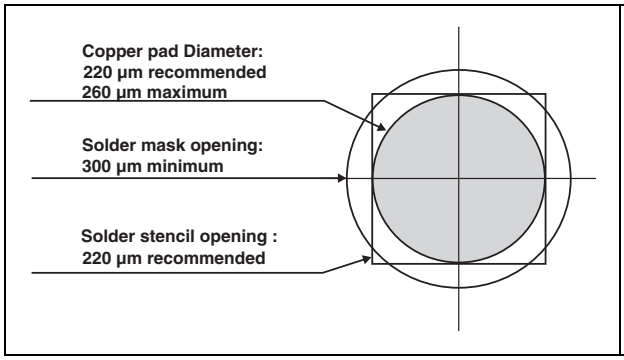



**Figure 20. Marking**

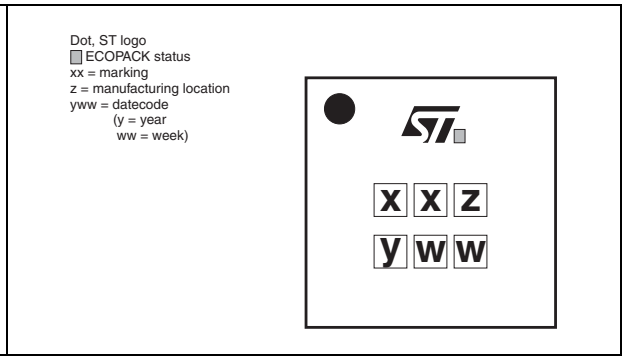
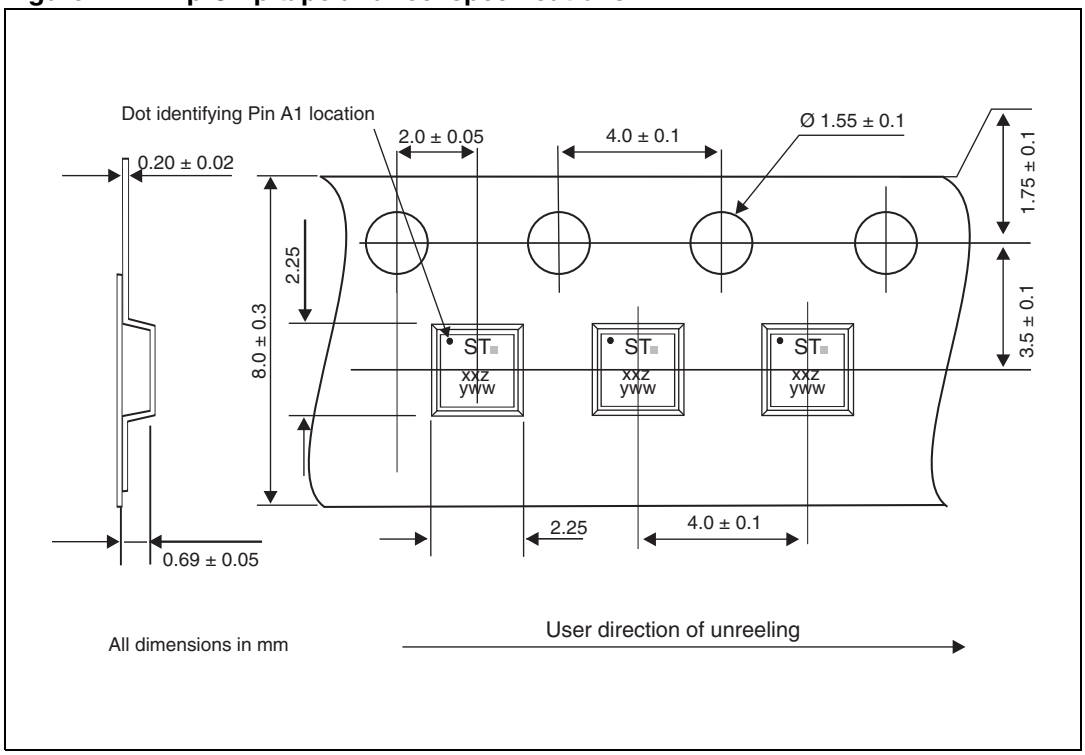



**Figure 21. Flip Chip tape and reel specifications**




# 9 Ordering information

**Table 14. Ordering information**

| Order code | Marking | Package | Weight | Base qty | Delivery mode |
|---|---|---|---|---|---|
| EMIF06-SD03F3 | HY | Flip Chip | 5.46 mg | 5000 | Tape and reel (7") |

*Note: More information is available in the application notes:*
*AN2348 :"Flip Chip : Package description and recommendations for use"*
*AN1751 : EMI Filters: Recommendations and measurements*

# 10 Revision history

Table 15. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 21-Nov-2008 | 1 | First issue |
| 11-Feb-2010 | 2 | AC timing characteristics updated in *Table 11*. |

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.



STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

**www.st.com**