

# 74LVC2G126-Q100

Bus buffer/line driver; 3-state

Rev. 2 — 14 December 2016

Product data sheet

## 1. General description

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The 74LVC2G126\_Q100 is a dual non-inverting buffer/line driver with 3-state outputs. An output enable input (pin nOE) controls each 3-state output. A LOW-level at pin nOE causes the output to assume a high-impedance OFF-state. Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of the 74LVC2G126\_Q100 as a translator in a mixed 3.3 V and 5 V environment.

It is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - ◆ JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\text{ }\Omega$ )
- $\pm 24\text{ mA}$  output drive ( $V_{CC} = 3.0\text{ V}$ )
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC2G126DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G126DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

### 4. Marking

Table 2. Marking codes

Type number	Marking code <sup>[1]</sup>
74LVC2G126DP-Q100	V26
74LVC2G126DC-Q100	V26

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram

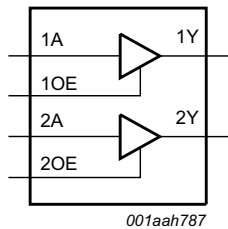


Fig 1. Logic symbol

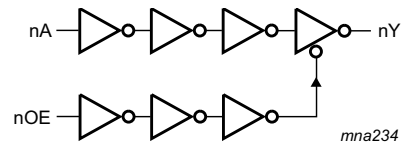


Fig 2. Logic diagram (one gate)

### 6. Pinning information

#### 6.1 Pinning

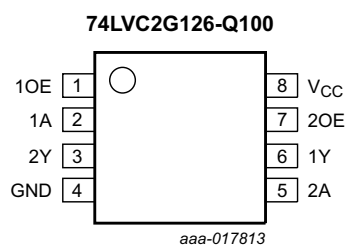


Fig 3. Pin configuration SOT505-2 and SOT765-1

## 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 7	output enable input (active HIGH)
1A, 2A	2, 5	data input
1Y, 2Y	6, 3	data output
GND	4	ground (0 V)
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

Table 4. Function table<sup>[1]</sup>

Input		Output
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
V <sub>I</sub>	input voltage		[1] -0.5	+6.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA
V <sub>O</sub>	output voltage	Active mode	[1] -0.5	V <sub>CC</sub> + 0.5	V
		Power-down mode	[1][2] -0.5	+6.5	V
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub>	supply current		-	+100	mA
I <sub>GND</sub>	ground current		-100	-	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[3] -	300	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V<sub>CC</sub> = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 packages: above 55 °C, the value of P<sub>tot</sub> derates linearly at 2.5 mW/K.  
For VSSOP8 packages: above 110 °C, the value of P<sub>tot</sub> derates linearly at 8.0 mW/K.

## 9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	Active mode	0	$V_{CC}$	V
		$V_{CC} = 0$ V; Power-down mode	0	5.5	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	10	ns/V

## 10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$T_{amb} = -40$ °C to +85 °C						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
		$V_{CC} = 4.5$ V to 5.5 V	$0.7 \times V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100$ $\mu$ A; $V_{CC} = 1.65$ V to 5.5 V	-	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 1.65$ V	-	-	0.45	V
		$I_O = 8$ mA; $V_{CC} = 2.3$ V	-	-	0.3	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	-	0.4	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	-	0.55	V
		$I_O = 32$ mA; $V_{CC} = 4.5$ V	-	-	0.55	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100$ $\mu$ A; $V_{CC} = 1.65$ V to 5.5 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -4$ mA; $V_{CC} = 1.65$ V	1.2	-	-	V
		$I_O = -8$ mA; $V_{CC} = 2.3$ V	1.9	-	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	-	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.3	-	-	V
		$I_O = -32$ mA; $V_{CC} = 4.5$ V	3.8	-	-	V

**Table 7. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to $5.5 \text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = 5.5 \text{ V}$ or GND; $V_{CC} = 3.6 \text{ V}$	-	$\pm 0.1$	$\pm 2$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 5.5 \text{ V}$ ; $V_{CC} = 0 \text{ V}$	-	$\pm 0.1$	$\pm 2$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V}$ to $5.5 \text{ V}$ ; $I_O = 0 \text{ A}$	-	0.1	4	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per pin; $V_I = V_{CC} - 0.6 \text{ V}$ ; $I_O = 0 \text{ A}$ ; $V_{CC} = 2.3 \text{ V}$ to $5.5 \text{ V}$	-	5	500	$\mu\text{A}$
$C_I$	input capacitance		-	2	-	pF
<b><math>T_{amb} = -40 \text{ }^\circ\text{C}</math> to <math>+125 \text{ }^\circ\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65 \text{ V}$ to $1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V}$ to $2.7 \text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7 \text{ V}$ to $3.6 \text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5 \text{ V}$ to $5.5 \text{ V}$	$0.7 \times V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65 \text{ V}$ to $1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V}$ to $2.7 \text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7 \text{ V}$ to $3.6 \text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5 \text{ V}$ to $5.5 \text{ V}$	-	-	$0.3 \times V_{CC}$	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100 \mu\text{A}$ ; $V_{CC} = 1.65 \text{ V}$ to $5.5 \text{ V}$	-	-	0.1	V
		$I_O = 4 \text{ mA}$ ; $V_{CC} = 1.65 \text{ V}$	-	-	0.70	V
		$I_O = 8 \text{ mA}$ ; $V_{CC} = 2.3 \text{ V}$	-	-	0.45	V
		$I_O = 12 \text{ mA}$ ; $V_{CC} = 2.7 \text{ V}$	-	-	0.60	V
		$I_O = 24 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	-	-	0.80	V
		$I_O = 32 \text{ mA}$ ; $V_{CC} = 4.5 \text{ V}$	-	-	0.80	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100 \mu\text{A}$ ; $V_{CC} = 1.65 \text{ V}$ to $5.5 \text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4 \text{ mA}$ ; $V_{CC} = 1.65 \text{ V}$	0.95	-	-	V
		$I_O = -8 \text{ mA}$ ; $V_{CC} = 2.3 \text{ V}$	1.7	-	-	V
		$I_O = -12 \text{ mA}$ ; $V_{CC} = 2.7 \text{ V}$	1.9	-	-	V
		$I_O = -24 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	2.0	-	-	V
		$I_O = -32 \text{ mA}$ ; $V_{CC} = 4.5 \text{ V}$	3.4	-	-	V
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to $5.5 \text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = 5.5 \text{ V}$ or GND; $V_{CC} = 3.6 \text{ V}$	-	-	$\pm 2$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 5.5 \text{ V}$ ; $V_{CC} = 0 \text{ V}$	-	-	$\pm 2$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V}$ to $5.5 \text{ V}$ ; $I_O = 0 \text{ A}$	-	-	4	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per pin; $V_I = V_{CC} - 0.6 \text{ V}$ ; $I_O = 0 \text{ A}$ ; $V_{CC} = 2.3 \text{ V}$ to $5.5 \text{ V}$	-	-	500	$\mu\text{A}$

[1] Typical values are measured at  $V_{CC} = 3.3 \text{ V}$  and  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 6](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA to nY; see <a href="#">Figure 4</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	3.9	9.8	1.0	12.3	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	2.6	4.9	0.5	6.3	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.8	4.7	1.0	5.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	2.4	4.3	0.5	5.4	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.9	3.2	0.5	4.0	ns
t <sub>en</sub>	enable time	nOE to nY; see <a href="#">Figure 5</a> <sup>[3]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	4.1	10.0	1.0	12.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.6	5.0	1.0	6.3	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.8	4.7	1.0	5.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.4	4.1	1.0	5.1	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.8	3.1	0.5	3.9	ns
t <sub>dis</sub>	disable time	nOE to nY; see <a href="#">Figure 5</a> <sup>[4]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	3.3	12.6	1.0	15.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	1.9	5.7	0.5	7.5	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.0	4.8	1.5	6.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.5	4.4	1.0	5.7	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.8	3.3	0.5	4.4	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[5]</sup>						
		output enabled	-	17	-	-	-	pF
		output disabled	-	5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>

[3] t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>

[4] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>

[5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

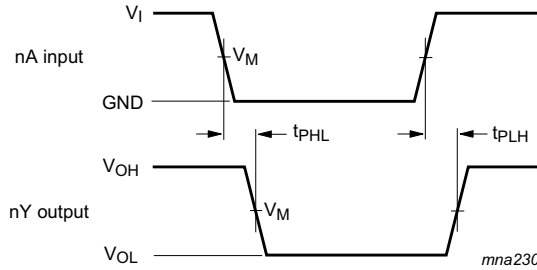
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

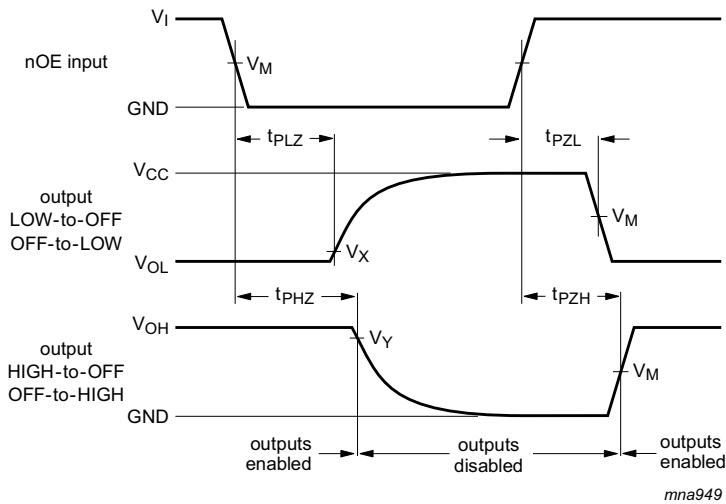
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

12. Waveforms



Measurement points are given in [Table 9](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 4. The data input (nA) to output (nY) propagation delays**

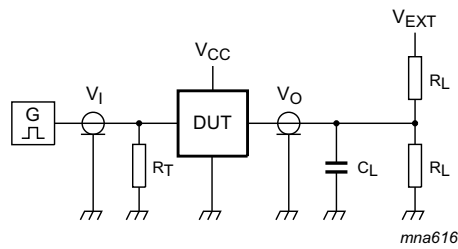


Measurement points are given in [Table 9](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 5. 3-state enable and disable times**

**Table 9. Measurement points**

Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 6. Test circuit for measuring switching times**

**Table 10. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	6 V
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	6 V
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$



13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

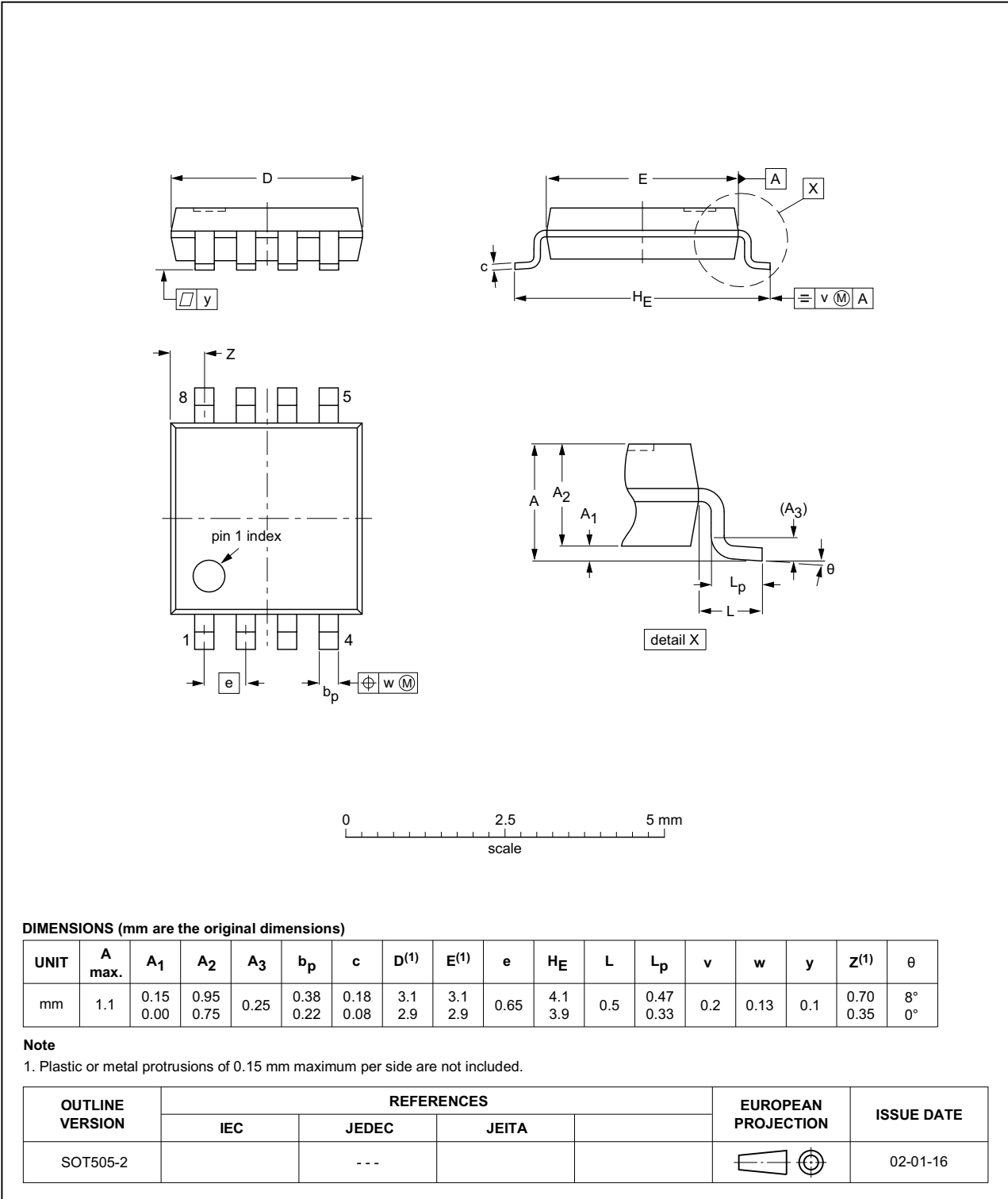


Fig 7. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

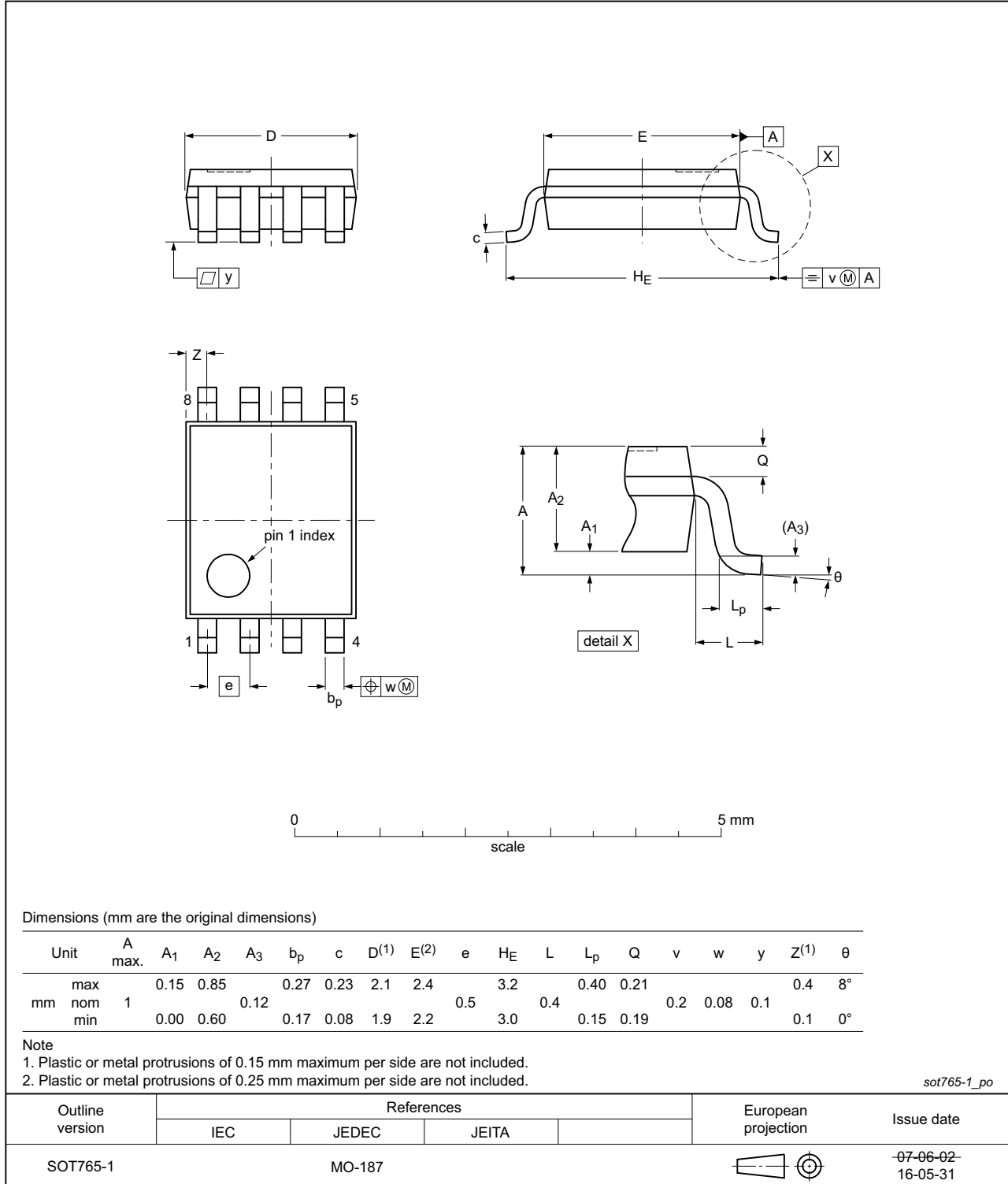


Fig 8. Package outline SOT765-1 (VSSOP8)

## 14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G126_Q100 v.2	20161214	Product data sheet	-	74LVC2G126_Q100 v.1
Modifications:	• <a href="#">Table 7</a> : The maximum limits for leakage current and supply current have changed.			
74LVC2G126_Q100 v.1	20150512	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

### 16.2 Definitions

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## 17. Contact information

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For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)

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