EMIF10-COM01F2

10-line IPAD™, EMI filter including ESD protection

Features

- EMI symmetrical (I/O) low-pass filter
- Lead free package
- Very low PCB space consuming: < 6 mm^2
- Very thin package: 0.65 mm
- High efficiency in ESD suppression on both input & output pins
- High reliability offered by monolithic integration

Complies with the following standard:

- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

Applications

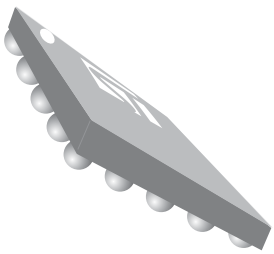
EMI filtering and ESD protection for:

- Computers and printers
- Communication systems
- Mobile phones

Description

The EMIF10-COM01F2 is a highly integrated device designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 Flip-Chip packaging means the package size is equal to the die size.

Additionally, this filter includes an ESD protection circuitry which prevents damage to the application when subjected to ESD surges up to 15 kV.



Flip Chip
(25 bumps)

Figure 1. Pin configuration (bump side)

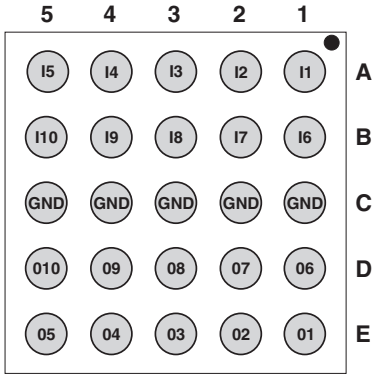
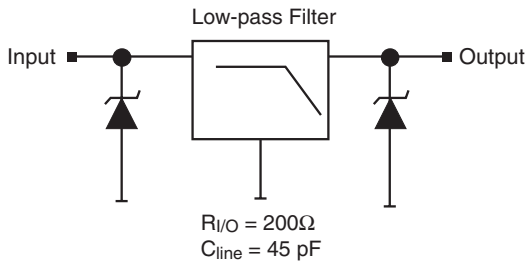


Figure 2. Basic cell configuration



TM: IPAD is a trademark of STMicroelectronics.

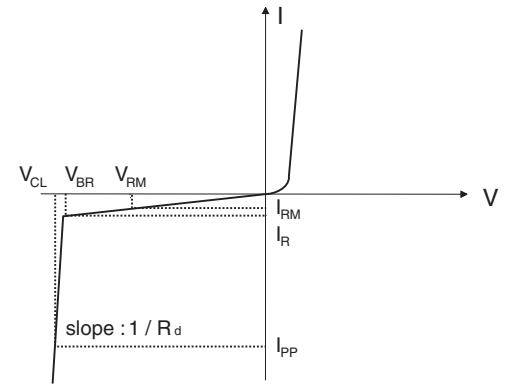
1 Characteristics

Table 1. Absolute ratings (T_{amb} = 25 °C)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge	15 8	kV
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Resistance between Input and Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8	10	V
I_{RM}	V_{RM} = 3 V per line			500	nA
R_d	I_{PP} = 10 A, t_p = 2.5 µs		1		Ω
$R_{I/O}$		180	200	220	Ω
C_{line}	At 0 V bias		45	50	pF
t_{LH}	V_{input} = 2.8 V R_{load} = 100 kΩ			25	ns

Figure 3. S21(db) attenuation measurement(1)

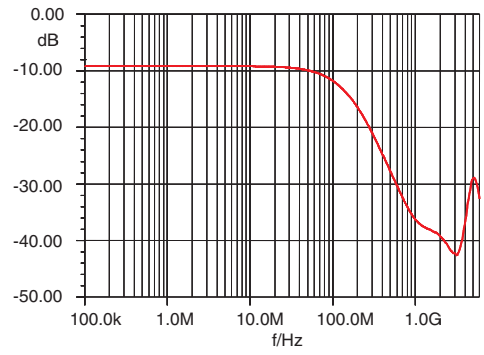
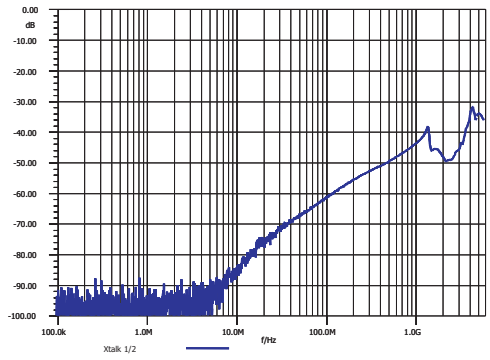


Figure 4. Analog crosstalk



1. Spikes at high frequencies are induced by the PCB layout

Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

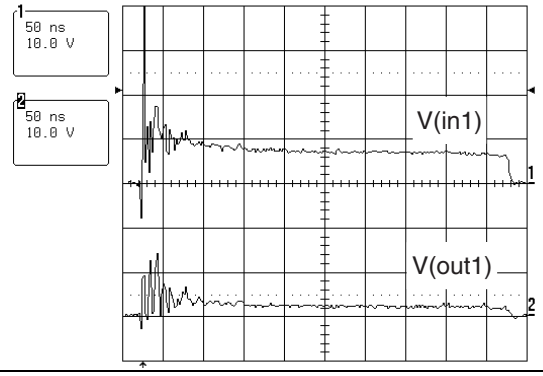


Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

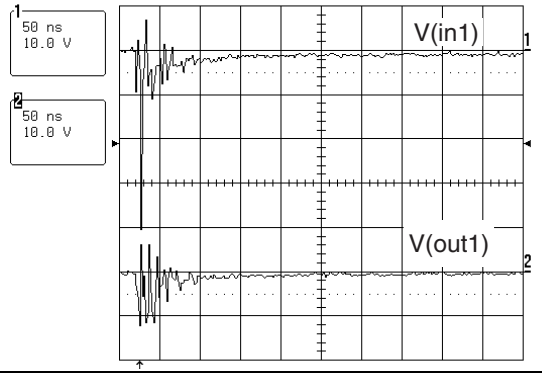


Figure 7. Rise time measurement

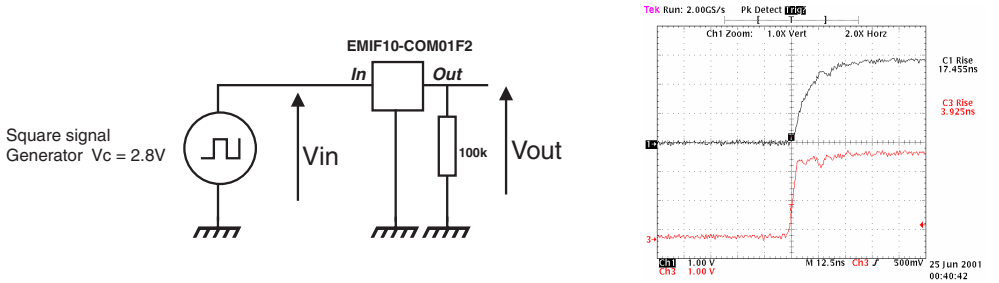
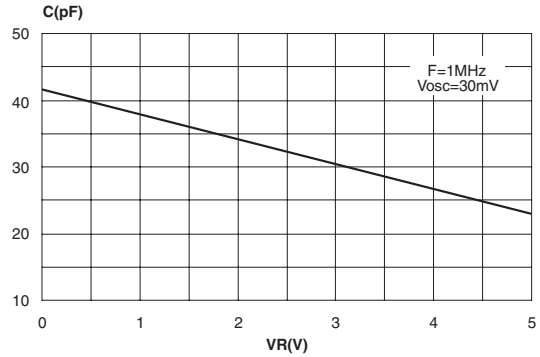
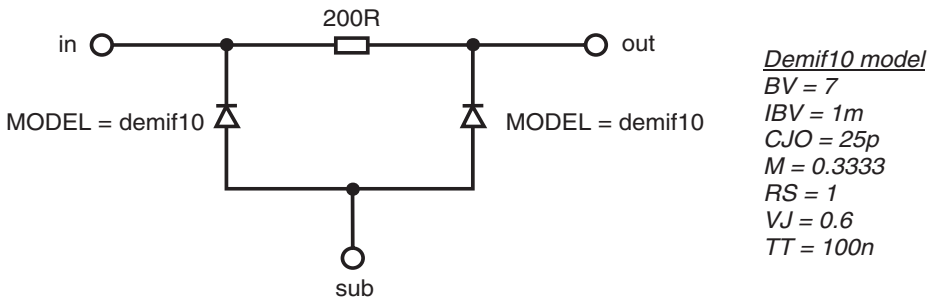


Figure 8. Capacitance versus reverse applied voltage



2 Application information

Figure 9. Aplac model

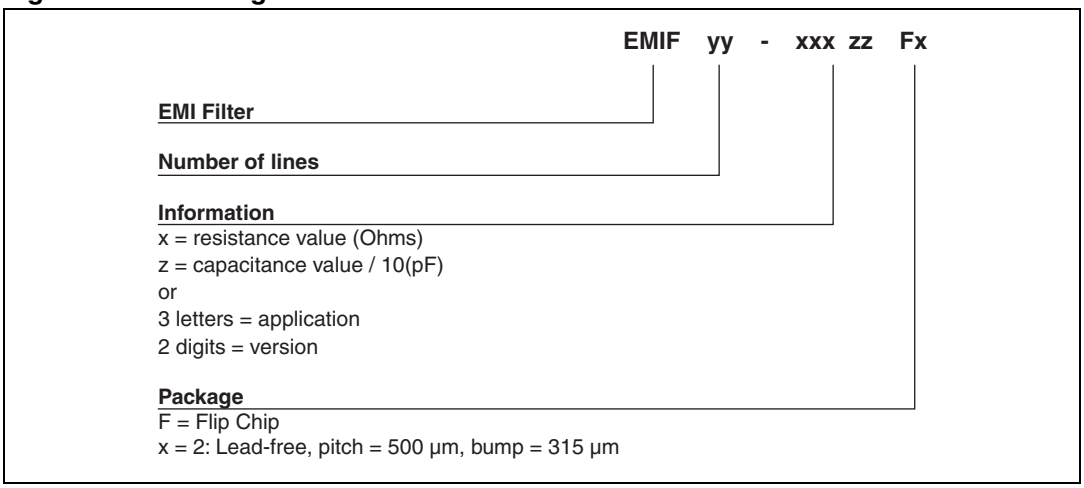


2.1 PCB grounding recommendations

In order to ensure a good efficiency in terms of ESD protection and filtering behavior, we recommend to implement microvias (100 µm dia.) between the GND bumps and the GND layer. GND bumps can be connected together in PCB layer 1, and in addition, if possible, use through hole vias (200 µm dia.) in both sides of filter to improve contact to GND (layer). This layout will minimize the distance to the ground and thus parasitic inductances. In addition, we recommend to have GND plane wherever possible.

3 Ordering information scheme

Figure 10. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Figure 11. Flip Chip package dimensions

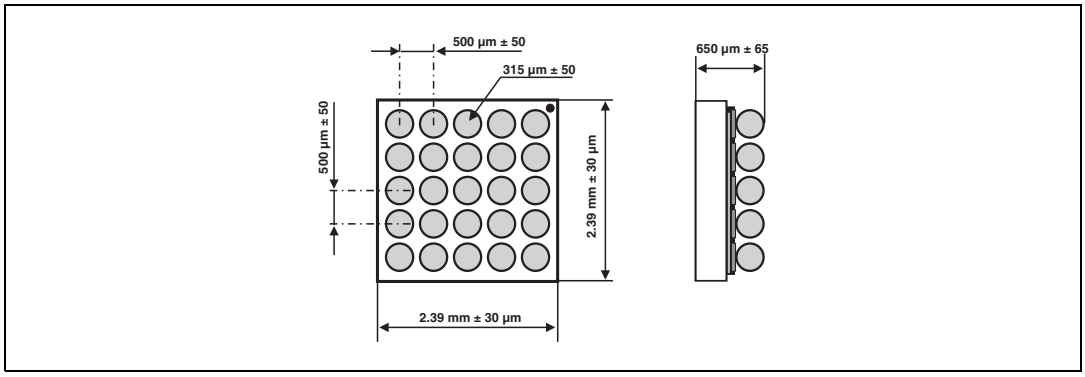


Figure 12. Footprint recommendations

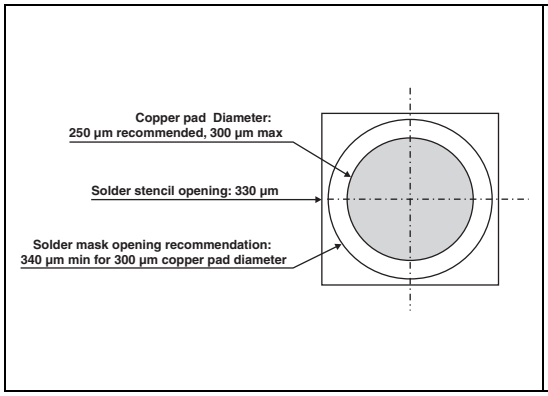


Figure 13. Marking

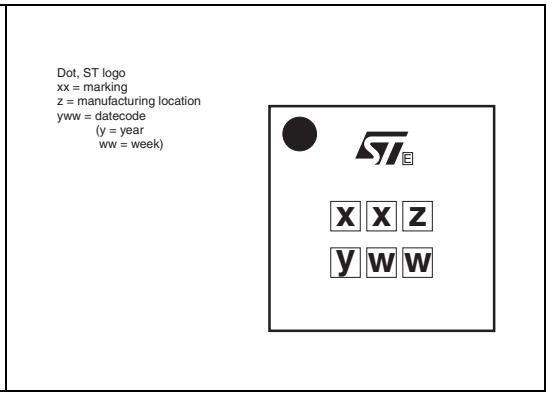
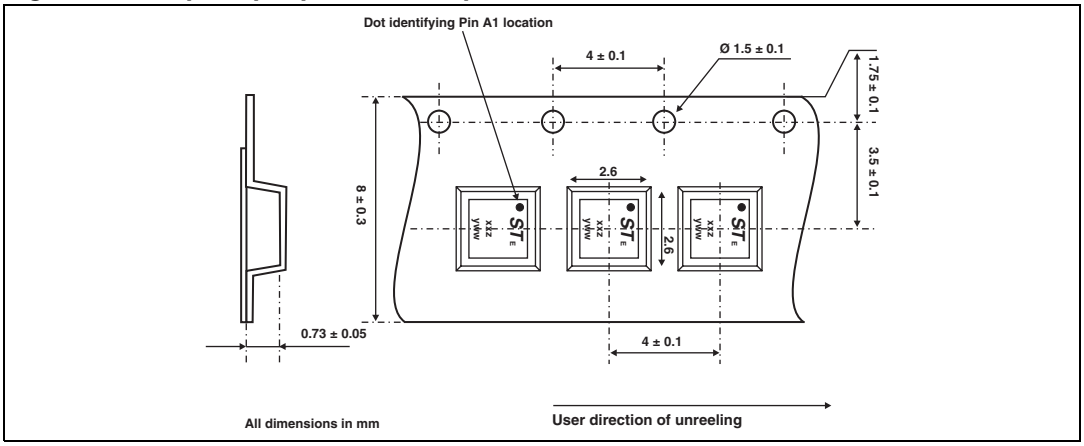


Figure 14. Flip Chip tape and reel specification



5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF10-COM01F2	FE	Flip Chip	8.3 mg	5000	Tape and reel

Note: More information is available in the application notes:

AN1235: “Flip Chip: Package description and recommendations for use”

AN1751: "EMI Filters: Recommendations and measurements"

6 Revision history

Table 4. Document revision history

Date	Revision	Description of changes
14-Dec-2004	1	First issue.
08-Apr-2005	2	Die shrink.
19-Oct-2005	3	Replaced Figures 3 and 13. Added ECOPACK statement.
03-Apr-2006	4	Reformatted to current standard. Pin identification in Figure 1 updated.
17-Apr-2008	5	Updated ECOPACK statement. Updated *Figure 10*, *Figure 11* and *Figure 14.* Reformatted to current standards.

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