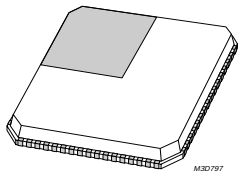


PIP202-12M-2

DC-to-DC converter powertrain

Rev. 02 — 24 November 2003 **Product data**

1. Description

The PIP202-12M is designed for use as the power output stage of a synchronous buck DC-to-DC converter. It contains a MOSFET control IC, two power MOSFET transistors and a Schottky diode. By combining the power MOSFETs and the driver circuit into a single component, stray inductances are virtually eliminated, resulting in higher switching frequency, lower switching losses and a compact, efficient design.

2. Features

- Input voltage conversion range from 3.3 V to 12 V
- Output voltages from 0.8 V to 5 V
- Capable of up to 25 A continuous output current
- Operating frequency up to 1 MHz
- Peak system efficiency >92% at 500 kHz
- Low-profile, surface mount package (10 × 10 × 0.85 mm)
- Compatible with any single or multi-phase PWM controller.

3. Applications

- High-current DC-to-DC point-of-load converters
- Small form-factor Voltage Regulator Modules
- Microprocessor and memory voltage regulators.

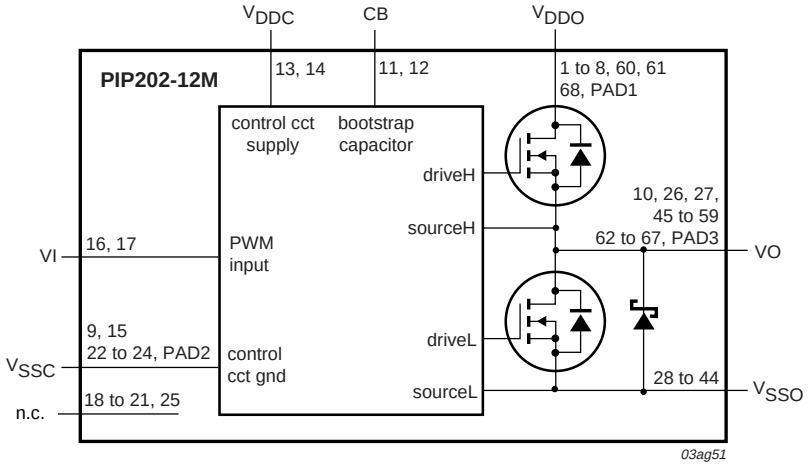
4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PIP202-12M-2	HVQFN68 (MLF68)	plastic, thermal enhanced very thin quad flat package; no leads; 68 terminals; body 10 × 10 × 0.85 mm	SOT687-1

PHILIPS

5. Block diagram

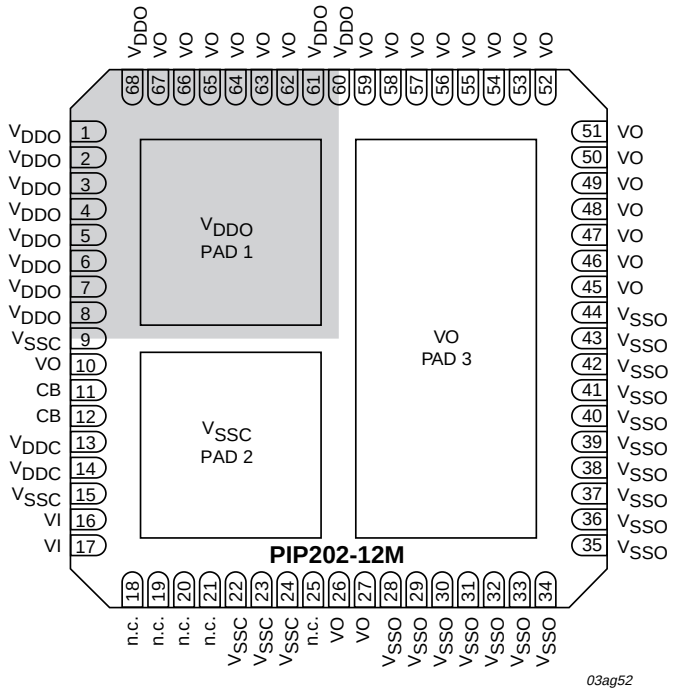


A bootstrap diode is integrated into the design of the PIP202-12M between V_{DDC} and CB.

Fig 1. Block diagram.

6. Pinning information

6.1 Pinning



Shaded area denotes terminal 1 index area.

Fig 2. Pin configuration (footprint view).

6.2 Pin description

Table 2: Pin description

Symbol	Pin		I/O	Description
V_{DDO}	1 to 8, 60, 61, 68	[1] [4]	-	output stage supply voltage
V_{SSC}	9, 15, 22 to 24	[2] [4]	-	control circuit supply ground
VO	10, 26, 27, 45 to 59, 62 to 67	[3] [4]	O	output
CB	11, 12		I/O	bootstrap capacitor connection
V_{DDC}	13, 14		-	control circuit supply voltage
VI	16, 17		I	pulse width modulated input
V_{SSO}	28 to 44		-	output stage supply ground
n.c.	18 to 21, 25	[5]	-	no internal connection

[1] All pins connected to PAD1

[2] All pins connected to PAD2

[3] All pins connected to PAD3

[4] PAD1, PAD2 and PAD3 are electrical connections and must be soldered to the printed circuit board

[5] All n.c. pins should be connected to V_{SSC}.

7. Functional description

7.1 Basic functionality

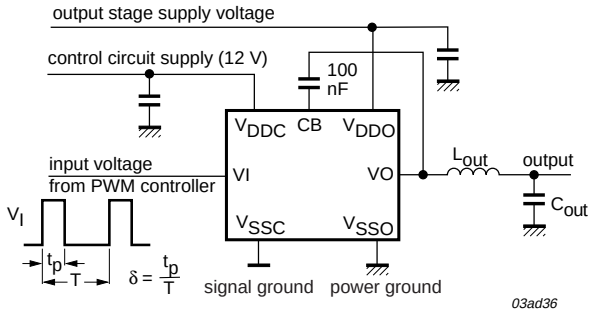


Fig 3. Simplified functional block diagram of a synchronous DC-to-DC converter output stage.

In order to understand the functions performed by the PIP202-12M, consider the requirements of a synchronous DC-to-DC converter output stage, driven from a PWM controller (Figure 3).

When the input voltage is HIGH, the upper MOSFET must be on and the lower MOSFET must be off. Current flows from the supply (V_{DDO}), through the upper MOSFET and the inductor (L_{out}), to the output.

When the input voltage is LOW and current is flowing in the inductor, the upper MOSFET must be off and the lower MOSFET must be on. Current flows from the power ground (V_{SSO}), through the lower MOSFET and the inductor (L_{out}), to the output.

Finally, when switching between states, both MOSFETs must not be on at the same time.

7.2 MOSFET driver function

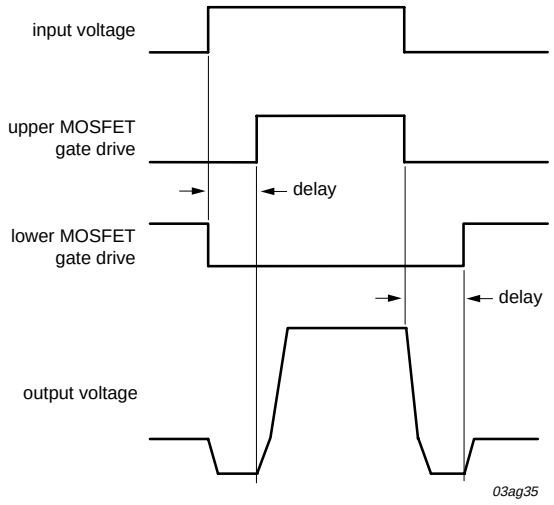


Fig 4. Input, output and gate drive waveforms of a synchronous DC-to-DC converter output stage.

The input, output and gate drive waveforms are shown in Figure 4. When the input voltage goes HIGH, the gate drive to the lower MOSFET immediately goes LOW. This causes the output current to flow through the Schottky diode, connected between the drain and source of the lower MOSFET. This causes output voltage to fall from zero to approximately −0.5 V.

After a delay, if the input voltage is still HIGH, the gate drive to the upper MOSFET goes HIGH. This causes the output voltage to rise to the output stage supply voltage, V_{DDO}.

When the input voltage goes LOW, the gate drive to the upper MOSFET immediately goes LOW. The output voltage falls from V_{DDO}, until it is clamped by the Schottky diode at approximately −0.5 V.

After a delay, if the input voltage is still LOW, the gate drive to the lower MOSFET goes HIGH. The lower MOSFET turns on, and the output voltage rises from −0.5 V to zero.

7.3 Bootstrap diode

A bootstrap diode is integrated into the design of the PIP202-12M between V_{DDC} and CB.

7.4 3-state function

If the input from the PWM controller becomes high impedance (3-state) for longer than $t_{d(3\text{-state})}$, then both MOSFETs are turned off and the VI input is driven to 2.5 V by an internal 2 x 10 kΩ resistor voltage divider between an internal 5 V reference and ground. Once the V_I input is outside the 3-state window for longer than $t_{d(3\text{-state})}$ normal operation will commence.

8. Limiting values

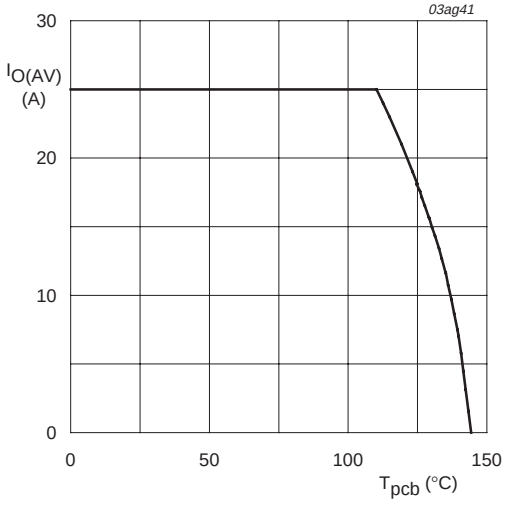
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDC}	control circuit supply voltage			–0.5	15	V
V_{DDO}	output stage supply voltage			–0.5	25	V
V_I	input voltage			–0.5	5.25	V
V_O	output voltage			–0.5	V_{DDO} + 0.5	V
V_{CB}	bootstrap voltage			–0.5	V_O + 15	V
$I_{O(AV)}$	average output current	V_{DDC} = 12 V; $T_{pcb} \leq$ 110 °C; Figure 5		-	25	A
I_{ORM}	repetitive peak output current	V_{DDC} = 12 V; $t_p \leq$ 10 µs	[1]	-	200	A
P_{tot}	total power dissipation	T_{pcb} = 25 °C	[2]	-	25	W
		T_{pcb} = 90 °C	[2]	-	12	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–55	+150	°C

[1] Pulse width and repetition rate limited by maximum value of T_j.

[2] Assumes a thermal resistance from junction to printed-circuit board of 5 K/W.



V_{DDC} = 12 V; V_{DDO} = 12 V; f_i = 500 kHz; V_O = 1.6 V.

Fig 5. Average output current as a function of printed-circuit board temperature.

9. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-pcb)}$	thermal resistance from junction to printed-circuit board		-	4	5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	device mounted on FR4 printed-circuit board; copper area around device 25 × 25 mm				
		no thermal vias	-	25	-	K/W
		with thermal vias	-	20	-	K/W
		with thermal vias and forced air cooling; airflow = 0.8 ms^{-1} (150 LFM)	-	15	-	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	measured on upper surface of package.	-	11	-	K/W

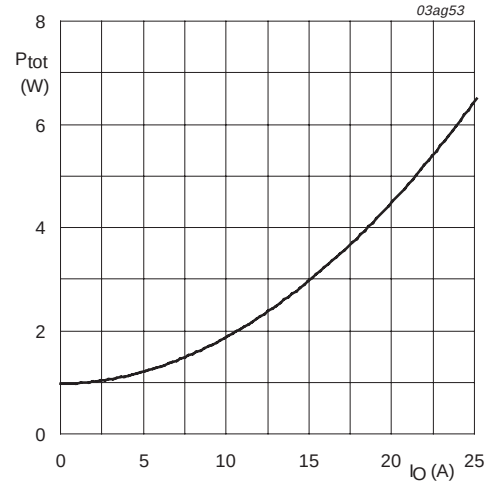
10. Characteristics

Table 5: Characteristics

V_{DDC} = 12 V; *T_j = 25 °C unless otherwise specified.*

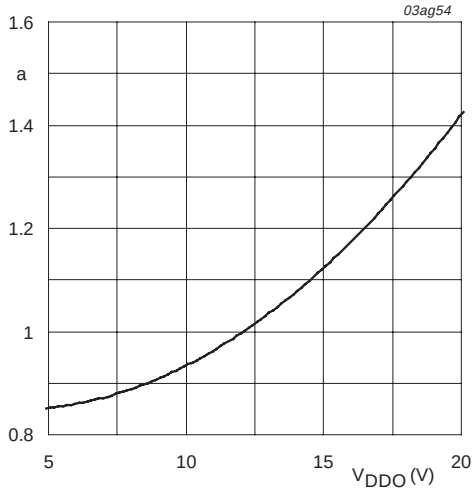
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V_{DDC}	control circuit supply voltage	25 °C ≤ T_j ≤ 150 °C		7	12	14	V
V_{IH}	HIGH-level input voltage	25 °C ≤ T_j ≤ 150 °C	[1]	3.0	3.45	3.9	V
V_{IL}	LOW-level input voltage	25 °C ≤ T_j ≤ 150 °C	[1]	1	1.45	1.9	V
I_{LI}	input leakage current	0 V ≤ V_I ≤ 5 V		-	0.3	1.2	mA
I_{DDC}	control circuit supply current	f_i = 0 Hz		-	1.5	3	mA
		f_i = 500 kHz; Figure 10		-	45	60	mA
P_{tot}	total power dissipation	V_{DDO} = 12 V; $I_{O(AV)}$ = 20 A; f_i = 500 kHz; V_O = 1.6 V; T_{pcb} ≤ 120 °C; Figure 6		-	4.5	-	W
Dynamic characteristics							
$t_{d(on)(IH-OH)}$	turn-on delay time input HIGH to output HIGH	V_{DDO} = 12 V; $I_{O(AV)}$ = 25 A		-	77	85	ns
$t_{d(off)(IL-OL)}$	turn-off delay time input LOW to output LOW			-	30	45	ns
$t_{o(r)}$	output rise time			-	18	25	ns
$t_{o(f)}$	output fall time			-	12	20	ns
$t_{d(3\text{-state})}$	3-state delay time			-	140	-	ns

[1] If the input voltage remains between V_{IH} and V_{IL} (2.5 V typ) for longer than $t_{d(3\text{-state})}$, then both MOSFETs are turned off.



V_{DDC} = 12 V; V_{DDO} = 12 V; V_O = 1.6 V; f_i = 500 kHz

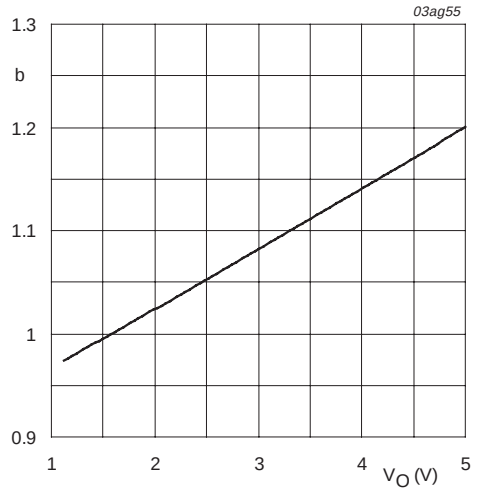
Fig 6. Total power dissipation as a function of average output current; typical values.



V_{DDC} = 12 V; V_O = 1.6 V; f_i = 500 kHz; $I_{O(AV)}$ = 12.5 A

$$a = \frac{P_{tot}}{P_{tot(V_{DDO} = 12V)}}$$

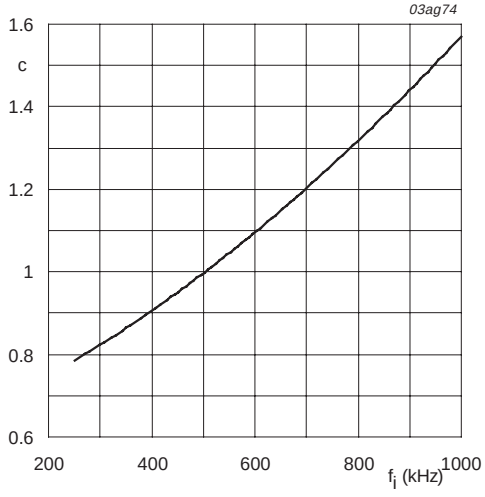
Fig 7. Normalized power dissipation as a function of output stage supply voltage; typical values.



V_{DDC} = 12 V; V_{DDO} = 12 V; f_i = 500 kHz; $I_{O(AV)}$ = 12.5 A

$$b = \frac{P_{tot}}{P_{tot(V_O = 1.6V)}}$$

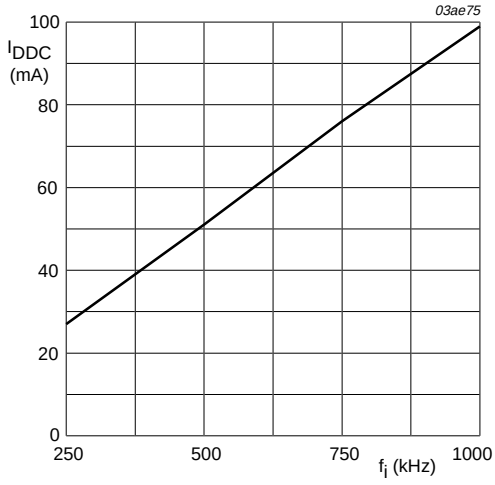
Fig 8. Normalized power dissipation as a function of output voltage; typical values.



V_{DDC} = 12 V; V_{DDO} = 12 V; V_O = 1.6 V; $I_{O(AV)}$ = 12.5 A

$$c = \frac{P_{tot}}{P_{tot(f_i = 500kHz)}}$$

Fig 9. Normalized power dissipation as a function of input frequency; typical values.



V_{DDC} = 12 V; V_{DDO} = 12 V; V_O = 1.6 V; $I_{O(AV)}$ = 12.5 A.

Fig 10. Control circuit supply current as a function of input frequency; typical values.

11. Application information

11.1 Typical application

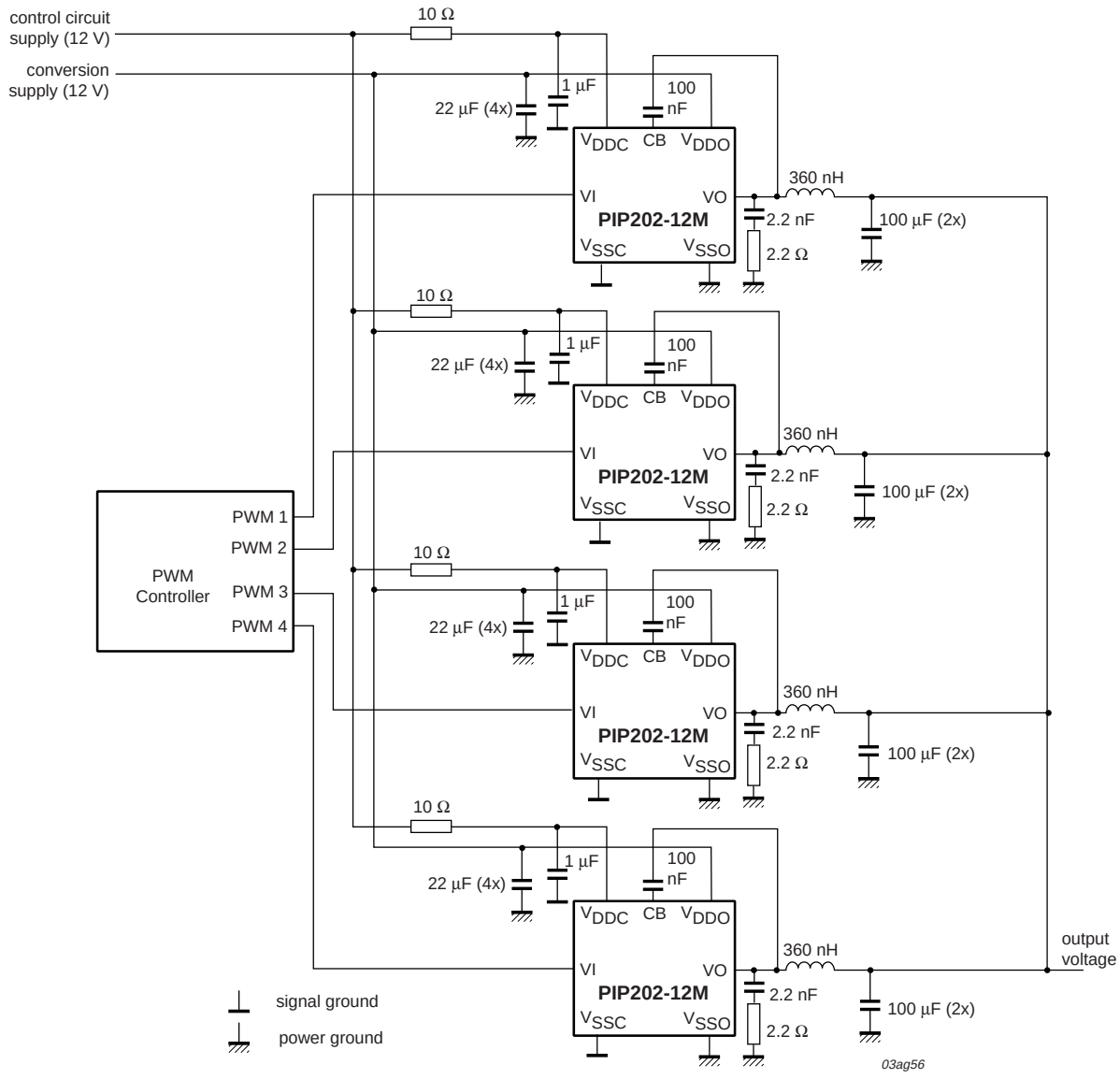


Fig 11. Typical application circuit using the PIP202-12M in a four-phase converter.

A typical four-phase buck converter is shown in Figure 11. This system uses four PIP202-12M devices to deliver a continuous output current of 80 A at an operating frequency of 500 kHz.

Remark: An external bootstrap diode is not required as one is already integrated into the design of the PIP202-12M between V_{DDC} and CB.

At 500 KHz and 20 A output current, the maximum dissipation in each PIP202-12M is typically 4.5 W. The typical thermal resistance from junction to ambient is given in Table 4. With thermal vias and forced air cooling, the thermal resistance of each PIP202-12M from junction to ambient is 15 K/W. Assuming an ambient temperature of 55 °C, the junction temperature (T_j) is given by:

$$T_j = P_{tot} \times R_{th(j-a)} + T_{amb} = 4.5 \times 15 + 55 = 122.5°C \quad (1)$$

The thermal resistance between the junction and the printed-circuit board is 5 K/W. Therefore, the printed-circuit board temperature (T_{pcb}) is given by:

$$T_{pcb(max)} = T_{j(max)} - P_{tot} \times R_{th(j-pcb)} = 122.5 - 4.5 \times 5 = 100°C \quad (2)$$

11.2 Advantages of an integrated driver

One problem in the design of low-voltage, high-current DC-to-DC converters using discrete components, is stray inductance between the various circuit elements.

Stray inductance in the gate drive circuit increases the switching times of the MOSFETs and causes high-frequency oscillation of the gate voltage.

Stray inductance in the high-current loop between V_{DDO} and V_{SSO} causes switching losses and electromagnetic interference. In discrete designs, high-frequency electric and magnetic fields radiate from PCB tracks and couple into adjacent circuits.

By integrating the power MOSFETs and their drive circuits into a single package, stray inductance is virtually eliminated, resulting in a compact, efficient design.

In discrete designs, the delays in the MOSFET drivers must be long enough to ensure no cross-conduction even when using the slowest MOSFETs. Use of an integrated driver allows the propagation delays in the MOSFET drivers to be precisely matched to the MOSFETs. This minimizes switching losses and eliminates cross-conduction whilst allowing the circuit to operate at a higher frequency.

11.3 External connection of power and signal lines

A major benefit of the PIP202-12M module is the ability to switch the internal power MOSFETs faster than a DC-to-DC converter built from discrete components. This not only reduces switching losses and increases system efficiency but also results in higher transient voltages on the device supply lines (V_{DDO} and V_{SSO}). This is due to the high rate of change of current (dI/dt) through the combined parasitic inductance of the PCB tracks and the decoupling capacitors.

To minimize the amplitude of these transients, decoupling capacitors must be placed between V_{DDO} and V_{SSO}, as close as possible to the device pins. Low inductance, chip ceramic capacitors are recommended.

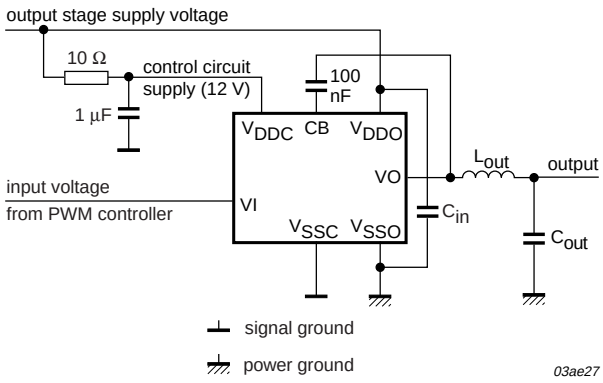


Fig 12. External connection of power and signal lines.

To protect the control circuit from the transient voltages, the following precautions must be taken. Refer to Figure 12.

1. The output stage ground (V_{SSO}) must be connected to the decoupling capacitor (C_{in}) before joining the ground plane. Otherwise, the switching noise on V_{SSO} will couple into the control circuit ground (V_{SSC}).
2. The control circuit supply must be filtered using a resistor-capacitor (RC) filter. The values shown in Figure 12 are suitable for most applications.
3. It is essential that the V_{SSC} (signal ground) connection at the device is not connected in the current return path between the V_{SSO} (power ground) connection at the device and the V_{DDO} input capacitor.
4. It is also essential that the input to the V_{DDC} (logic power) filter is not connected in the current path between the V_{DDO} (conversion power) connection at the device.

11.4 Switching frequency

A high operating frequency reduces the size and number of capacitors needed to filter the output current, and also reduces the size of the output inductors. The disadvantage, however is higher dissipation due to switching and MOSFET driver losses. For example, doubling the operating frequency of the circuit in Figure 11 from 500 kHz to 1 MHz would increase the power dissipation in each PIP202-12M from 4 W to 6 W, at an output current of 20 A in each PIP202-12M.

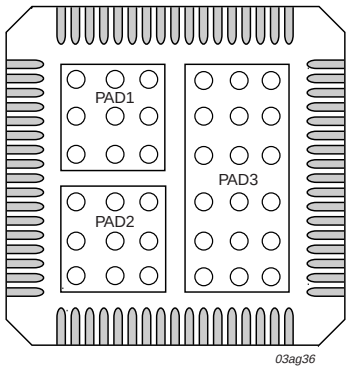
The maximum switching frequency is limited by thermal considerations, the dissipation in the PIP202-12M device(s) and the thermal resistance from junction to ambient.

11.5 Thermal design

The PIP202-12M has three pads on its underside. These are designated PAD1, PAD2 and PAD3 (Figure 2). PAD1 is connected to V_{DDO}, PAD2 is connected to V_{SSC} and PAD3 is connected to VO. In addition to providing low inductance electrical connections, these pads conduct heat away efficiently from the MOSFETs and control IC to the printed-circuit board. The thermal resistance from junction to printed-circuit board is approximately 5 K/W. In order to take full advantage of the low

thermal resistance of this package, the printed-circuit board must be designed so that heat is conducted away efficiently from the package. This can be achieved by maximizing the area of copper around each pad, and by incorporating thermal vias to conduct the heat to inner and/or bottom layers of the printed-circuit board.

An example of a thermal via pattern is shown in Figure 13. In a typical application, with no forced air cooling, the use of thermal vias typically reduces the thermal resistance from 25 K/W to 20 K/W. The additional use of a small fan can reduce this further to approximately 15 K/W.



All holes 0.5 mm diameter with 1 mm spacing.

Fig 13. Printed-circuit board thermal via pattern.

The thermal resistance of a particular design can be measured by passing a known current between V_{SSO} and V_{DDO}. The current flows through the Schottky diode and through the source-drain diode of the upper MOSFET. The direction of current flow is into V_{SSO} and out of V_{DDO}. The volt drop between V_{SSO} and V_{DDO} is then measured and used to calculate the power dissipation in the PIP202-12M. The case temperature of the PIP202-12M can be measured using an infra-red thermometer. The thermal resistance can then be calculated using the following equation:

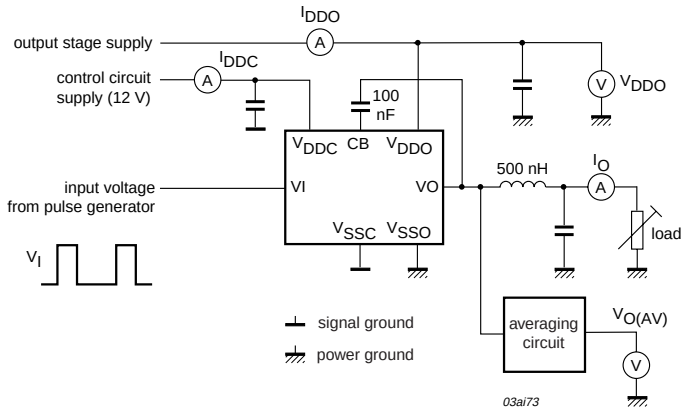
$$R_{th(j-pcb)} = \frac{T_{case} - T_{amb}}{I \times V_F}(K/W) \quad (3)$$

where T_{case} is the measured case temperature (°C), T_{amb} is the ambient temperature (°C), I is the MOSFET current (A), and V_F is the voltage drop between V_{SSO} and V_{DDO} (V).

Where more than one phase is used, for example the circuit of Figure 11, the thermal resistance of each PIP202-12M should be measured with current flowing in all phases.

12. Test information

Figure 14 shows the test circuit used to measure power loss in the PIP202-12M. The output voltage is measured using an averaging circuit. This eliminates losses in the output inductor and the PCB tracks. The calculated power loss, using this method, includes the losses in the Equivalent Series Resistance (ESR) of the input filter capacitors. This must be subtracted from the total loss to give the net loss in the PIP202-12M.



$$P_{DDO} = V_{DDO} \times I_{DDO}$$

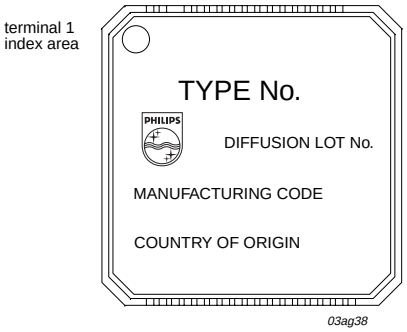
$$P_{DDC} = V_{DDC} \times I_{DDC}$$

$$P_O = V_{O(AV)} \times I_O$$

$$P_{tot} = P_{DDO} + P_{DDC} - P_O$$

Fig 14. Power loss (P_{tot}) test circuit.

13. Marking



TYPE No: PIP202-12M-N (N is version number)

DIFFUSION LOT No: 7 characters

MANUFACTURING CODE: see Figure 16

COUNTRY OF ORIGIN: Korea

Fig 15. SOT687-1 marking.

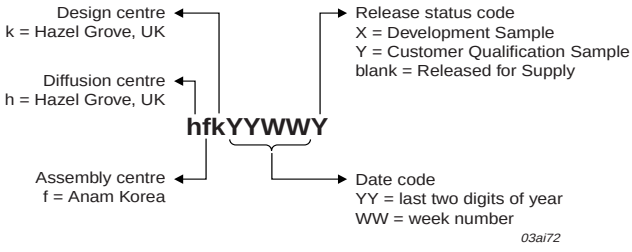
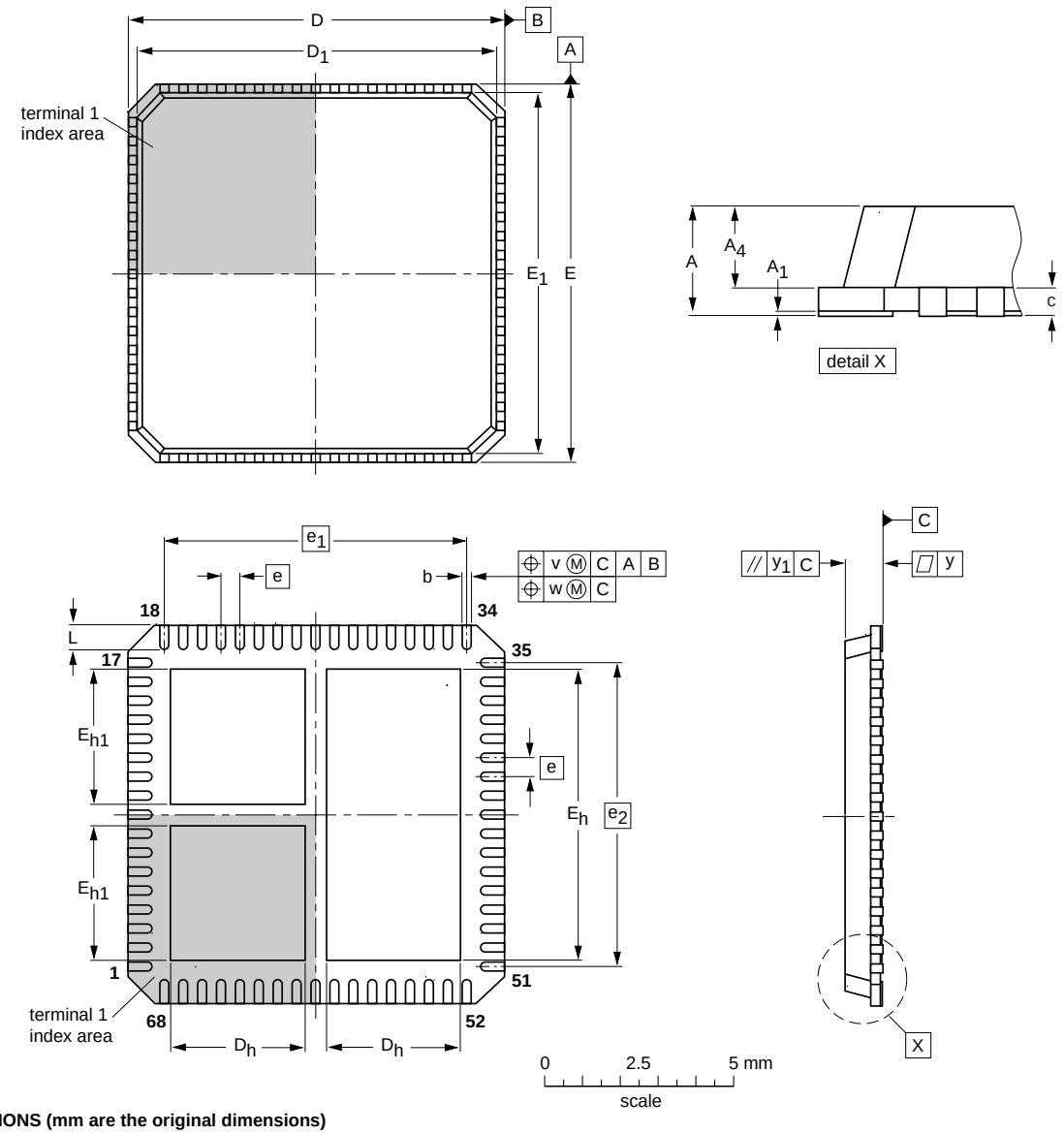


Fig 16. Interpretation of manufacturing code.

14. Package outline

HVQFN68: plastic thermal enhanced very thin quad flat package; no leads; 68 terminals; body 10 x 10 x 0.85 mm **SOT687-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_4	b	c	D	D_1	D_h	E	E_1	E_h	E_{h1}	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.80 0.65	0.30 0.18	0.2	10.15 9.85	9.95 9.55	3.8 3.5	10.15 9.85	9.95 9.55	7.85 7.55	3.8 3.5	0.5	8	8	0.75 0.50	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT687-1	- - -	MO-220	- - -			~~02-10-18~~ 03-06-13

Fig 17. SOT687-1.

15. Soldering

15.1 Introduction to soldering MLF packages

The MicroLeadFrame package (MLF) is a near Chip Scale Package (CSP) with a copper leadframe. It is a leadless package, where electrical contact to the printed circuit board is made through metal pads on the underside of the package. In addition to the small pads around the periphery of the package, there are large pads on the underside that provide low thermal resistance, low electrical resistance, low inductance connections between the power components inside the MLF package and the PCB. It is this feature of the MLF package that makes it ideally suited for VRM applications.

Electrical connection between the package and the printed circuit board is made by printing solder paste on the printed circuit board, placing the component and reflowing the solder in a convection or infra-red oven. The solder reflow process is shown in Figure 18 and the typical temperature profile is shown in Figure 19. To ensure good solder joints, the peak temperature T_p should not exceed 220 °C for thin packages such as MLF, and the time above liquidus temperature should be less than 1.25 minutes. The maximum temperature can be increased for lead free solder. The ramp rate during preheat should not exceed 3 K/s. Nitrogen purge is recommended during reflow.

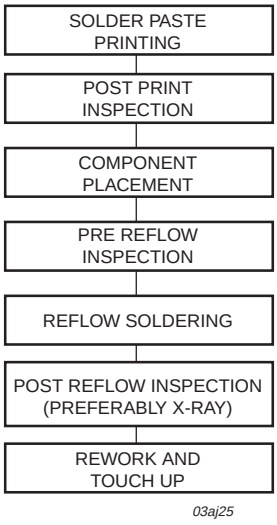


Fig 18. Typical reflow soldering process flow.

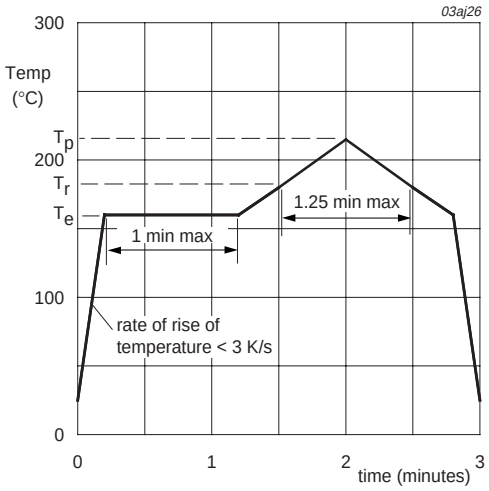


Fig 19. Typical reflow soldering temperature profile.

15.2 Rework guidelines

Since the solder joints are largely inaccessible, only the side fillets can be touched up. If there are defects underneath the package, then the whole package has to be removed.

The first step in component removal is to reflow the solder joints. It is recommended that the board is heated from the underside using a convective heater whilst hot air or gas is directed at the upper surface of the component. Nozzles should be used to direct the hot air or gas to minimize heating of adjacent components. Excessive airflow should be avoided since this may cause the package to skew. An airflow of 15 to 20 liters per minute is usually adequate.

Once the solder joints have reflowed, the component should be lifted off the board using a vacuum pen.

The next step is to clean the solder pads using solder braid and a blade shaped soldering tool. Finally, the pads should be cleaned with a solvent. The solvent is usually specific to the type of solder paste used in the original assembly and the paste manufacturers recommendations should be followed.

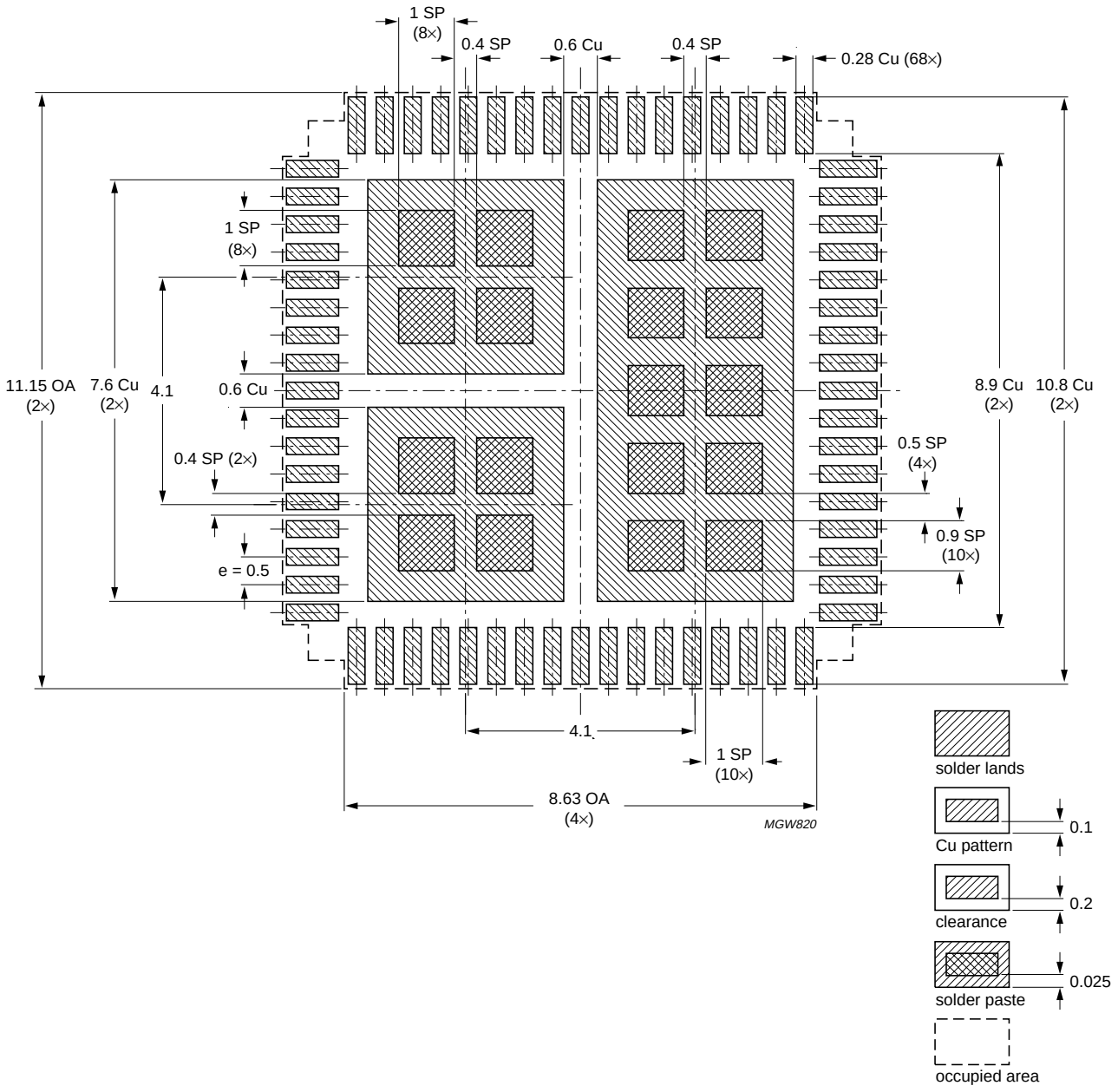
16. Mounting

16.1 PCB design guidelines

The terminals on the underside of the package are rectangular in shape with a rounded edge on the inside. Electrical connection between the package and the printed-circuit board is made by printing solder paste onto the PCB footprint followed by component placement and reflow soldering. The PCB footprint shown in Figure 20 is designed to form reliable solder joints.

The use of solder resist between each solder land is recommended. PCB tracks should not be routed through the corner areas shown in Figure 20. This is because there is a small, exposed remnant of the leadframe in each corner of the package, left over from the cropping process.

Good surface flatness of the PCB lands is desirable to ensure accuracy of placement after soldering. Printed-circuit boards that are finished with a roller tin process tend to leave small lumps of tin in the corners of each land. Levelling with a hot air knife improves flatness. Alternatively, an electro-less silver or silver immersion process produces completely flat PCB lands.



All dimensions in mm.

Fig 20. PCB footprint for SOT687-1 package (reflow soldering).

16.2 Solder paste printing

The process of printing the solder paste requires care because of the fine pitch and small size of the solder lands. A stencil thickness of 0.125 mm is recommended. The stencil apertures can be made the same size as the PCB lands in Figure 20.

The type of solder paste recommended for MLF packages is “No clean”, Type 3, due to the difficulty of cleaning flux residues from beneath the MLF package.

17. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20031124		**Product data (9397 750 11943)** Modifications: • Table 5 “Characteristics” on page 6: Min, Typ and Max values changed for V_{IH}, V_{IL} and $t_{d(3\text{-state})}$.
01	20020715	-	**Product data (9397 750 10031)**

18. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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