Introduction

The ACS8944 JAM PLL is a Jitter- Attenuating, Multiplying Phase-Locked Loop, for generating low jitter output clocks compliant up to SONET OC-12 and STM-4 622.08 MHz specifications. Its primary function is to clean up clock jitter for high performance optical line cards which have OC-3 or OC-12 SONET serializers or framers, and is the entry level device in Semtech's range of JAM PLLs.

The ACS8944 JAM PLL has a single differential LVPECL input and a single differential LVPECL output. Both input and output clock frequencies are individually programmable and can be hardware configured to be any of 19.44 MHz, 38.88 MHz, 77.76 MHz or 155.52 MHz.

The headline jitter figures quoted for the ACS8944 depend on the frequency band over which the jitter is measured. For example, typical stand-alone output jitter is typically 2.8 ps rms (well within GR-253-CORE[8] specification requirements of 16.1 ps rms for OC-12 and 64.3 ps rms for OC-3).

The device's operating bandwidth (and consequently the jitter attenuation point relating to this bandwidth) is set by external passive components in a differential arrangement which offers good noise immunity.

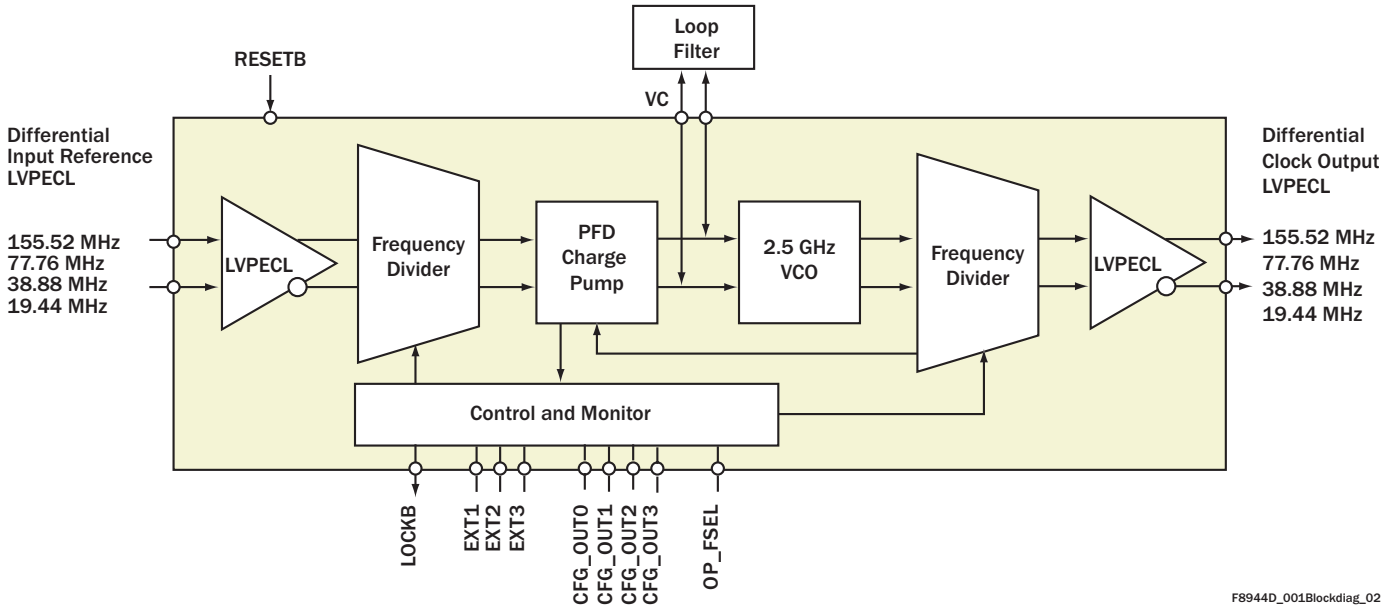
Features

- Meets rms jitter requirements of:
  - Telcordia GR-253-CORE[8] for OC-3 and OC-12
  - ITU-T G.813[4]/G.812[3] for STM-1 and STM-4 rates
  - ETSI EN300-462-7[1]/EN302-084[2] up to STM-16 rates
- Typical jitter generation down to:
  - 0.3 ps rms for 250 kHz to 5 MHz band for G.813, or EN300-462, at STM-4 (OC-12) rates
  - 2.8 ps rms for 12 kHz to 20 MHz band (against 4.02 ps rms for GR-253-CORE at OC-48 rate)
- Pull-in range ±400 ppm about center input frequency
- Frequency translation e.g. 19.44 MHz to 155.52 MHz
- 3.3 V operation, - 40 to +85 °C temperature range
- Small outline leadless 7 mm x 7 mm QFN48 package
- Demonstration Board available on request
- PLL bandwidth and jitter peaking are fully adjustable.
- Supports bandwidths from 2 kHz for superior input jitter filtering
- Lead (Pb)-free version available (ACS8944T), RoHS[9] and WEEE[10] compliant

Note...For items marked [1],[2], etc. references are given in full in the Reference Section on page 21.

Block Diagram

Figure 1 Simplified Block Diagram of the ACS8944 JAM PLL



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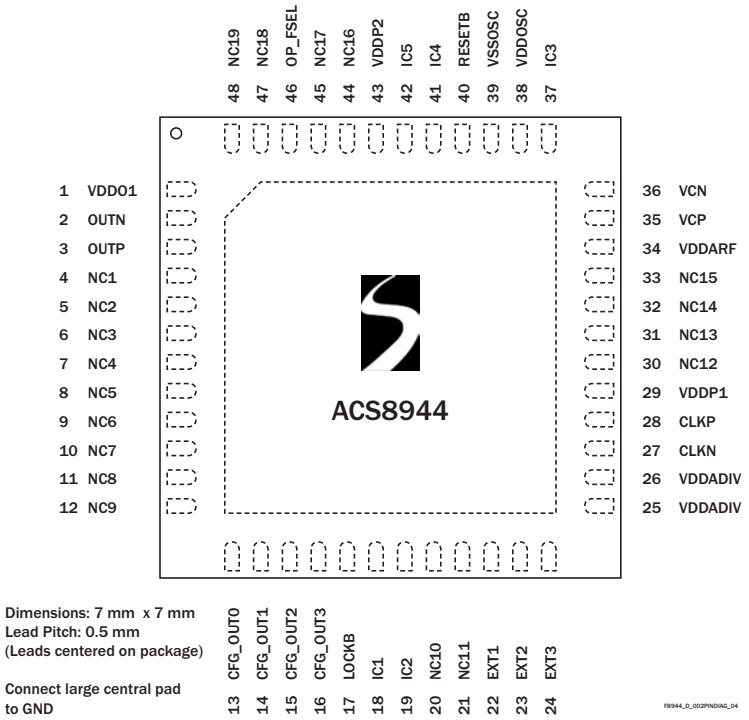
Pin Diagram

Figure 2 ACS8944 Pin Diagram



Pin Description

Table 1 Power Pins

Pin No.	Symbol	I/O	Type	Description
1	VDDO1	P	-	Supply voltage. Supply to OUTP & OUTN clock output pins, +3.3 Volts ±5%.
25, 26	VDDADIV	P	-	Supply voltage. Supply for internal dividers in VCO loop, kept as an isolated supply to allow for low supply noise for the output divider stages. +3.3 Volts ±5%.
29, 43	VDDP1,VDDP2	P	-	Supply voltage. Supply to input and output pins. +3.3 Volts ±5%.
34	VDDARF	P	-	Supply voltage. Supply for phase and frequency detector (PFD), kept as an isolated supply to allow for low supply noise. +3.3 Volts ±5%.
38	VDDOSC	P	-	Supply voltage. Supply input to the internal VCO. +3.3 Volts +5%/-10%
39	VSSOSC	P	-	Supply ground. 0 V for VCO.
49	VSS0	P	-	Supply ground. Common 0 V. This is the central leadframe pad on the underneath of the package.

Note...I = Input, O = Output, P = Power, LVTTL/LVCMOS^{U} = LVTTL/LVCMOS input with pull-up resistor, LVTTL/LVCMOS$_{D}$ = LVTTL/LVCMOS input with pull-down resistor.

Table 2 Internally Connected (IC)/ Not Connected (NC) Pins

Pin No.	Symbol	I/O	Type	Description
18,19, 37, 41	IC1, IC2, IC3, IC4,	-	-	Internally connected. Connect to ground.
42	IC5	-	-	Internally connected. Connect to VDD.
4, 5, 6, 7, 8, 9, 10, 11, 12, 20, 21, 30, 31, 32, 33, 44, 45, 47, 48	NC1, NC2, NC3, NC4, NC5, NC6, NC7, NC8, NC9, NC10, NC11, NC12 NC13, NC14, NC15, NC16, NC17, NC18, NC19	-	-	Not connected. Leave to float.

Table 3 Functional Pins

Pin No.	Symbol	I/O	Type	Description
2	OUTN	O	LVPECL	LVPECL differential output at a rate from 19.44 MHz up to 155.52 MHz. Partnered with pin 3. See pin 3 description for more detail.
3	OUTP	O	LVPECL	LVPECL differential output at a rate from 19.44 MHz up to 155.52 MHz. Partnered with pin 2. The output frequency selection is preset by externally connecting OP_FSEL pin (pin 46), to one from a set of four output frequency pins CFG_OUT[3:0] (Pins 16, 15, 14 and 13); which, on reset will give a corresponding generated output frequency of 19.44 MHz, 38.88 MHz, 77.76 MHz, or 155.52 MHz.
13	CFG_OUT0	O	LVTTL/LVCMOS	Configuration pin used to set input reference frequency for CLK (N and P) and output clock frequency for OUT (N and P) used in conjunction with pins 14, 15, 16, and 46 as defined in Tables 4 and 5.
14	CFG_OUT1	O	LVTTL/LVCMOS	Configuration pin used to set input reference frequency for CLK (N and P) and output clock frequency for OUT (N and P) used in conjunction with pins 13, 15, 16 and 46 as defined in Tables 4 and 5.
15	CFG_OUT2	O	LVTTL/LVCMOS	Configuration pin used to set input reference frequency for CLK (N and P) and output clock frequency for OUT (N and P) used in conjunction with pins 13, 14, 16 and 46 as defined in Tables 4 and 5.
16	CFG_OUT3	O	LVTTL/LVCMOS	Configuration pin used to set input reference frequency for CLK (N and P) and output clock frequency for OUT (N and P) used in conjunction with pins 13, 14, 15 and 46 as defined in Tables 4 and 5.
17	LOCKB	O	Analog	Lock detect output. This is a pulse width modulated output current, with each pulse typically +10 µA. The output produces a pulse with a width in proportion to the phase error seen at the internal phase detector. This pin should be connected via an external parallel capacitor and resistor to ground. The pin voltage will then give an indication of phase lock: When low, the device is phase locked; when high the device has frequent large phase errors and so is not phase locked. The value of the RC components used determines the time and level of consistency required for lock indication.
22	EXT1	I	LVTTL/LVCMOS$_D$	Input frequency configuration pin. See Table 4.
23	EXT2	I	LVTTL/LVCMOS$_D$	Input frequency configuration pin. See Table 4.

Table 3 Functional Pins (cont...)

Pin No.	Symbol	I/O	Type	Description
24	EXT3	I	LVTTL/LVCMOS$_D$	Input frequency configuration pin. See Table 4.
27	CLKN	I	LVPECL	Input reference clock to which the PLL will phase and frequency lock (negative pin of differential pair, partnered with pin 28). Can accept 19.44 MHz, 38.88 MHz, 77.76 MHz or 155.52 MHz to within ±400 ppm.
28	CLKP	I	LVPECL	Input reference clock to which the PLL will phase and frequency lock (positive pin of differential pair, partnered with pin 27). Can accept 19.44 MHz, 38.88 MHz, 77.76 MHz or 155.52 MHz to within ±400 ppm.
35	VCP	I/O	Analog	Connection for external loop filter components. This is the differential control voltage input to the internal VCO and the internal differential charge pump output.
36	VCN	I/O	Analog	Connection for external loop filter components. This is the differential control voltage input to the internal VCO and the internal differential charge pump output.
40	RESETB	I	LVTTL/LVCMOS^U Schmitt Trigger	Active low reset signal with pull up and Schmitt type input. Used to apply a Power On Reset (POR) signal during system initialization. Should be connected via a capacitor to ground.
46	OP_FSEL	I	LVTTL/ LVCMOS$_D$	Output Frequency Select Pin. Used with the Output Frequency Configuration pins (pins 13 to 16) to configure the output frequency (on power-up/reset) of the differential output OUT(N/P). See Table 5.

Note...I = Input, O = Output, P = Power, LVTTL/LVCMOS^U = LVTTL/LVCMOS input with pull-up resistor, LVTTL/LVCMOS$_D$ = LVTTL/LVCMOS input with pull-down resistor

Description

The ACS8944 is a low jitter integrated PLL for clock dejittering and clock rate translation, meeting the jitter requirements for SONET up to and including OC-12 (622.08 MHz systems). It is compliant to the relevant ITU, Telcordia/Bellcore and ETSI standards for at least OC-3 (155.52 MHz) and OC-12 (622.08 MHz) - equivalent to the corresponding STM-1 and STM-4 rates.

It can be configured for a range of applications using a minimal number of external components and is available in a small form factor QFN48 package at 7 mm x 7 mm x 0.9 mm outer dimensions.

Input

The ACS8944 has a single, LVPECL, differential input (CLKN/P, pins 27 and 28). It is designed to operate with any of 19.44 MHz, 38.88 MHz, 77.76 MHz or 155.52 MHz input references, and can pull in an input which is within ±400 ppm of these spot frequencies.

Input Configuration

The input must be configured for the expected input frequency. This is achieved by connecting the EXT[3:1] pins, to the configuration pins or to power (VDD) or ground (VSS), in accordance with the configuration scheme in Table 4, e.g. for an expected input of 155.52 MHz, connect EXT1 to VSS, EXT2 to CFG_OUT1 and EXT3 to CFG_OUT3.

Table 4 Input Frequency Selection

For Expected Input Frequency of	Connect		
	EXT1	EXT2	EXT3
	to		
19.44 MHz	CFG_OUT3	VDD	CFG_OUT3
38.88 MHZ	CFG_OUT0	CFG_OUT1	CFG_OUT3
77.76 MHz	VDD	VDD	CFG_OUT3
155.52 MHz	VSS	CFG_OUT1	CFG_OUT3

Output

The ACS8944 has a single, LVPECL, differential output (OUTN/P, pins 2 and 3).

The frequency of the output is determined by the wiring of OP_FSEL to the appropriate CFG_OUT pin in accordance with Table 5.

Table 5 Output Frequency Selection

For Output Frequency of	Connect OP_FSEL to
19.44 MHz	CFG_OUT3
38.88 MHZ	CFG_OUT2
77.76 MHz	CFG_OUT1
155.52 MHz	CFG_OUT0

Voltage Controlled Oscillator

The internal VCO operates at 2.48832 GHz and is internally divided down to the selected rate giving a precise 50/50 balanced mark/space ratio for the output.

Jitter Filtering

Input jitter is attenuated by the PLL with the frequency cut-off point (Fc) at which jitter is either tracked or attenuated being defined by the -3 dB point, i.e. the position of the first pole of the PLL loop filter. The bandwidth (frequency at which the first pole occurs) is defined by the component value selected for the filter from Table 6.

For 19.44 MHz input, using a loop filter bandwidth of 2 kHz gives:

- High input jitter attenuation and roll off:
  - - 20 dB/decade from first loop filter pole, (Fc)
  - - 40 dB/decade from 2nd pole (typically 10 x Fc)
- Jitter peaking is less than 1 dB (dependent on the loop filter components)
- Typical final output jitter, e.g. 2.8 ps rms measured over the integration range of 12 kHz-20 MHz offset from carrier.

Jitter Filtering: Partnering with Semtech Line Card Protection Part

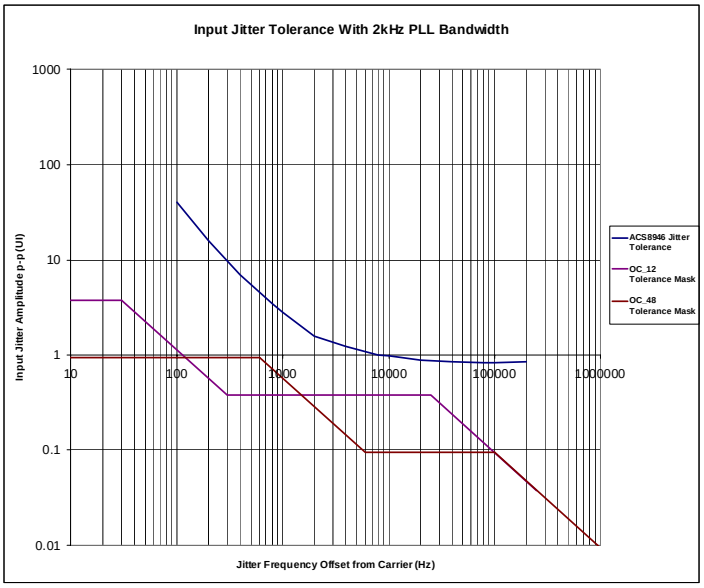
One “Real World” application for the ACS8944 is to use it to dejitter the clock output from a Semtech ACS8525 LC/P device. In this case it is recommended to set the ACS8944 PLL to a bandwidth of around 2 kHz to provide a low jitter total solution. The test results detailed in the electrical specifications section show the “Real World” performance of this combination of parts to be a superior solution when compared with those traditionally using simple discrete PLLs, and has the following advantages:

- Low overall bandwidth, 18 Hz for example—dictated by the ACS8525.
- High input jitter attenuation and roll-off:
- First, second and third order roll-off points:
  - - 20 dB/decade 18 Hz to 750 Hz,
  - - 40 dB/decade 750 Hz to 200 kHz and
  - - 60 dB/decade for >200 kHz.
- Typical final output jitter, e.g. 2.9 ps rms (measured over the integration range 12 kHz-20 MHz)—dictated by the ACS8944.
- High frequency stability when all input clocks fail; holdover frequency control to Stratum 3—dictated by the ACS8525.

Input Jitter Tolerance

Jitter tolerance is defined as the maximum amplitude of sinusoidal jitter that can exist on the input reference clock above which the device fails to maintain lock. For the ACS8944 device, the jitter tolerance is shown in Figure 3.

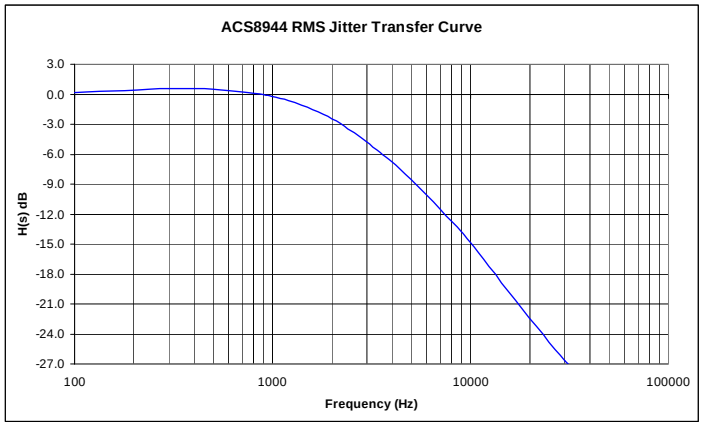
Figure 3 Jitter Tolerance; ACS8944 Standalone



Jitter Transfer

Jitter transfer is a ratio of input jitter present on the reference clock to the filtered jitter present on the output clock. Standalone, the Jitter Transfer Characteristic is defined solely by the loop filter bandwidth and is shown in Figure 4.

Figure 4 Jitter Transfer Characteristic, ACS8944 Stand-alone



In the combined solution, the ACS8525 device provides additional low frequency jitter filtering. The jitter transfer characteristic of the combined ACS8944 and ACS8525 is shown in Figure 5.

Figure 5 Jitter Transfer Characteristic, ACS8525 and ACS8944 combined

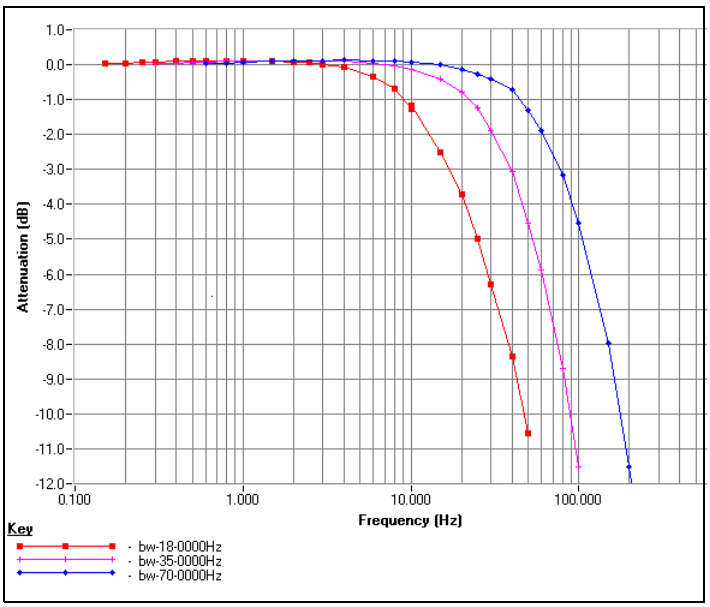
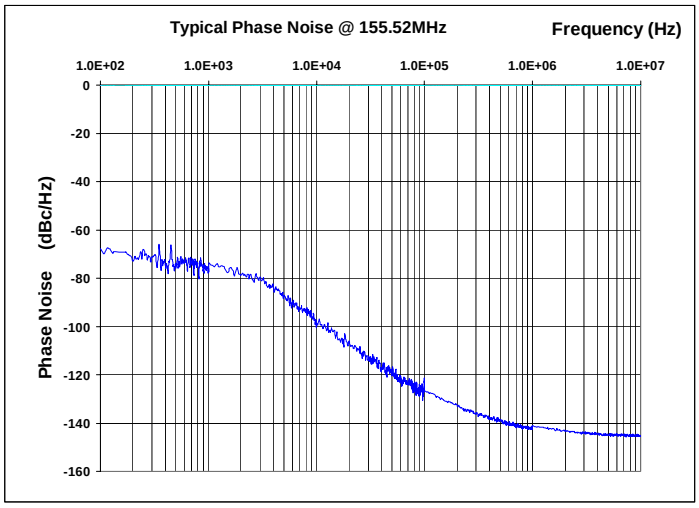
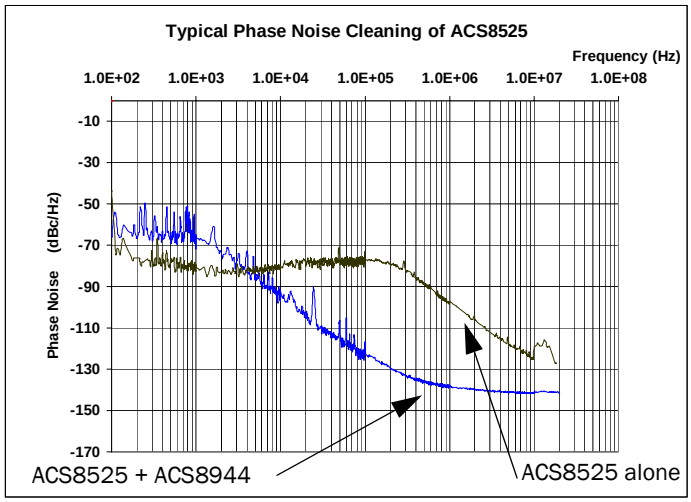


Figure 6 Phase Offset from Carrier, ACS8944



In the combined line card solution, the inherent jitter generated by the ACS8525 is attenuated by the ACS8944 as shown in the phase noise plot in Figure 7, which uses a PLL bandwidth of 2 kHz.

Figure 7 Phase Offset from Carrier, ACS8525 with/without ACS8944



Phase Noise Performance

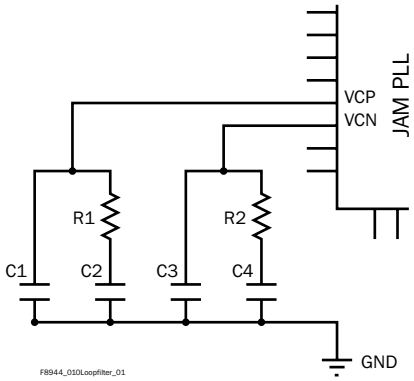
The inherent jitter generation by the ACS8944 is shown in the phase noise plot in Figure 6 for a PLL bandwidth of 2 kHz, output frequency of 155.52 MHz and input of 19.44 MHz.

Loop Filter Components

The loop filter comprises two identical sets of passive RC components that connect to the differential charge pump outputs and internal VCO control inputs. Pins VCN and

VCP are the combined differential charge pump outputs and VCO control voltage inputs. Figure 5 shows the arrangement.

Figure 8 Loop Filter Components



All electrolytic capacitors should be low leakage and low ESR (equivalent series resistance). Ceramic (preferred) or tantalum are suitable for C1 and C3.

Tables 6 and 7 are based on a damping factor of 1.2 (phase margin 80.2°). Higher damping factors may be used if lower transfer peaking is required. Contact Semtech Sales Support for further details.

Table 6 Loop Filter Components when using 19.44 MHz or 77.76 MHz Input Frequency

Closed Loop Bandwidth	R1 & R2	C2 & C4	C1 & C3
2 kHz	75 Ω	15 µF	100 nF
4 kHz	150 Ω	4.7 µF	33 nF
8 kHz	270 Ω	0.68 µF	7.5 nF
1.5 kHz	56 Ω	33 µF	200 nF

Table 7 Loop Filter Components when using 38.88 MHz or 155.52 MHz Input Frequency

Closed Loop Bandwidth	R1 & R2	C2 & C4	C1 & C3
2 kHz	150 Ω	6.8 µF	47 nF
4 kHz	300 Ω	2.2 µF	22 nF
8 kHz	560 Ω	0.47 µF	3.9 nF
1.5 kHz(i)	110 Ω	15 µF	91 nF

Note: (i) Not available at 155.52 MHz input frequency

Output Jitter

The output jitter meets all requirements of ITU, Telcordia and ETSI standards for SONET rates up to OC-12/STM-4/622.08 MHz. See the “Electrical Specifications” sections for details on the jitter figures across the different output jitter frequency bands relevant to each specification.

The recommended bandwidth of around 2 kHz is suitable for both meeting the specification on output jitter generation requirements and for filtering out the input jitter from the input clock.

System Reset

After power-up or a system reset via the RESETB (pin 40), the internal control logic waits for the presence of an input signal of approximately the correct frequency (at least 40% of the nominal) and then allows a further settling time of 60ms before allowing internal frequency tuning, frequency-locking and phase-locking on to the input clock. Consequently reset should be removed only when the input frequency is within 400 ppm of the nominal frequency.

Layout Recommendations

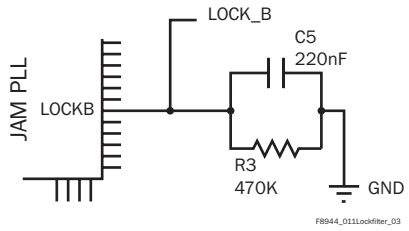
It is highly recommended to use a stable and filtered 3.3 V power supply to the device. A separate filtered power and ground plane is recommended with supply decoupling capacitors of 10 nF and 100 pF utilizing good high frequency chip capacitors (0402 or 0603 format surface-mount package) on each VDD. Good differential signal layout on the input and output lines should be used to ensure matched track impedance and phase. Contact Semtech directly for further layout recommendations.

Lock Detector

A simple lock detector is incorporated which combines the plus and minus phase errors from the phase detector, such that if any phase error signal is present, the LOCKB output drives out a +10 µA current, otherwise it is off.

Consequently this output (LOCKB) is a pulse width modulated (PWM) pulse stream whose mark/space ratio indicates the current input phase error. Filtering this signal with a simple external RC parallel filter as shown in Figure 9 will give a signal whose output level indicates PLL phase and frequency lock.

Figure 9 Lock Filter Components



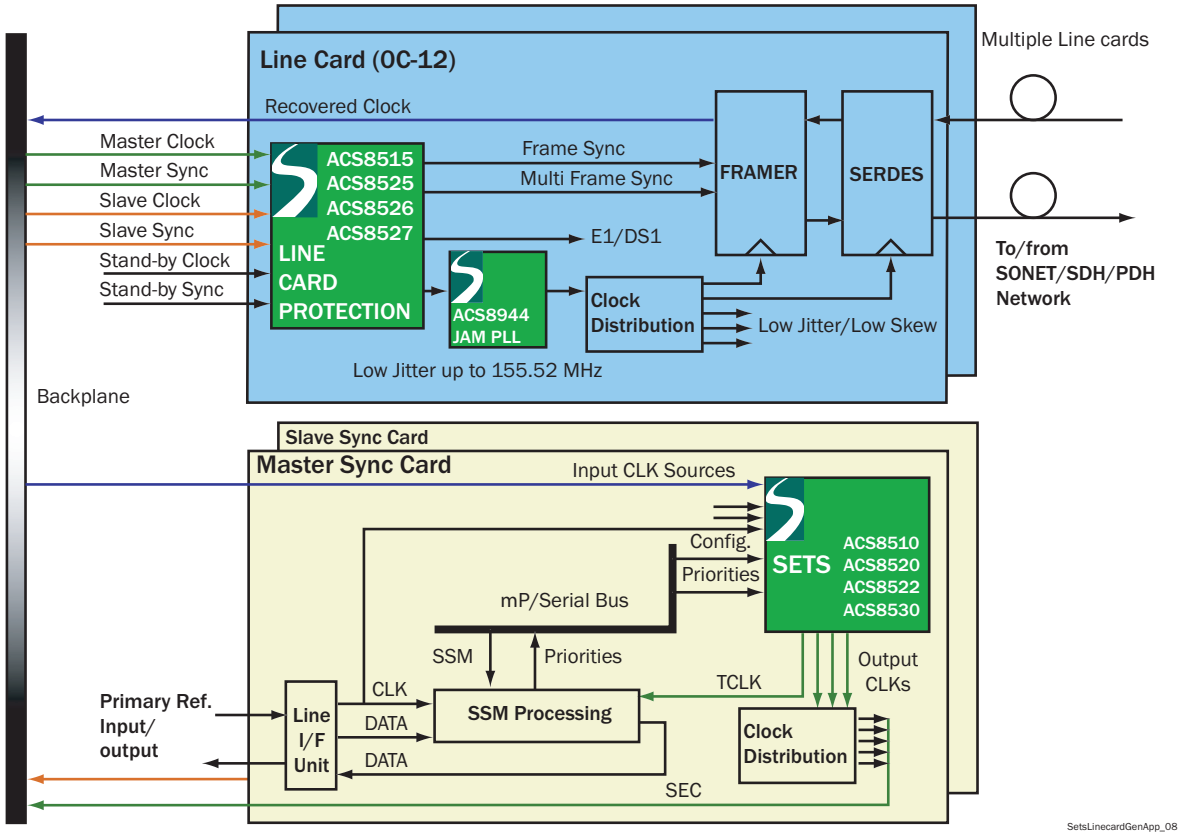
The filtering components are external so that the time to indicate lock or not locked can be optimized for the application. The output indicates both phase and frequency lock. During off-frequency conditions the LOCKB output will be predominately high in its PWM generation with the filtered version giving a constant high state.

Applications

The ACS8944 is targeted at applications requiring clock cleaning at 19.44 MHz, 38.88 MHz, 77.76 MHz or 155.52 MHz where input jitter is filtered out or attenuated at frequencies above the ACS8944 PLL bandwidth. It also performs the function of a clock multiplying unit (CMU) translating any one of these input frequencies to any one of 19.44 MHz, 38.88 MHz, 77.76 MHz or 155.52 MHz output frequencies.

The ACS8944 can save space when compared with discrete analog + VCXO solutions or module-based solutions. In the example in Figure 10 the ACS8944 is shown symbolically as a low cost line card dejittering device. The ACS8944 carries out the appropriate frequency multiplication for onward distribution as required by the line card.

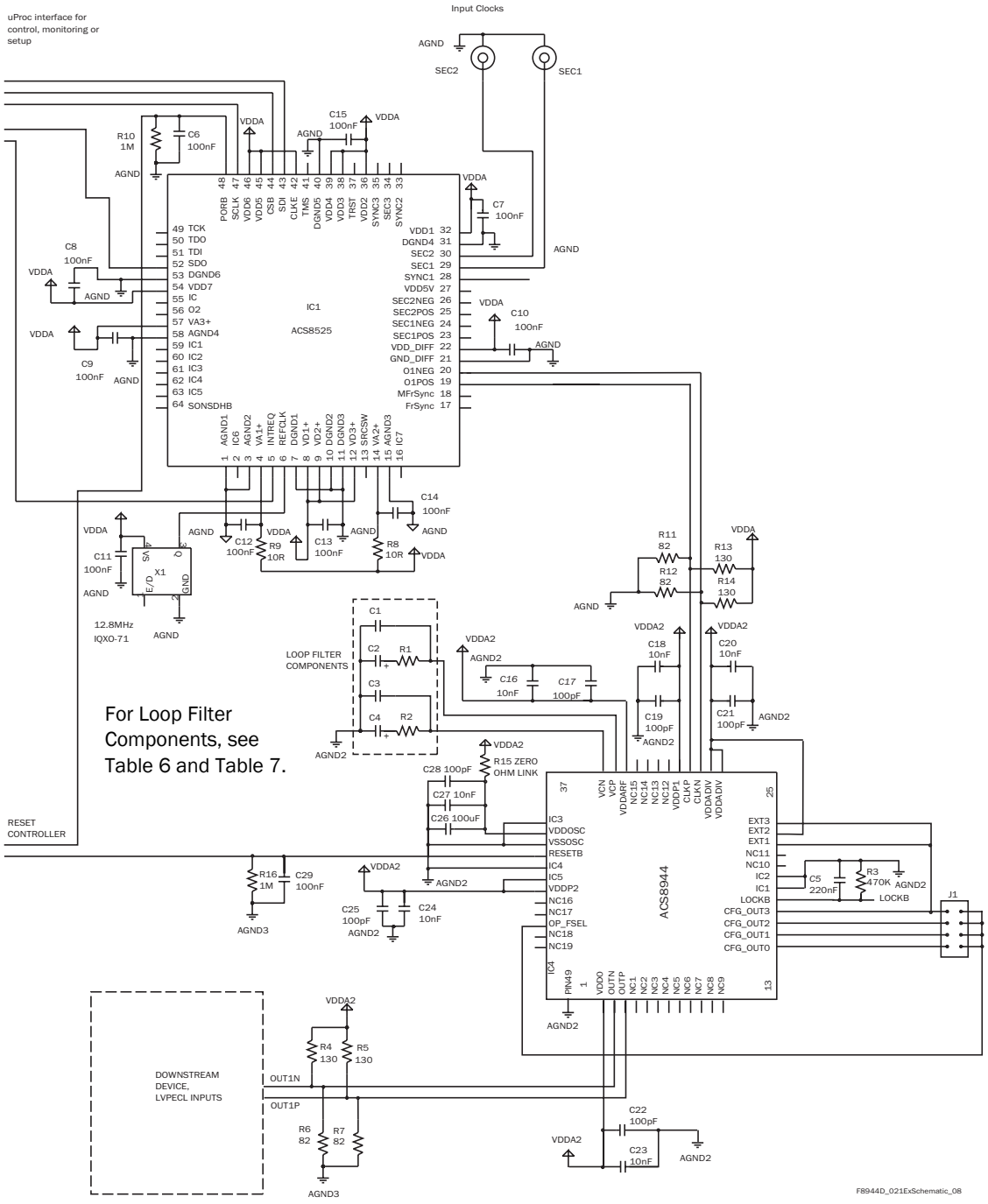
Figure 10 Typical Application



Application Schematic of Combined ACS8525 and ACS8944

Figure 11 shows the circuit diagram of the clock solution part of an application combining an ACS8525 line card part with a dejittering ACS8944. A full design would require a microcontroller for advanced control and ACS8525 device setup; an ACS8525 line card protection device containing DPLLs/APLLs, synthesizers and monitors and the ACS8944 for jitter reduction. Just the parts relevant to the clock production are shown here, i.e. the ACS8525 and ACS8944.

Figure 11 Line Card Clock Source Example Schematic ACS8525 and ACS8944



Note...For optimal performance use a Low Voltage Dropout (LDO) Regulator to supply VDDA2

Maximum Ratings

Important Note: The Absolute Maximum Ratings, Table 8, are stress ratings only, and functional operation of the device at conditions other than those indicated in the Operating Conditions sections of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

Table 8 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage (D.C.): VDDP1, VDDP2, VDDADIV, VDDARF, VDDOSC, VDDO	V_{DD}	-0.5	3.6	V
Input Voltage (non-supply pins): Digital Inputs: EXT1, EXT2, RESETB, OP_FSEL	V_{IN}	-0.5	5.5	V
Input Voltage (non-supply pins) LVPECL Inputs: CLKN, CLKP, ANALOG I/O: VCN, VCP, LOCKB	V_{IN}	-0.5	V_{DD} + 0.5	V
Output Voltage (non-supply pins): Digital Outputs:FREQ155, FREQ77, FREQ38, FREQ19 LVPECL Outputs: OUTN, OUTP	V_{OUT}	-0.5	V_{DD} + 0.5	V
Ambient Operating Temperature Range	T_A	-40	+85	°C
Storage Temperature	T_{STOR}	-50	+150	°C
Reflow Temperature (Pb)	T_{REPB}	-	245	°C
Reflow Temperature (Pb Free)	$T_{REPBFREE}$	-	260	°C
ESD HBM (Human Body Model)[(i), (ii)]	ESD_{HBM}	2	-	kV
Latchup[(iii)]	I_{LU}	±100	-	mA

Notes: (i) All pins pass 2kV HBM except VCN/VCP which are rated at 500 V HBM.

(ii) Tested to JEDEC standard JESD22-A114.

(iii) Tested to JEDEC standard JESD78.

Operating Conditions

Table 9 Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply Voltage (D.C.): VDDP1, VDDP2, VDDADIV, VDDARF, VDDO	V_{DD}	3.135	3.3	3.465	V
VDDOSC	V_{DDOSC}	3.0	3.3	3.465	V
Ambient Temperature Range	T_A	-40	-	+85	°C
Supply Current (including VDDOSC)	I_{DD}	-	250	300	mA
VDDOSC Supply Current	I_{DDOSC}	-	20	25	mA

Table 9 Operating Conditions (cont...)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Total Power Dissipation (excluding power dissipation in external biasing components	P_{TOT}	-	870	1040	mW

Thermal Characteristics

Table 10 Thermal Conditions

Parameter	Symbol	Minimum	Maximum	Units
Thermal Resistance Junction to Ambient	θ_{JA}	-	25	°C/W
Operating Junction Temperature	T_{JCT}	-	125	°C

AC Characteristics

Table 11 AC Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input to Output Delay	t_{PDIO}	0.5	-	3.0	ns
Input Clock Rise/Fall Time[(i)] (CLK)	t_{CRF}	-	-	10	ns
LVPECL Output Rise/Fall Time[(i), (ii)]	t_{PECLRF}	-	0.8	1.2	ns
Input Clock Duty Cycle (CLK)	t_{CDF}	40	50	60	%
Output Clock Duty Cycle	t_{ODC}	48	50	52	%
RESETB Pulse Width after Power-up	t_{RPW}	-	-	100	ms
Frequency Tuning after RESETB High	t_{FT}	-	-	60	ms

Notes: (i) Rise/fall time measured 10-90%.
(ii) Using output load specified in Figure 14.

DC Characteristics

Across all operating conditions, unless otherwise stated.

Table 12 DC Characteristics: LVCMOS Inputs with Internal Pull-down/Schmitt input with Internal Pull-up

Parameter	Symbol	Minimum	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	V
V_{IN} *Low*	V_{IL}	-	0.8	V
Pull-down Resistor	R_{PD}	43	108	kΩ
Pull-up Resistor (Schmitt input)	R_{PU}	53	113	kΩ
Input Current	I_{IN}	-	±10	µA

Table 13 DC Characteristics: LVPECL Input Port

Parameter	Symbol	Minimum	Maximum	Units
LVPECL Input Offset Voltage Differential Inputs (Note (ii))	V_{IO_LVPECL}	V_{DD}-2.0	V_{DD}-0.5	V
Input Differential Voltage	V_{ID_LVPECL}	0.1	1.4	V
LVPECL Input Low Voltage Single-ended Input (Note (i))	$V_{IL\_LVPECL\_S}$	V_{SS}	V_{DD}-1.5	V
LVPECL Input High Voltage Single-ended Input (Note (i))	$V_{IL\_LVPECL\_S}$	V_{DD}-1.3	V_{DD}	V
Input High Current Input Differential Voltage V_{ID} = 1.4 V	I_{IH_LVPECL}	-10	+10	µA
Input Low Current Input Differential Voltage V_{ID} = 1.4 V	I_{IL_LVPECL}	-10	+10	µA

Notes: (i) Unused differential input terminated to VDD-1.4 V.

(ii) Both pins must remain within the supply voltage, i.e. >V_{SS} and <V_{DD}.

Table 14 DC Characteristics: LVPECL Output Port

Parameter	Symbol	Minimum	Maximum	Units
LVPECL Output Low Voltage (Note (i))	V_{OL_LVPECL}	V_{DD}-2.1	V_{DD}-1.62	V
LVPECL Output High Voltage (Note (i))	V_{OH_LVPECL}	V_{DD}-1.45	V_{DD}-0.88	V
LVPECL Output Differential Voltage (Note (i))	V_{OD_LVPECL}	0.37	1.22	V

Note: (i) With a 50 ohms load on each pin to V_{DD} -2V.

Table 15 DC Characteristics: LVTTL/CMOS Output Port

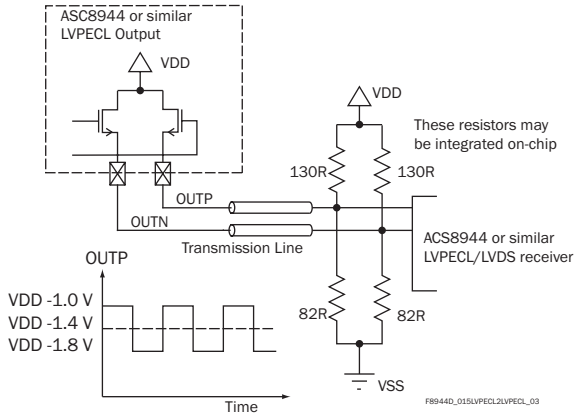
Parameter	Symbol	Minimum	Typical	Maximum	Units
Output Low Voltage @ I_{OL} (MAX)	V_{OL}	-	-	0.4	V
Output High Voltage @ I_{OH} (MIN)	V_{OH}	2.4	-	-	V
Low Level Output Current @ V_{OL} = 0.4 V	I_{OL}	2	-	-	mA
High Level Output Current @ V_{OH} = 2.4 V	I_{OH}	2	-	-	mA

Input and Output Interface Terminations

Interfacing to either the same type or electrically different interface types is illustrated by the following circuit diagrams, covering translation from LVDS to LVPECL.

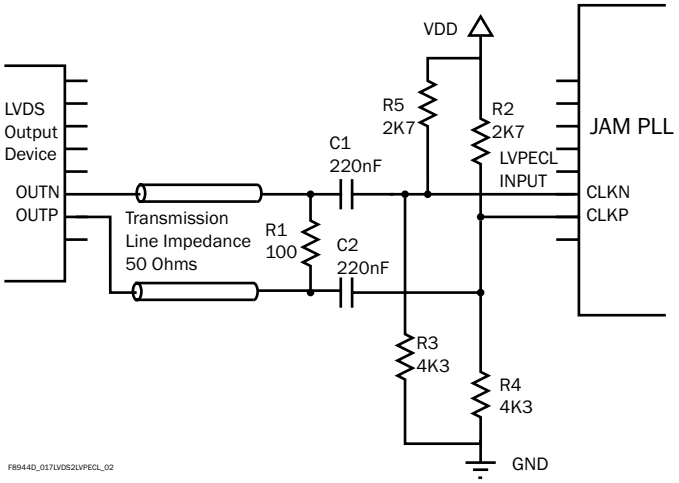
The example of Figure 12 shows LVPECL to LVPECL terminations with D.C. coupling, so that the ACS8944 sees an equivalent load of around 50 Ω from the R3, R4, R5, R6 resistor arrangement at the receiver end.

Figure 12 LVPECL Output - DC Coupled to LVPECL or LVDS Receiver



The preferred termination circuitry for the LVDS signals between the ACS8525/26/27 and the ACS8944 LVPECL is shown in Figure 13. The bias for the LVPECL input is set for A.C. inputs at a mid point of approximately 2 V (with a 3.3 V VDD), as opposed to a normal D.C. coupled bias of VDD - 2 V. This is due to the push-pull nature of an A.C. coupled signal.

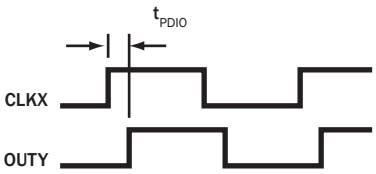
Figure 13 Generic LVDS - AC Coupled to LVPECL Receiver



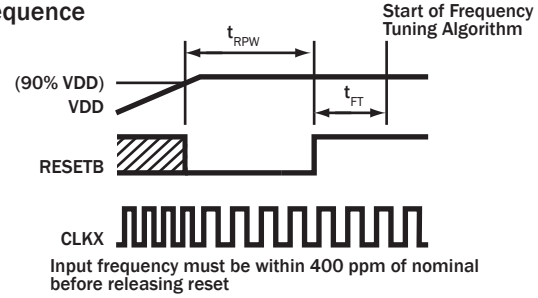
Input/Output Timing

Figure 14 Timing Diagrams

1) **Input to Output Delay**



2) **Power-up Sequence**



Jitter Performance

Table 16 Output Jitter Generation: ACS8944 Stand-alone @155.52 MHz Input/155.52 MHz Output

Test Definition				Measured Results		
Specification	**Interface Frequency**	**Filter Spec (iv)**	**Spec Limit**	**Typical**	**Max**	**Units**
G.813 Option 1[4], and ETSI EN 300 462 - 7 - 1[1]	STM-1 (optical) 155 MHz	65 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 5.1	12.5	ps p-p
			-	0.5	1.2	ps rms
		500 Hz to 1.3 MHz	0.5 UI p-p = 3215 ps	* 110.4	302.8	ps p-p
			-	11.0	30.3	ps rms
	STM-4 622 MHz	250 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 3.2	5.3	ps p-p
			-	0.3	0.5	ps rms
		1 kHz to 5 MHz	0.5 UI p-p = 804 ps	* 82.4	213.0	ps p-p
			-	8.2	21.3	ps rms
	STM-16 2.5 GHz	1 MHz to 20 MHz	0.1 UI p-p = 40 ps	* 3.7	6.3	ps p-p
			-	0.4	0.6	ps rms
		5 kHz to 20 MHz	0.5 UI p-p = 201 ps	* 33.7	90.3	ps p-p
			-	3.4	9.0	ps rms
ETSI EN 300 462 - 7 - 1[1]	STM-1 (electrical) 155 MHz	65 kHz to 1.3 MHz	0.075 UI p-p = 482 ps	* 5.1	12.5	ps p-p
			-	0.5	1.2	ps rms
G.813 Option 2[4]	STM-1 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 18.1	52.4	ps p-p
			-	1.8	5.2	ps rms
	STM-4 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 18.2	47.9	ps p-p
			-	1.8	4.8	ps rms
	STM-16 2.5 GHz	12 kHz to 20 MHz	0.1 UI p-p = 40 ps	* 18.4	48.4	ps p-p
				1.8	4.8	ps rms
GR-253-CORE[8]	OC-3/STS-3 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 18.1	52.4	ps p-p
			0.01 UI rms = 64.3 ps	1.8	5.2	ps rms
	OC-12/STS-12 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 18.2	47.9	ps p-p
			0.01 UI p-p = 16.1 ps	1.8	4.8	ps rms
	OC-48/STS-48 2.5 GHz	5 kHz to 20 MHz	1.5 UI p-p = 600 ps	* 33.7	90.3	ps p-p
			-	3.4	9.0	ps rms
		1 MHz to 20 MHz	0.15 UI p-p = 60 ps	* 3.7	6.3	ps p-p
			-	0.4	0.6	ps rms

Notes: (i) Measured on the ACS8944 Evaluation Board using output clock OUT1, with a 0 dBm reference clock from an ESG E4400B signal generator AC coupled to CLK1. VDD = 3.0 V to 3.465 V, T_A -40 °C to +85 °C.

(ii) "" Derived values using the normal Gaussian crest value ratio of 10.*

(iii) PLL Closed Loop bandwidth set to 2 KHz with a damping factor of 1.2.

(iv) All measurement results are derived from the phase noise plots using integration ranges defined by the telecommunication standards' specifications

Table 17 Output Jitter Generation: ACS8944 Stand-alone @77.76 MHz Input/155.52 MHz Output

Test Definition				Measured Results		
Specification	**Interface Frequency**	**Filter Spec (Iv)**	**Spec Limit**	**Typical**	**Max**	**Units**
G.813 Option 1[4], and ETSI EN 300 462 - 7 - 1[1]	STM-1 (optical) 155 MHz	65 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 5.1	12.3	ps p-p
			-	0.5	1.2	ps rms
		500 Hz to 1.3 MHz	0.5 UI p-p = 3215 ps	* 102.6	281.3	ps p-p
			-	10.3	28.1	ps rms
	STM-4 622 MHz	250 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 3.2	5.4	ps p-p
			-	0.3	0.5	ps rms
		1 kHz to 5 MHz	0.5 UI p-p = 804 ps	* 76.6	197.8	ps p-p
			-	7.7	19.8	ps rms
	STM-16 2.5 GHz	1 MHz to 20 MHz	0.1 UI p-p = 40 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms
		5 kHz to 20 MHz	0.5 UI p-p = 201 ps	* 32.7	87.5	ps p-p
			-	3.3	8.7	ps rms
ETSI EN 300 462 - 7 - 1[1]	STM-1 (electrical) 155 MHz	65 kHz to 1.3 MHz	0.075 UI p-p = 482 ps	* 5.1	12.3	ps p-p
			-	0.5	1.2	ps rms
G.813 Option 2[4]	STM-1 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 17.5	50.8	ps p-p
			-	1.7	5.1	ps rms
	STM-4 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 17.6	46.4	ps p-p
			-	1.8	4.6	ps rms
	STM-16 2.5 GHz	12 kHz to 20 MHz	0.1 UI p-p = 40 ps	* 17.8	46.9	ps p-p
				1.8	4.7	ps rms
GR-253-CORE[8]	OC-3/STS-3 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 17.5	50.8	ps p-p
			0.01 UI rms = 64.3 ps	1.7	5.1	ps rms
	OC-12/STS-12 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 17.6	46.4	ps p-p
			0.01 UI p-p = 16.1 ps	1.8	4.6	ps rms
	OC-48/STS-48 2.5 GHz	5 kHz to 20 MHz	1.5 UI p-p = 600 ps	* 32.7	87.5	ps p-p
			-	3.3	8.7	ps rms
		1 MHz to 20 MHz	0.15 UI p-p = 60 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms

Notes: (i) Measured on the ACS8944 Evaluation Board using output clock OUT1, with a 0 dBm reference clock from an ESG E4400B signal generator AC coupled to CLK1. VDD = 3.0 V to 3.465 V, T_A -40 °C to +85 °C.

(ii) "" Derived values using the normal Gaussian crest value ratio of 10.*

(iii) PLL Closed Loop bandwidth set to 2 KHz with a damping factor of 1.2.

(iv) All measurement results are derived from the phase noise plots using integration ranges defined by the telecommunication standards' specifications.

Table 18 Output Jitter Generation: ACS8944 Stand-alone @38.88 MHz Input/155.52 MHz Output

Test Definition				Measured Results		
Specification	**Interface Frequency**	**Filter Spec (Iv)**	**Spec Limit**	**Typical**	**Max**	**Units**
G.813 Option 1[4], and ETSI EN 300 462 - 7 - 1[1]	STM-1 (optical) 155 MHz	65 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 5.3	12.9	ps p-p
			-	0.5	1.3	ps rms
		500 Hz to 1.3 MHz	0.5 UI p-p = 3215 ps	* 111.1	304.7	ps p-p
			-	11.1	30.5	ps rms
	STM-4 622 MHz	250 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 3.3	5.4	ps p-p
			-	0.3	0.5	ps rms
		1 kHz to 5 MHz	0.5 UI p-p = 804 ps	* 86.9	224.5	ps p-p
			-	8.7	22.4	ps rms
	STM-16 2.5 GHz	1 MHz to 20 MHz	0.1 UI p-p = 40 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms
		5 kHz to 20 MHz	0.5 UI p-p = 201 ps	* 33.7	100.0	ps p-p
			-	3.7	10.0	ps rms
ETSI EN 300 462 - 7 - 1[1]	STM-1 (electrical) 155 MHz	65 kHz to 1.3 MHz	0.075 UI p-p = 482 ps	* 5.3	12.9	ps p-p
			-	0.5	1.3	ps rms
G.813 Option 2[4]	STM-1 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 19.3	56.1	ps p-p
			-	1.9	5.6	ps rms
	STM-4 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 19.5	51.2	ps p-p
			-	1.9	5.1	ps rms
	STM-16 2.5 GHz	12 kHz to 20 MHz	0.1 UI p-p = 40 ps	* 19.6	51.7	ps p-p
				2.0	5.2	ps rms
GR-253-CORE[8]	OC-3/STS-3 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 19.3	56.1	ps p-p
			0.01 UI rms = 64.3 ps	1.9	5.6	ps rms
	OC-12/STS-12 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 19.5	51.2	ps p-p
			0.01 UI p-p = 16.1 ps	1.9	5.1	ps rms
	OC-48/STS-48 2.5 GHz	5 kHz to 20 MHz	1.5 UI p-p = 600 ps	* 37.3	100.0	ps p-p
			-	3.7	10.0	ps rms
		1 MHz to 20 MHz	0.15 UI p-p = 60 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms

Notes: (i) Measured on the ACS8944 Evaluation Board using output clock OUT1, with a 0 dBm reference clock from an ESG E4400B signal generator AC coupled to CLK1. VDD = 3.0 V to 3.465 V, T_A -40 °C to +85 °C.

(ii) "" Derived values using the normal Gaussian crest value ratio of 10.*

(iii) PLL Closed Loop bandwidth set to 2 KHz with a damping factor of 1.2.

(iv) All measurement results are derived from the phase noise plots using integration ranges defined by the telecommunication standards' specifications.

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Table 19 Output Jitter Generation: ACS8944 Stand-alone @19.44 MHz Input/155.52 MHz Output

Test Definition				Measured Results		
Specification	**Interface Frequency**	**Filter Spec (Iv)**	**Spec Limit**	**Typical**	**Max**	**Units**
G.813 Option 1[4], and ETSI EN 300 462 - 7 - 1[1]	STM-1 (optical) 155 MHz	65 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 6.6	16.0	ps p-p
			-	0.7	1.6	ps rms
		500 Hz to 1.3 MHz	0.5 UI p-p = 3215 ps	* 137.1	376.0	ps p-p
			-	13.7	37.6	ps rms
	STM-4 622 MHz	250 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 3.4	5.6	ps p-p
			-	0.3	0.6	ps rms
		1 kHz to 5 MHz	0.5 UI p-p = 804 ps	* 117.5	303.5	ps p-p
			-	11.7	30.3	ps rms
	STM-16 2.5 GHz	1 MHz to 20 MHz	0.1 UI p-p = 40 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms
		5 kHz to 20 MHz	0.5 UI p-p = 201 ps	* 55.9	149.6	ps p-p
			-	5.6	15.0	ps rms
ETSI EN 300 462 - 7 - 1[1]	STM-1 (electrical) 155 MHz	65 kHz to 1.3 MHz	0.075 UI p-p = 482 ps	* 6.6	16.0	ps p-p
			-	0.7	1.6	ps rms
G.813 Option 2[4]	STM-1 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 27.8	80.6	ps p-p
			-	2.8	8.1	ps rms
	STM-4 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 27.9	73.3	ps p-p
			-	2.8	7.3	ps rms
	STM-16 2.5 GHz	12 kHz to 20 MHz	0.1 UI p-p = 40 ps	* 28.0	73.6	ps p-p
				2.8	7.4	ps rms
GR-253-CORE[8]	OC-3/STS-3 155 MHz	12 kHz to 1.3 MHz	0.1 UI p-p = 643 ps	* 27.8	80.6	ps p-p
			0.01 UI rms = 64.3 ps	2.8	8.1	ps rms
	OC-12/STS-12 622 MHz	12 kHz to 5 MHz	0.1 UI p-p = 161 ps	* 27.9	73.3	ps p-p
			0.01 UI p-p = 16.1 ps	2.8	7.3	ps rms
	OC-48/STS-48 2.5 GHz	5 kHz to 20 MHz	1.5 UI p-p = 600 ps	* 55.9	149.6	ps p-p
			-	5.6	15.0	ps rms
		1 MHz to 20 MHz	0.15 UI p-p = 60 ps	* 3.7	6.2	ps p-p
			-	0.4	0.6	ps rms

Notes: (i) Measured on the ACS8944 Evaluation Board using output clock OUT1, with a 0 dBm reference clock from an ESG E4400B signal generator AC coupled to CLK1. VDD = 3.0 V to 3.465 V, T_A -40 °C to +85 °C.

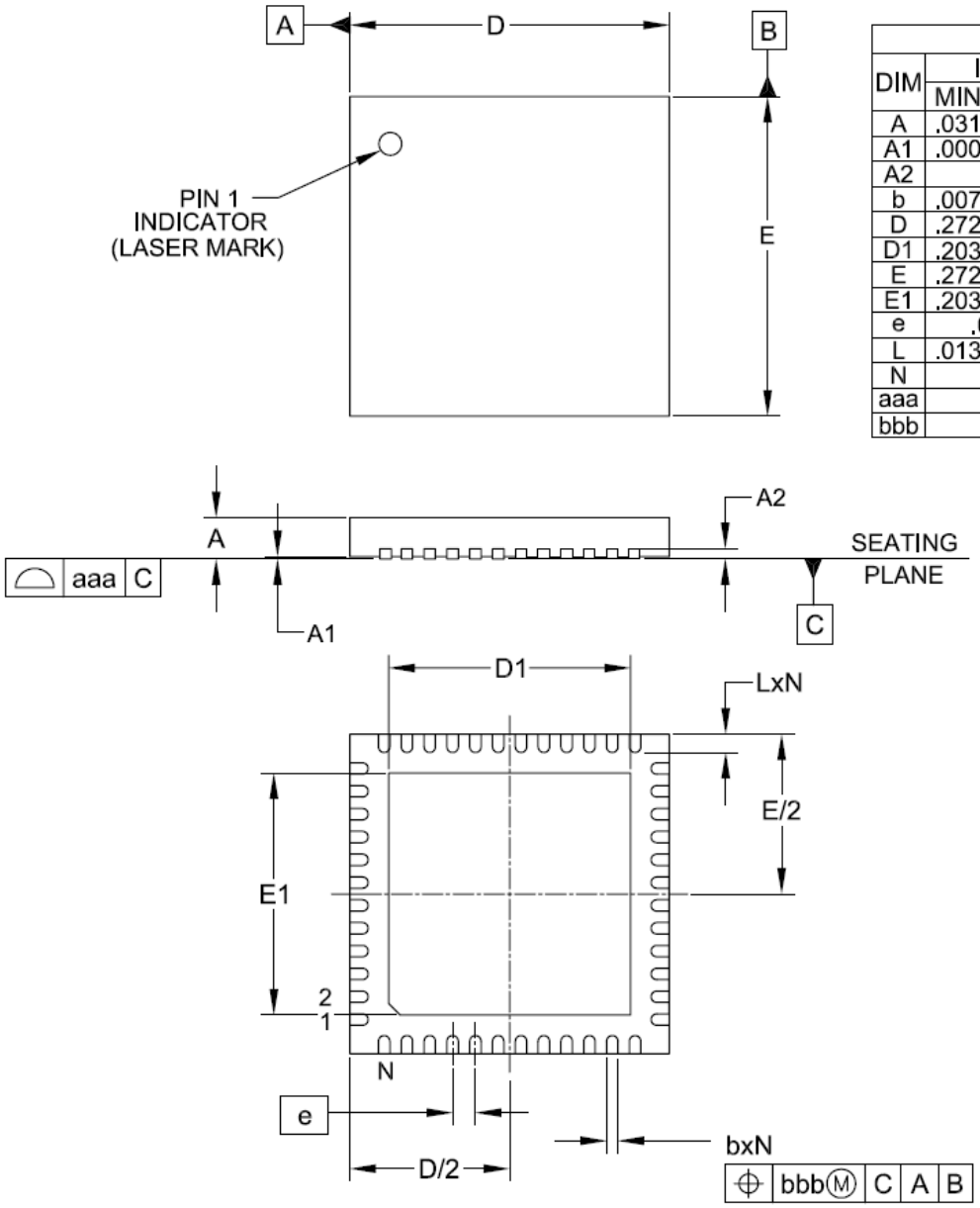
(ii) "" Derived values using the normal Gaussian crest value ratio of 10.*

(iii) PLL Closed Loop bandwidth set to 2 KHz with a damping factor of 1.2.

(iv) All measurement results are derived from the phase noise plots using integration ranges defined by the telecommunication standards' specifications.

Package Information

Figure 15 QFN48 Package.



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2		(.008)			(0.20)	
b	.007	.009	.012	0.18	0.23	0.30
D	.272	.276	.280	6.90	7.00	7.10
D1	.203	.209	.213	5.15	5.30	5.40
E	.272	.276	.280	6.90	7.00	7.10
E1	.203	.209	.213	5.15	5.30	5.40
e		.020 BSC			0.50 BSC	
L	.013	.016	.018	0.35	0.40	0.45
N		48			48	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

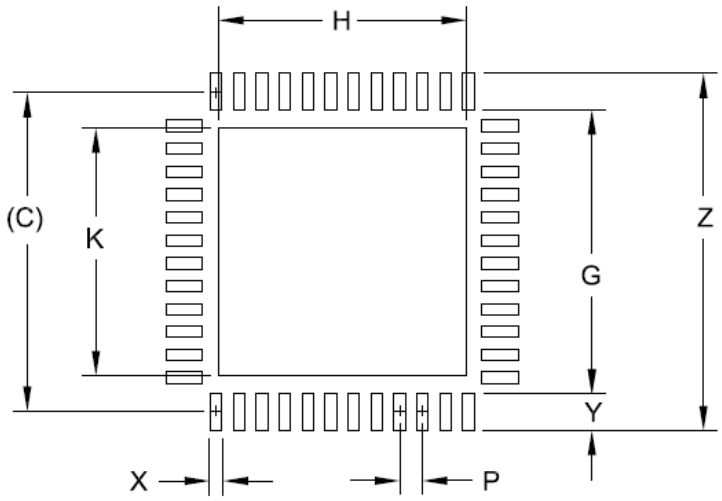
Thermal Conditions

The device is rated for full temperature range when this package is used with a 4-layer or more PCB. Copper coverage must exceed 50%. All pins must be soldered to the PCB. Maximum operating temperature must be reduced when the device is used with a PCB with less than these requirements.

The device includes a large thermal die paddle which must be soldered to the PCB in addition to the pins for improved thermal dissipation characteristics and to strengthen the mechanical connection to the PCB.

Although not essential for the ACS8944, one technique that may be used to improve heat dissipation from through the large centre pad is to include a thermal landing the same size as the centre pad on the component side of the board (and one on the opposite side of the PCB) connected to analog ground using a number of thermal vias, approximately 0.33mm diameter. These vias should be completely connected (flooded over) to the thermal landing(s) as well as to internal ground planes if using a multilayer PCB. 3 x 3 vias pitched at 1.27 mm between via centres would be more than sufficient for the ACS8944 if this method were adopted.

Figure 16 Typical 48 Pin QFN PCB Footprint



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.274)	(6.95)
G	.240	6.10
H	.213	5.40
K	.213	5.40
P	.021	0.50
X	.010	0.25
Y	.033	0.85
Z	.307	7.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
3. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.

Abbreviations

CMU	Clock Multiplier Unit
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
HBM	Human Body Model
I/O	Input/Output
JAM PLL	Jitter Attenuating, Multiplying Phase Locked Loop
LDO	Low Voltage Drop-out
LVCMOS	Low Voltage CMOS
LVDS	Low Voltage Differential Signal
LVPECL	Low Voltage (3.3 V) PECL
OC-3/12	Optical Carrier Signal Level 3/12 155.52 Mbps/ 622.08 Mbps
PECL	Positive Emitter Coupled Logic
PFD	Phase and Frequency Detector
PLL	Phase Locked Loop
POR	Power-On Reset
p-p	peak-to-peak
PWM	Pulse Width Modulated
rms	root-mean-square
RoHS	Restrictive Use of Certain Hazardous Substances (directive)
SDH	Synchronous Digital Hierarchy
SEC	SDH/SONET Equipment Clock
SETS	Synchronous Equipment Timing source
SONET	Synchronous Optical Network
STM-1/4/16	Synchronous Transport Module Levels 1/4: 155.52 Mbps/ 622.08 Mbps/ 2.488 Gbps (SDH)
STS-12	Synchronous Transport Signal Level: 12, 622.08 Mbps (SONET)
UI	Unit Interval
uP (µP)	Microprocessor
WEEE	Waste Electrical and Electronic Equipment (directive)
VCO	Voltage Controlled Oscillator

References and Related Standards

[1] ETSI EN 300 462-7-1 v1.1.2 (06/2001)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 7-1: Timing characteristics of slave clocks suitable for synchronization supply to equipment in local node applications

[2] ETSI EN 302 084 V1.1.1 (2000-02)
Transmission and Multiplexing (TM); The control of jitter and wander in transport networks

[3] ITU-T G.812 (06/1998)
Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

[4] ITU-T G.813 (08/1996)
Timing characteristics of SDH equipment slave clocks (SEC)

[5] ITU-T G.823 (03/2000)
The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy

[6] ITU-T G.824 (03/2000)
The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

[7] ITU-T G.825 (03/2000)
The control of jitter and wander within digital networks which are based on the Synchronous Digital Hierarchy (SDH)

[8] Telcordia GR-253-CORE, Issue 3 (09/ 2000)
Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria

[9] RoHS Directive 2002/95/EC: Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

[10] Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC): Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE)

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Revision Status/History

The Revision Status, as shown in top center of the datasheet header bar, may be DRAFT, PRELIMINARY, or FINAL, and refers to the status of the device (not the datasheet), within the design cycle. DRAFT status is used when the design is being realized but is not yet physically available, and the datasheet content reflects the intention of the design. The datasheet is raised to PRELIMINARY status when initial prototype devices are physically available, and the datasheet content more accurately represents the realization of the design. The datasheet is only raised to FINAL status after the device has been fully characterized, and the datasheet content updated with measured, rather than simulated parameter values.

This is a “FINAL” release of the ACS8944 datasheet. Changes made for this document revision are given below.

Table 20 Revision History

Revision	Reference	Description of Changes
Rev. 0.01/October 2004 to Rev. 0.10/May 2006	See version 0.09, April 2006	Initial drafts, for details see Revision Status/History in version 0.09.
Rev. 1.00/May 2006	All pages	Updated to Preliminary status.
Rev. 2.00/October 2006	All pages	Updated to Final status.
Rev. 3/November 2006	All pages	Revision scheme updated.

Notes

Ordering Information

Table 21 Parts List

Part Number	Description
ACS8944	JAM PLL Jitter Attenuating, Multiplying Phase Locked Loop for OC-12/STM-4.
ACS8944T	Lead (Pb)-free packaged version of ACS8944; RoHS and WEEE compliant.
ACS8944EVB	ACS8944 Evaluation Board (Demo Board).

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Life support- This product is not designed or intended for use in life support equipment, devices or systems, or other critical applications. This product is not authorized or warranted by Semtech for such use.

Right to change- Semtech Corporation reserves the right to make changes, without notice, to this product. Customers are advised to obtain the latest version of the relevant information before placing orders.

Compliance to relevant standards- Operation of this device is subject to the User's implementation and design practices. It is the responsibility of the User to ensure equipment using this device is compliant to any relevant standards.

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