ALPHA & OMEGA SEMICONDUCTOR
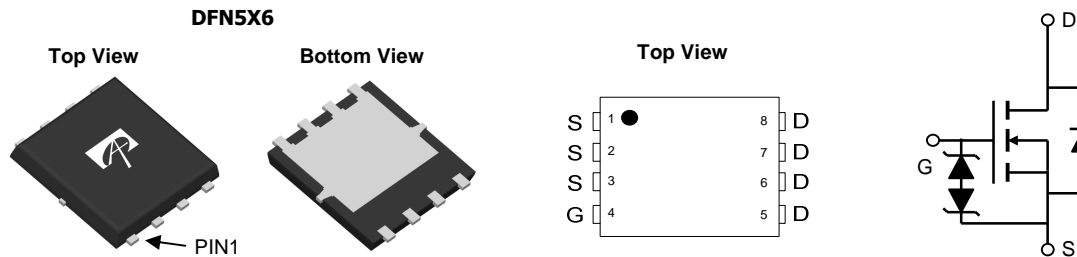
AON6404
30V N-Channel MOSFET

General Description

The AON6404 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

Product Summary

V_{DS} (V) = 30V
I_D = 85A (V_{GS} = 10V)
$R_{DS(ON)}$ < 2.2mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 3.8mΩ (V_{GS} = 4.5V)

 ESD protected
100% UIS Tested
100% Rg Tested

Green Product

DFN5X6

Top View   **Bottom View**

PIN1

Top View

```
S [ 1 ●      8 ] D
S [ 2        7 ] D
S [ 3        6 ] D
G [ 4        5 ] D
```


Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [B,G]	T_C=25℃	I_D	85	A
	T_C=100℃		67	
Pulsed Drain Current		I_{DM}	160	
Continuous Drain Current [A]	T_A=25℃	I_{DSM}	25	
	T_A=70℃		20	
Avalanche Current		I_{AS}	85	
Single avalanche energy L=0.1mH		E_{AS}	361	mJ
Power Dissipation [B]	T_C=25℃	P_D	83	W
	T_C=100℃		33	
Power Dissipation [A]	T_A=25℃	P_{DSM}	2.1	W
	T_A=70℃		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	15	20	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		45	60	℃/W
Maximum Junction-to-Case [C]	Steady-State	$R_{\theta JC}$	1.1	1.5	℃/W

Electrical Characteristics (T$_J$=25℃ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250µA, V$_{GS}$=0V		30	34		V
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=30V, V$_{GS}$=0V				1	uA
			T$_J$=55℃			5	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$= ±16V				10	uA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=V$_{GS}$ I$_D$=250µA		1.4	1.7	2	V
I$_{D(ON)}$	On state drain current	V$_{GS}$=10V, V$_{DS}$=5V		160			A
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=20A			1.8	2.2	mΩ
			T$_J$=125℃		2.5	3.1	
		V$_{GS}$=4.5V, I$_D$=20A			3	3.8	mΩ
g$_{FS}$	Forward Transconductance	V$_{DS}$=5V, I$_D$=20A			75		S
V$_{SD}$	Diode Forward Voltage	I$_S$=85A,V$_{GS}$=0V			0.87	1.3	V
I$_S$	Maximum Body-Diode Continuous Current					85	A
DYNAMIC PARAMETERS							
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=15V, f=1MHz			7420	9000	pF
C$_{oss}$	Output Capacitance				1045		pF
C$_{rss}$	Reverse Transfer Capacitance				720		pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz			1.2	1.8	Ω
SWITCHING PARAMETERS							
Q$_g$(10V)	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=15V, I$_D$=20A			118	155	nC
Q$_g$(4.5V)	Total Gate Charge				54		nC
Q$_{gs}$	Gate Source Charge				29		nC
Q$_{gd}$	Gate Drain Charge				22		nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=15V, R$_L$=0.75Ω, R$_{GEN}$=3Ω			17		ns
t$_r$	Turn-On Rise Time				18		ns
t$_{D(off)}$	Turn-Off DelayTime				67		ns
t$_f$	Turn-Off Fall Time				25		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=20A, dI/dt=100A/µs			60	80	ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=20A, dI/dt=100A/µs			66		nC

A: The value of R$_{θJA}$ is measured with the device in a still air environment with T$_A$=25℃, with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with T A=25°

B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsink is used.

C: Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=150℃.

D. The R$_{θJA}$ is the sum of the thermal impedance from junction to case R$_{θJC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=150℃. The SOA curve provides a single pulse ratin g.

G. Maximum current is limited by the package.

Rev4: May 2011

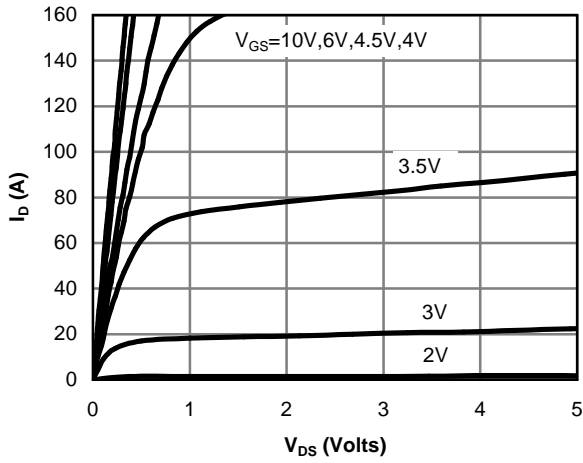## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

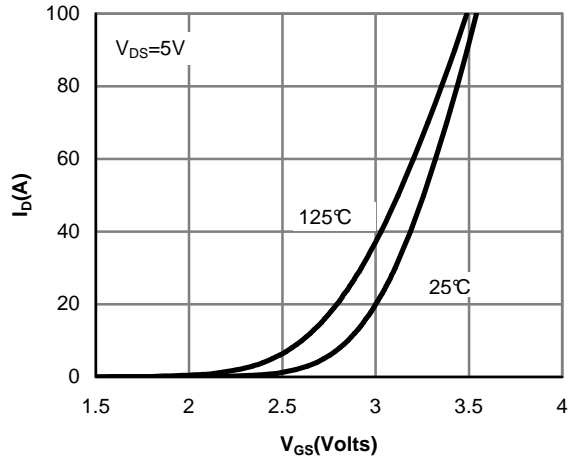Fig 1: On-Region Characteristics

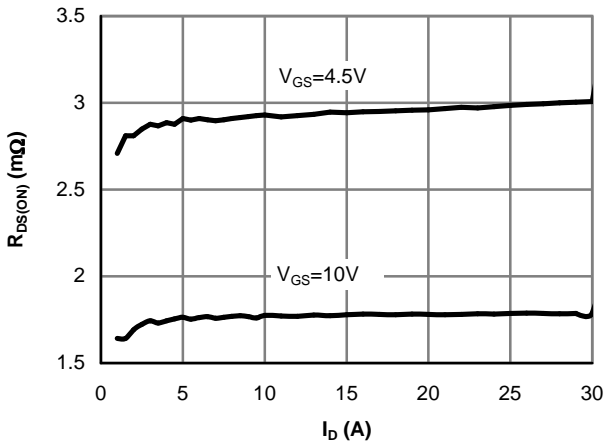Figure 2: Transfer Characteristics

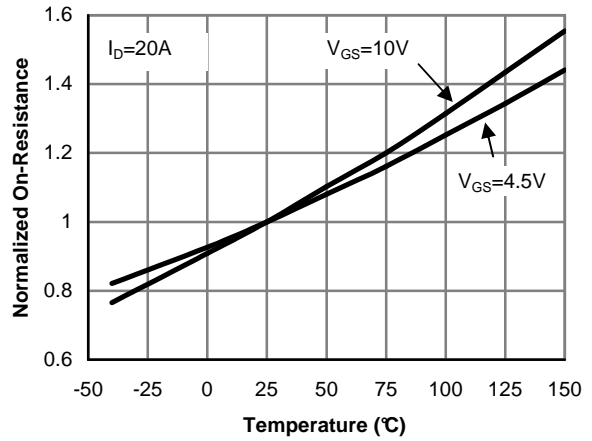Figure 3: On-Resistance vs. Drain Current and Gate Voltage
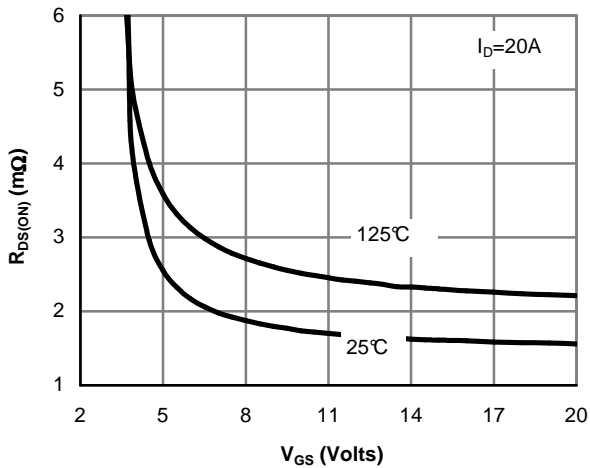

Figure 4: On-Resistance vs. Junction Temperature

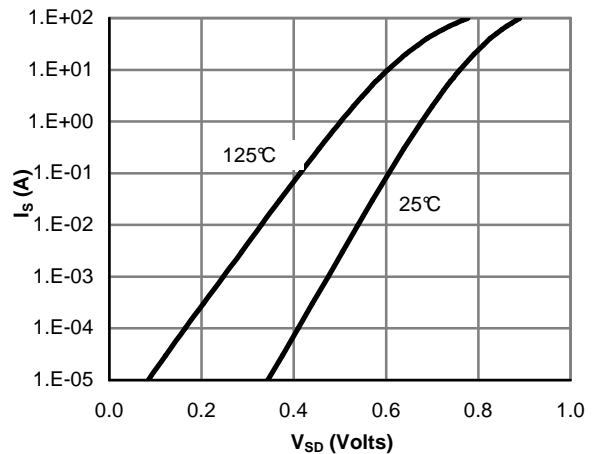Figure 5: On-Resistance vs. Gate-Source Voltage

Figure 6: Body-Diode Characteristics

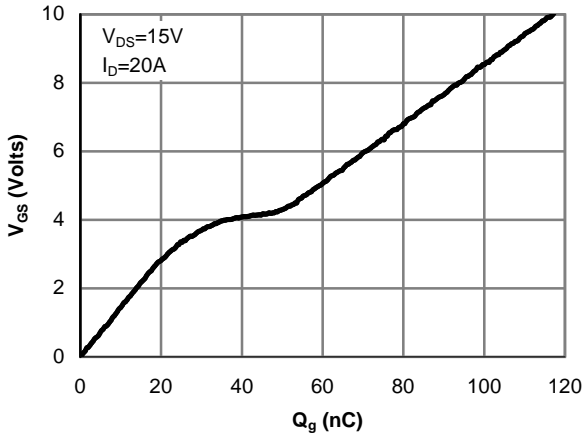## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
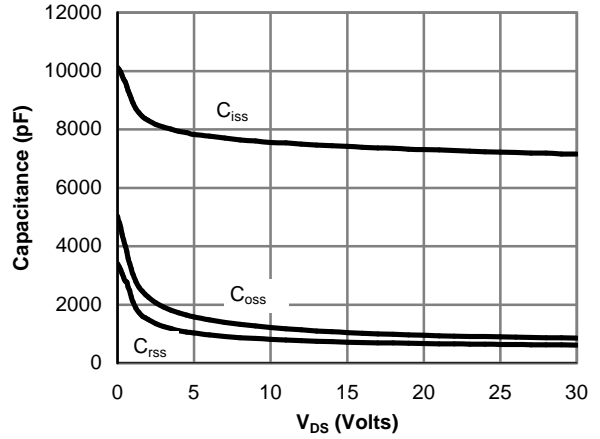
Figure 7: Gate-Charge Characteristics

V_{DS}=15V
I_D=20A

X-axis: Q_g (nC)
Y-axis: V_{GS} (Volts)

Figure 8: Capacitance Characteristics

C_{iss}
C_{oss}
C_{rss}

X-axis: V_{DS} (Volts)
Y-axis: Capacitance (pF)
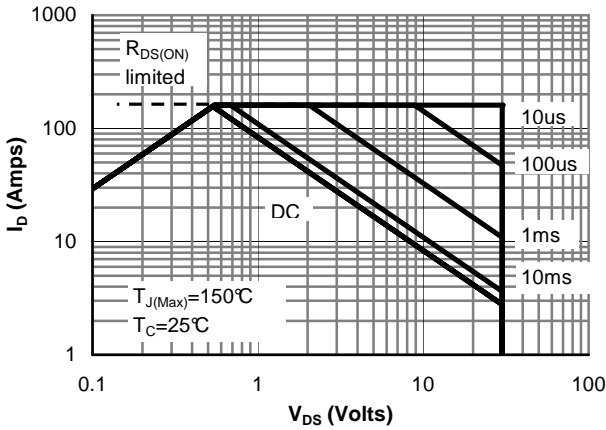
Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

$R_{DS(ON)}$ limited
10us
100us
DC
1ms
10ms
$T_{J(Max)}$=150℃
T_C=25℃

X-axis: V_{DS} (Volts)
Y-axis: I_D (Amps)
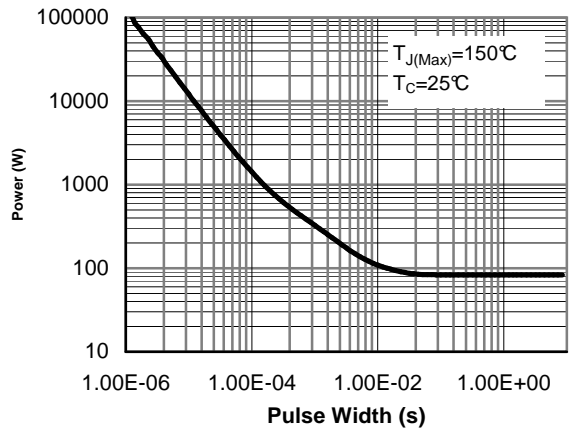
Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

$T_{J(Max)}$=150℃
T_C=25℃

X-axis: Pulse Width (s)
Y-axis: Power (W)

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

$D=T_{on}/T$
$T_{J,PK}=T_C+P_{DM}.Z_{\theta Jc}.R_{\theta Jc}$
$R_{\theta JC}$=1.5℃/W

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

P_D
T_{on}
T

Single Pulse

X-axis: Pulse Width (s)
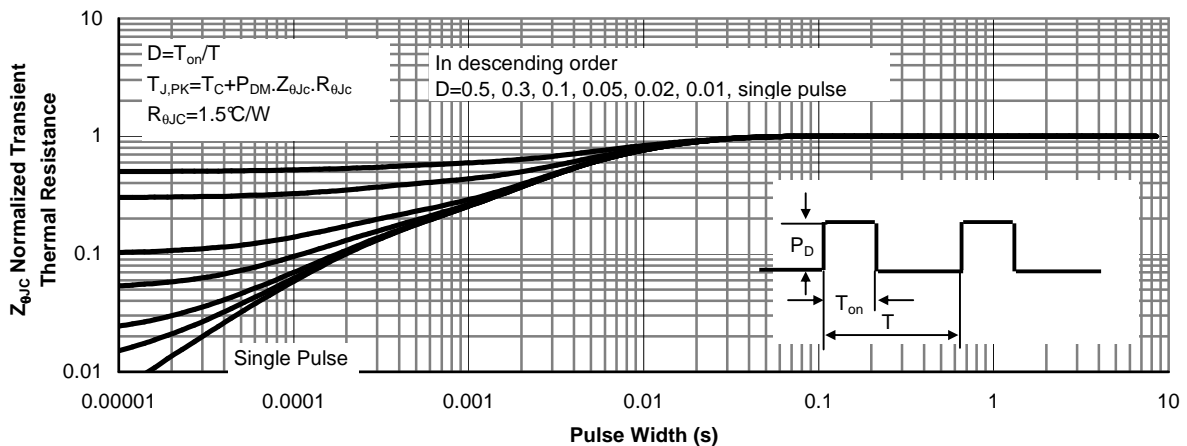Y-axis: $Z_{\theta Jc}$ Normalized Transient Thermal Resistance

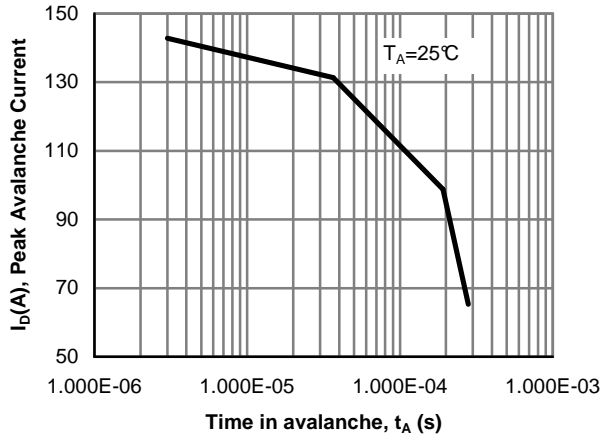## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
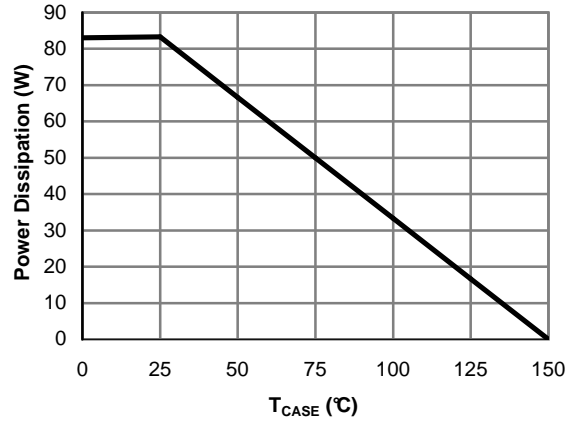
Figure 12: Single Pulse Avalanche capability
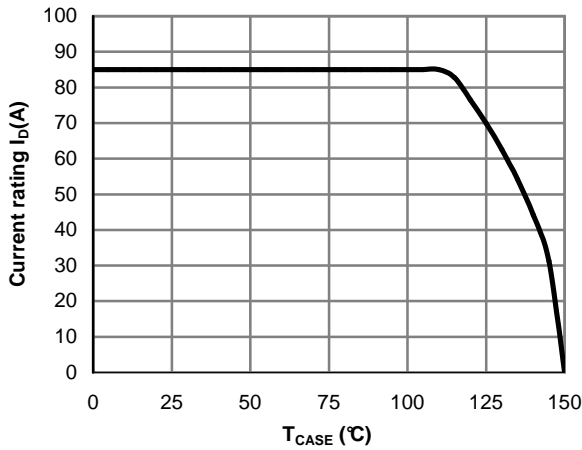
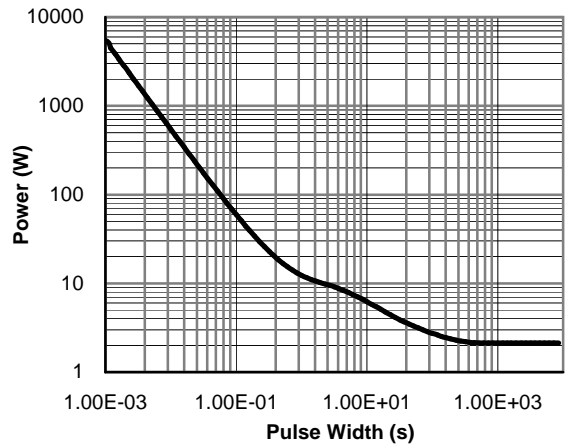Figure 13: Power De-rating (Note B)

Figure 14: Current De-rating (Note B,G)

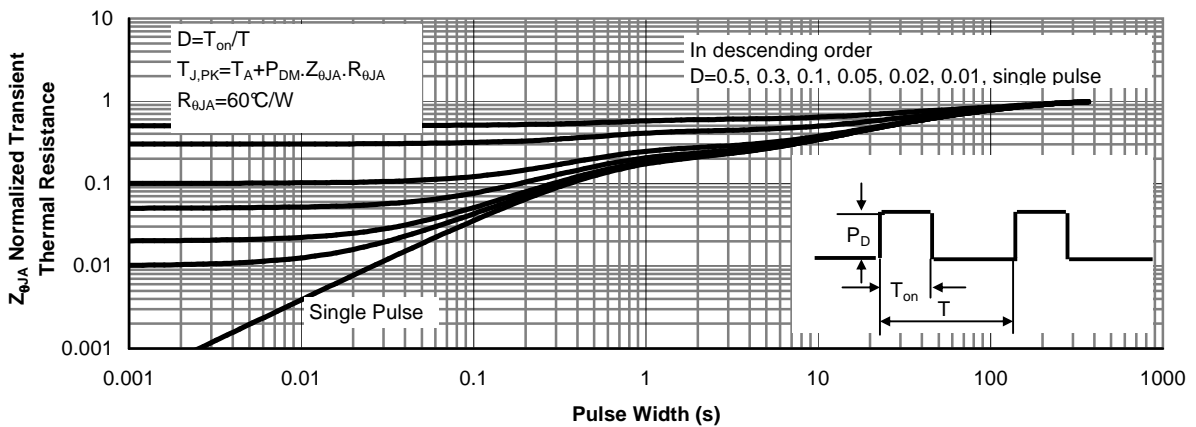Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note A)

$D=T_{on}/T$
$T_{J,PK}=T_A+P_{DM}\cdot Z_{\theta JA}\cdot R_{\theta JA}$
$R_{\theta JA}=60°C/W$

In descending order
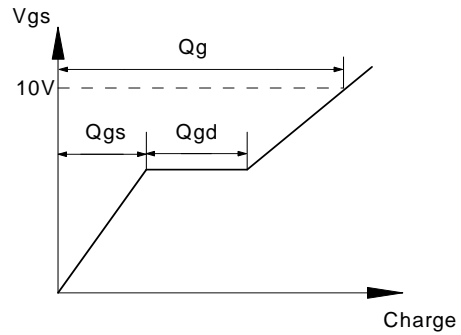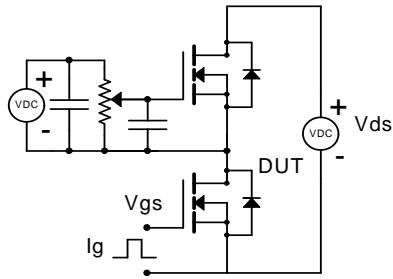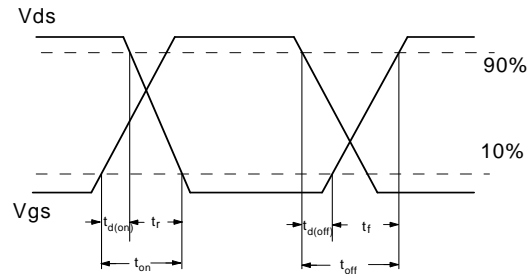D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse
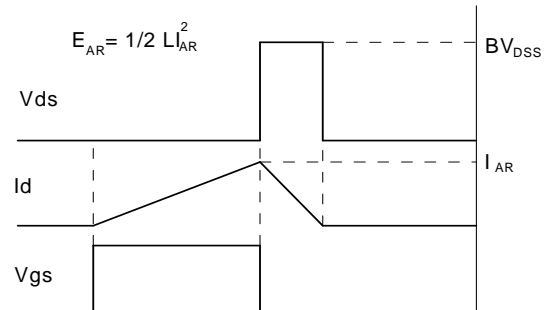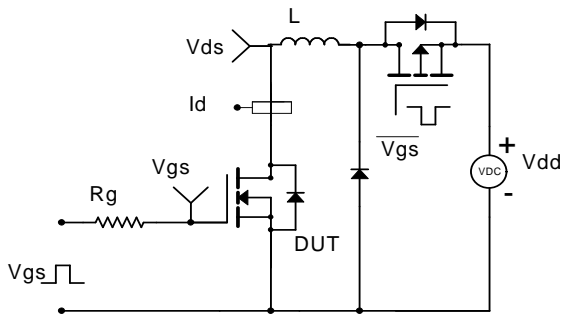
Figure 16: Normalized Maximum Transient Thermal Impedance (Note A)

Gate Charge Test Circuit & Waveform

Vgs

10V

Qg

Qgs   Qgd

Charge

Resistive Switching Test Circuit & Waveforms

RL

Vds

Rg   Vgs   DUT   Vdd

Vgs

Vds

90%

10%

Vgs

$t_{d(on)}$ t_r $t_{d(off)}$ t_f

t_{on} t_{off}
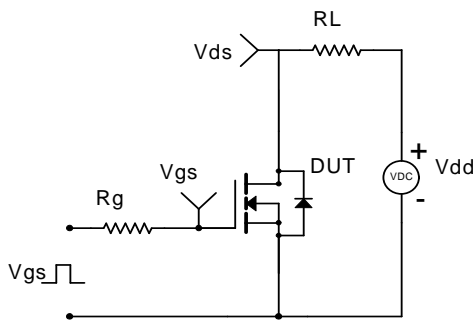
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

L

Vds

Id

Rg   Vgs $\overline{Vgs}$ Vdd

DUT

Vgs

$E_{AR} = 1/2 \, LI_{AR}^2$

BV_{DSS}

Vds

Id I_{AR}

Vgs

Diode Recovery Test Circuit & Waveforms

Vds +   DUT

Vds -

Isd   L

Vgs   Vdd

Ig

$Q_{rr} = -\int Idt$

Vgs

Isd I_F t_{rr}

dI/dt

I_{RM}

Vds   Vdd