STP5N105K5

N-channel 1050 V, 2.9 Ω typ., 3 A MDmesh™ K5 Power MOSFET in a TO-220 package

Datasheet - production data

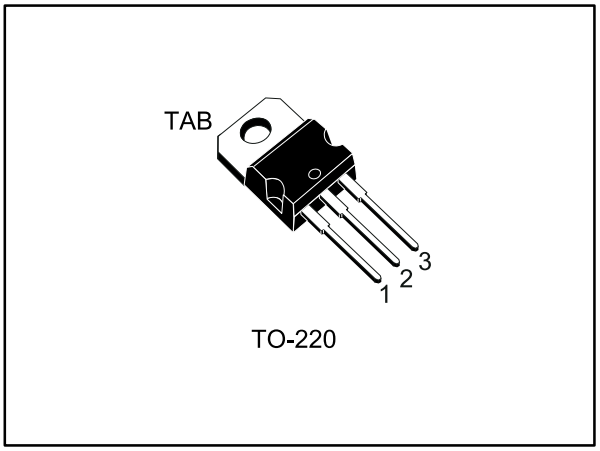
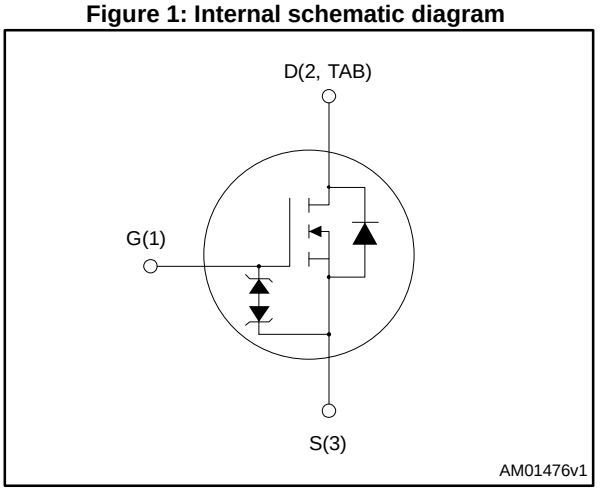


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STP5N105K5	1050 V	3.5 Ω	3 A	85 W

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This N-channel Zener-protected Power MOSFET is designed using ST's revolutionary avalanche-rugged very high voltage MDmesh™ K5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STP5N105K5	5N105K5	TO-220	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	3	A
I_D	Drain current (continuous) at T_C = 100 °C	2	A
I_{DM} (1)	Drain current (pulsed)	12	A
P_{TOT}	Total dissipation at T_C = 25 °C	85	W
I_{AR}	Max current during repetitive or single pulse avalanche	1	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	85	mJ
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_j	Operating junction temperature	- 55 to 150	°C
T_{stg}	Storage temperature		

Notes:

(1)Pulse width limited by safe operating area

(2)I_{SD} ≤ 3 A, di/dt ≤ 100 A/µs, $V_{DS(peak)}$ ≤ $V_{(BR)DSS}$

(3)V_{DS} ≤ 840 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.47	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb max	62.5	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 1 mA	1050			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 1050 V			1	µA
		V_{GS} = 0, V_{DS} = 1050 V, Tc=125 °C			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 1.5 A		2.9	3.5	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	210	-	pF
C_{oss}	Output capacitance		-	16	-	pF
C_{rss}	Reverse transfer capacitance		-	0.5	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 840 V	-	26	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	10	-	pF
R_G	Intrinsic gate resistance	f = 1MHz open drain	-	9	-	Ω
Q_g	Total gate charge	V_{DD} = 840 V, I_D = 3 A V_{GS} =10 V *Figure 16: "Gate charge test circuit"*	-	12.5	-	nC
Q_{gs}	Gate-source charge		-	2	-	nC
Q_{gd}	Gate-drain charge		-	9.5	-	nC

Notes:

(1)Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

(2)Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 525V, I_D = 1.5 A, R_G=4.7 Ω, V_{GS}=10 V *Figure 18: " Unclamped inductive load test circuit"*	-	15.5	-	ns
t_r	Rise time		-	8.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	31	-	ns
t_f	Fall time		-	24	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3	A
I_{SDM}	Source-drain current (pulsed)				12	A
V_{SD}(1)	Forward on voltage	I_{SD}= 3 A, V_{GS}=0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD}= 3 A, V_{DD}= 60 V di/dt = 100 A/µs, *Figure 17: " Test circuit for inductive load switching and diode recovery times"*	-	400		ns
Q_{rr}	Reverse recovery charge		-	2.3		µC
I_{RRM}	Reverse recovery current		-	12		A
t_{rr}	Reverse recovery time	I_{SD}= 3 A,V_{DD}= 60 V di/dt=100 A/µs, Tj=150 °C *Figure 17: " Test circuit for inductive load switching and diode recovery times"*	-	560		ns
Q_{rr}	Reverse recovery charge		-	3.1		µC
I_{RRM}	Reverse recovery current		-	11		A

Notes:

(1)Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

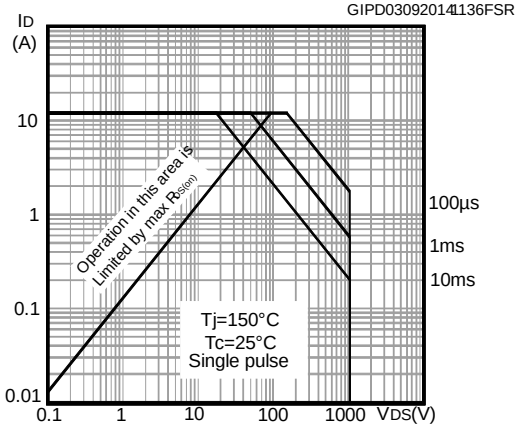


Figure 3: Thermal impedance

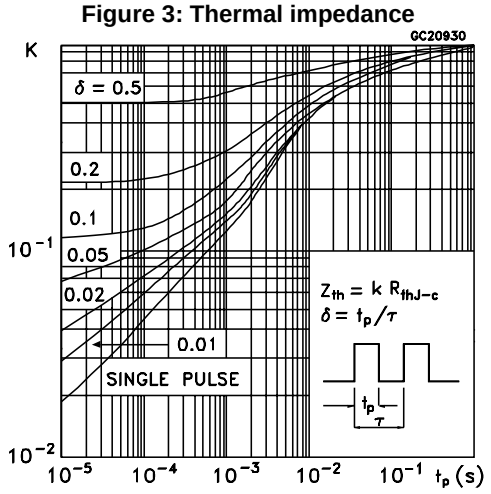


Figure 4: Output characteristics

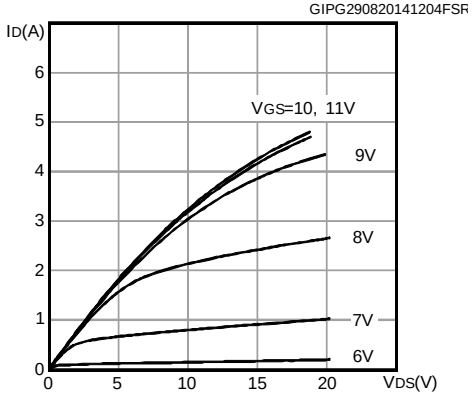


Figure 5: Transfer characteristics

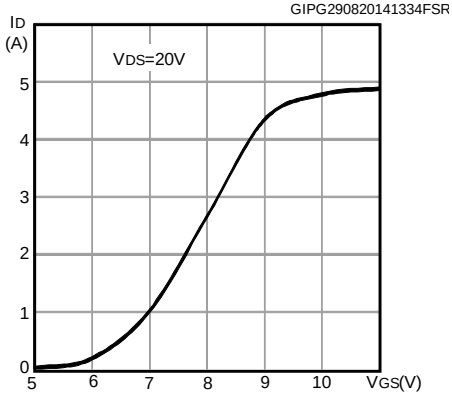


Figure 6: Gate charge vs gate-source voltage

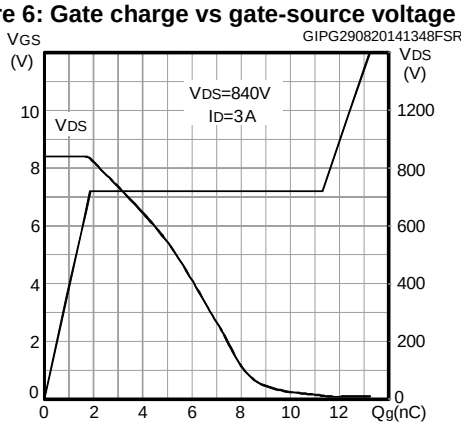


Figure 7: Static drain-source on-resistance

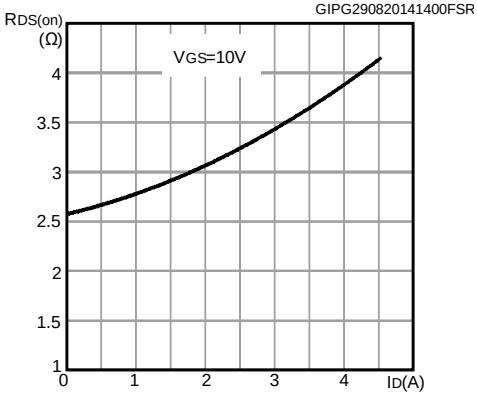


Figure 8: Capacitance variations

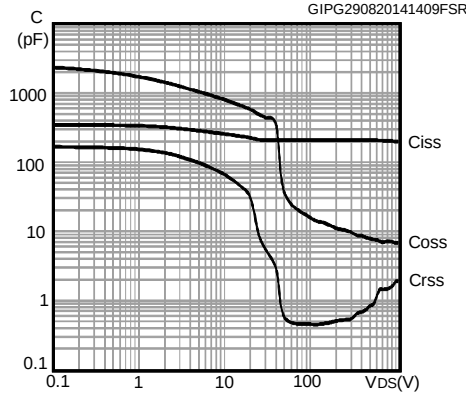


Figure 9: Source-drain diode forward characteristics

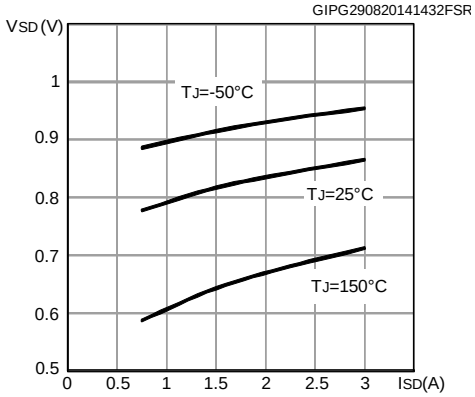


Figure 10: Normalized gate threshold voltage vs temperature

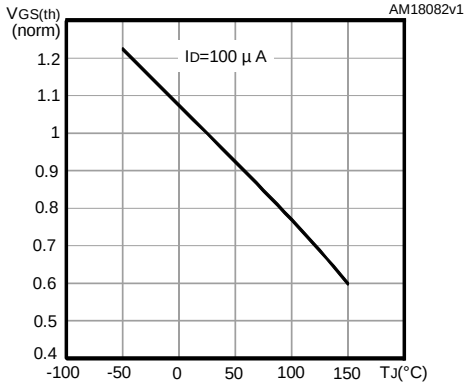


Figure 11: Normalized on-resistance vs temperature

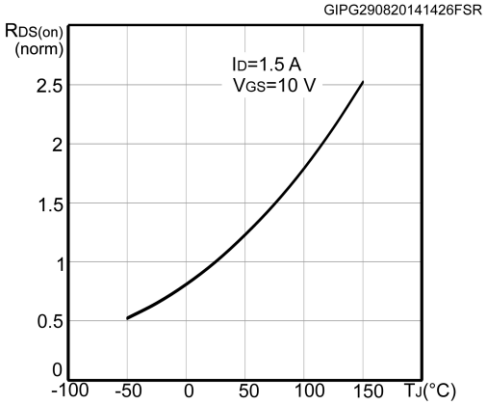


Figure 12: Normalized V(BR)DSS vs temperature

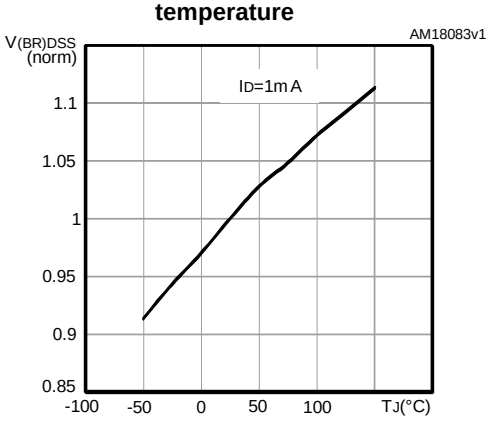


Figure 13: Maximum avalanche energy

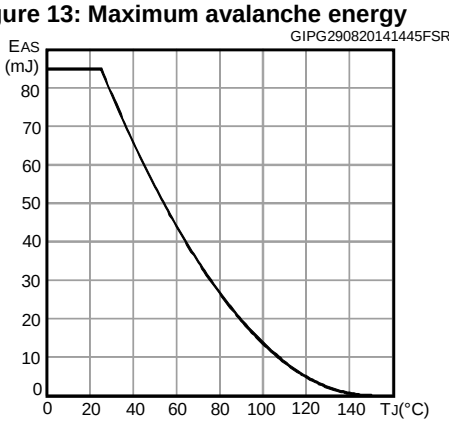
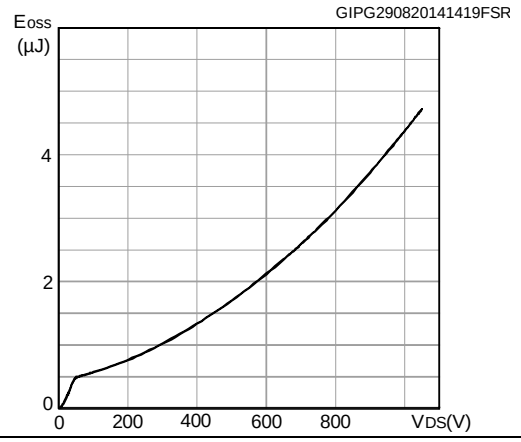


Figure 14: Output capacitance stored energy vs temperature



3 Test circuits

Figure 15: Switching times test circuit for resistive load

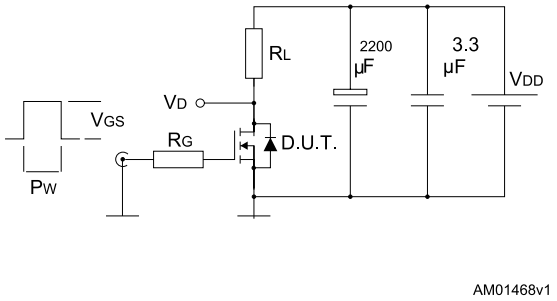


Figure 16: Gate charge test circuit

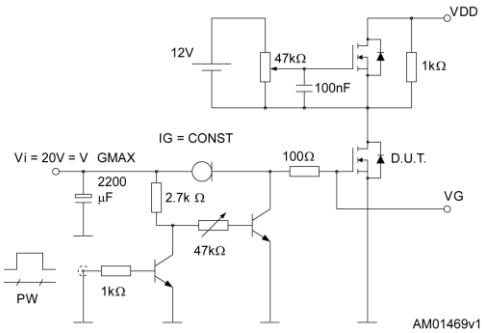


Figure 17: Test circuit for inductive load switching and diode recovery times

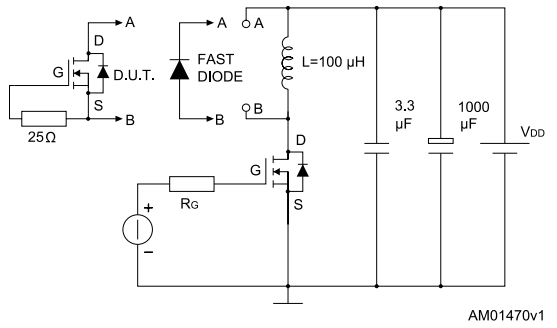


Figure 18: Unclamped inductive load test circuit

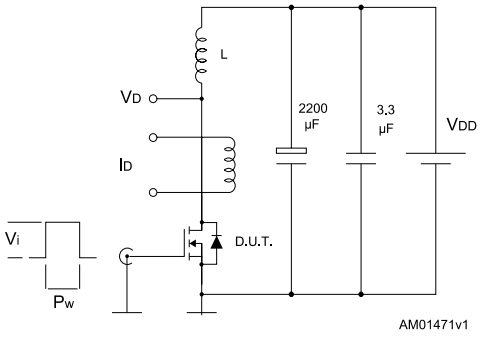


Figure 19: Unclamped inductive waveform

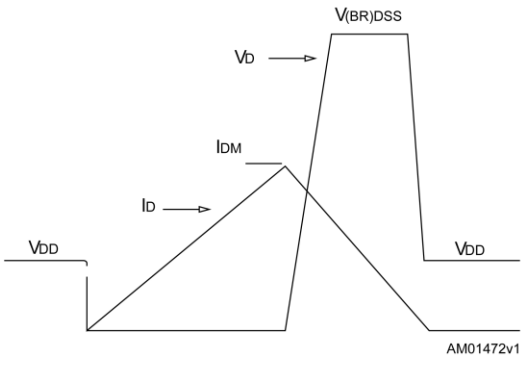
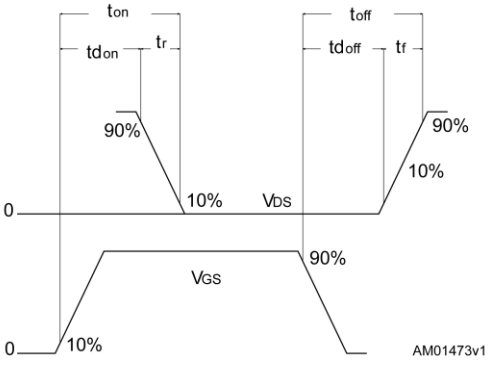


Figure 20: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220 package mechanical data

Figure 21: TO-220 type A package outline

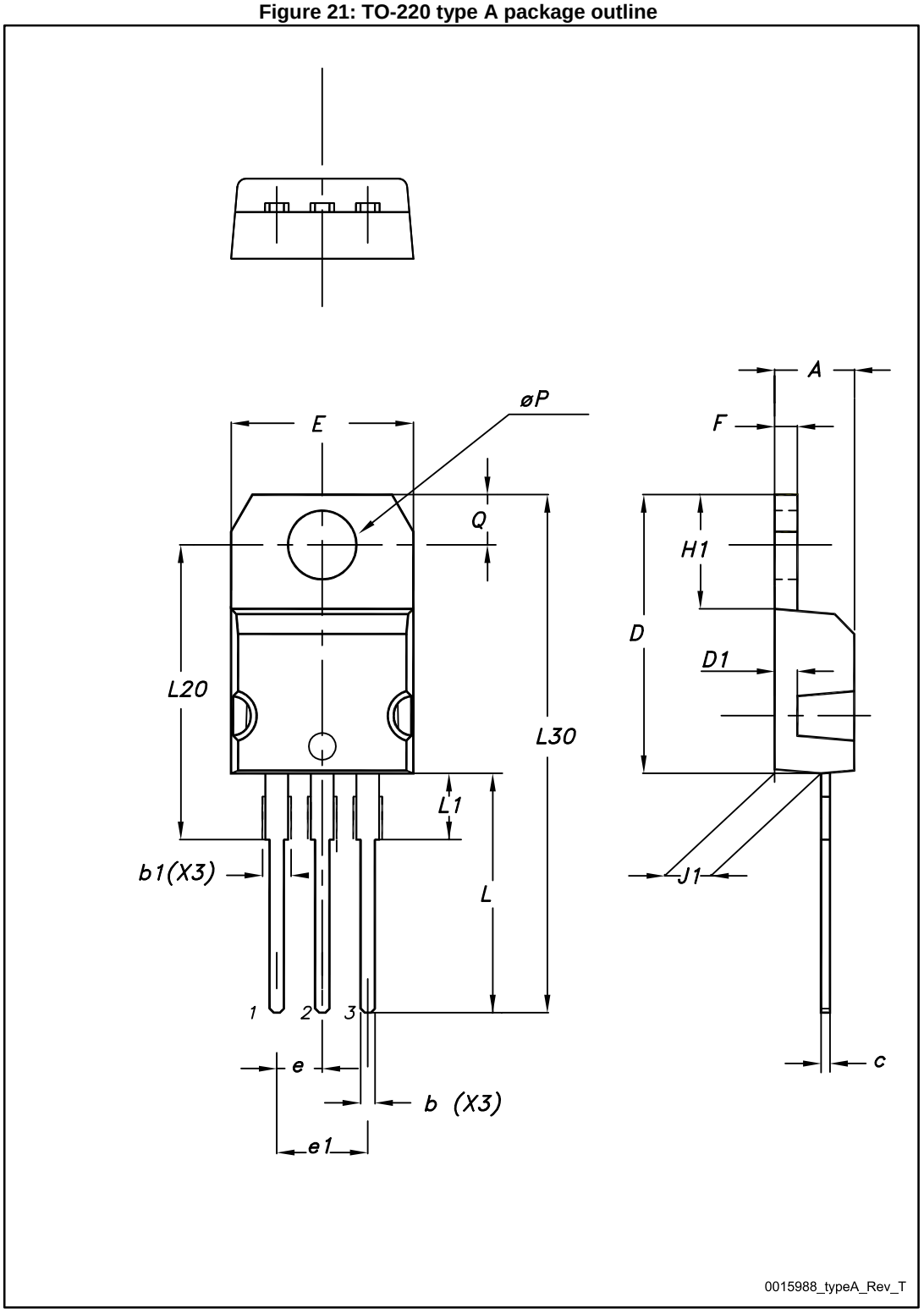


Table 9: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ÆP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
17-Jul-2014	1	First release.
03-Sep-2014	2	Document status promoted from preliminary to production data. Added *Section 3.1: "Electrical characteristics (curves)"* Minor text changes.
15-Oct-2014	3	Updated *Figure 6: "Gate charge vs gate-source voltage"*and *Figure 8: "Capacitance variations"*

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.