5A, 8MHz, 4-Phase Synchronous Step-Up DC/DC Converter

FEATURES

- **High Efficiency: Up to 95%**
- **Up to 3A Continuous Output Current**
- **4-Phase Operation for Low Output Ripple and Tiny Solution Size**
- **Output Disconnect and Inrush Current Limiting**
- **Very Low Quiescent Current: 12µA**
- 0.5V to 4.5V Input Range
- 2.4V to 5.25V Adjustable Output Voltage
- Adjustable Current Limit
- Adjustable, Fixed Frequency Operation from 100kHz to 2MHz per Phase
- Synchronizable Oscillator with Sync Output
- Internal Synchronous Rectifiers
- Manual or Automatic Burst Mode® Operation
- Power Good Comparator
- <1µA Shutdown Current
- Antiringing Control
- 5mm × 5mm Thermally Enhanced QFN Package

APPLICATIONS

- Handheld Computers
- Point-of-Load Regulators
- 3.3V to 5V Conversion

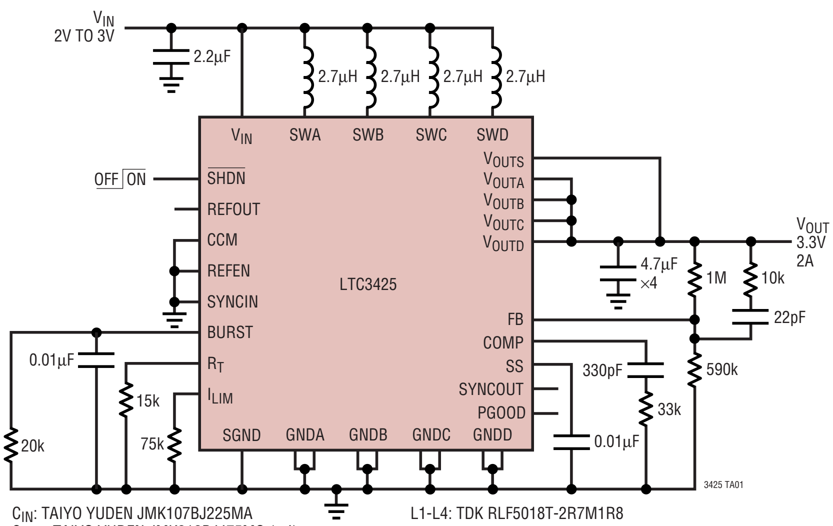
DESCRIPTION

The LTC®3425 is a synchronous, 4-phase boost converter with output disconnect capable of operation below 1V input. It includes four N-channel MOSFET switches and four P-channel synchronous rectifiers for an effective $R_{DS(ON)}$ of 0.045Ω and 0.05Ω, respectively. 4-phase operation greatly reduces peak inductor currents, and capacitor ripple current, and increases effective switching frequency, minimizing inductor and capacitor sizes. True output disconnect eliminates inrush current and allows zero load current in shutdown. External Schottky diodes are not required in most applications (V_{OUT} < 4.3V). Power saving Burst Mode operation can be user controlled or left in automatic mode.

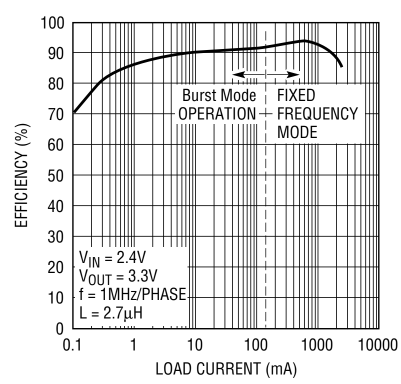
Other features include 1µA shutdown current, programmable frequency with sync in and out, programmable soft-start, antiringing control, thermal shutdown, adjustable current limit, reference output and power good comparator.

The LTC3425 is available in a small, thermally enhanced 32-pin QFN package.

TYPICAL APPLICATION



C_{IN}: TAIYO YUDEN JMK107BJ225MA
C_{OUT}: TAIYO YUDEN JMK212BJ475MG (×4)
L1-L4: TDK RLF5018T-2R7M1R8

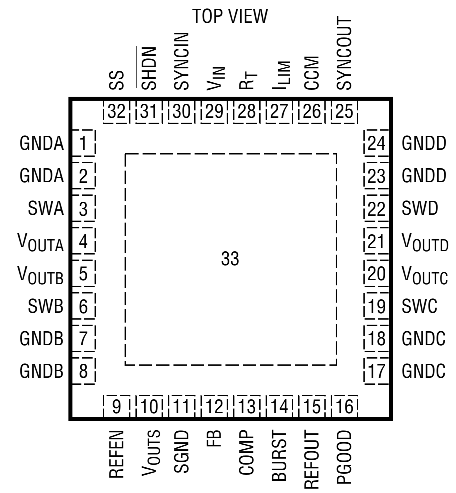


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage .... −0.3V to 6V
SWA-D Voltages ....−0.3V to 6V
V_{OUTA-D}, V_{OUTS} Voltages........................... −0.3V to 6V
BURST, $\overline{SHDN}$, SS, REFEN, SYNCOUT, PGOOD,
REFOUT, CCM, SYNCIN Voltages .... −0.3V to 6V
Operating Ambient Temperature Range
(Note 5) .... −40°C to 85°C
Storage Temperature Range .... −65°C to 125°C
Lead Temperature (Soldering, 10 sec).................. 300°C

PACKAGE/ORDER INFORMATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 40°C/W 1 LAYER BOARD,
θ_{JA} = 35°C/W 4 LAYER BOARD, θ_{JC} = 1.1°C/W
EXPOSED PAD IS GND (PIN 33) MUST BE SOLDERED TO PCB

ORDER PART NUMBER	UH PART MARKING
LTC3425EUH	3425

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 1.2V, V_{OUT} = 3.3V, R_T = 15k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Start-Up Voltage	V_{OUT} = 0V, I_{LOAD} < 1mA			0.88	1	V
Minimum Operating Voltage	(Note 3)	●			0.5	V
Output Voltage Adjust Range		●	2.4		5.25	V
Feedback Regulation Voltage		●	1.196	1.220	1.244	V
Feedback Input Current				1	50	nA
V_{OUT} Quiescent Current—Burst Mode Operation	BURST = 0V, REFEN = 0V, FB = 1.3V (Note 2) BURST = 0V, REFEN = 2V, FB = 1.3V (Note 2)			12 18	25 35	µA µA
V_{IN} Quiescent Current—Shutdown	$\overline{SHDN}$ = 0V, V_{OUT} = 0V, Not Including Switch Leakage			0.1	1	µA
V_{OUT} Quiescent Current—Active	V_C = 0V, Nonswitching (Note 2)			1.8	3	mA
NMOS Switch Leakage	V_{SW} = 5V			0.1	5	µA
PMOS Switch Leakage	V_{SW} = 5V, V_{OUT} = 0V			0.1	10	µA
NMOS Switch On Resistance	(Note 4)			0.04		Ω
PMOS Switch On Resistance	(Note 4)			0.05		Ω
NMOS Current Limit	I_{LIM} Resistor = 75k (Note 4) I_{LIM} Resistor = 200k (Note 4)	● ●	5.0 1.8	7.0 2.7		A A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 1.2V, V_{OUT} = 3.3V, R_T = 15k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PMOS Turn-Off Current	CCM < 0.4V			−80		mA
PMOS Reverse Current Limit	CCM > 1.4V			0.6		A
Max Duty Cycle		●	83	90	97	%
Min Duty Cycle		●			0	%
Frequency Accuracy	R_T = 15k	●	0.8	1	1.2	MHz
$\overline{SHDN}$ Input High	V_{OUT} = 0V (Initial Start-Up) V_{OUT} > 2.4V	● ●	1 0.65			V V
$\overline{SHDN}$ Input Low		●			0.25	V
$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$ = 5V or 0V $V_{\overline{SHDN}}$ = 2V			0.01 −0.50	1	µA µA
REFEN, CCM Input High		●	1.4			V
REFEN, CCM Input Low		●			0.4	V
REFEN, Input Current	V_{REFEN} = 5V			0.01	1	µA
SYNCIN Input High	(Note 7)	●	2.5			V
SYNCIN Input Low	(Note 7)	●			0.5	V
SYNCIN Input Current	V_{SYNCIN} = 5V			0.3	1	µA
CCM Input Current	V_{CCM} = 5V			2	4	µA
SYNC Input Pulse Width Range		●	0.1			µs
SYNC Out High			3			V
SYNC Out Low					0.4	V
REFOUT	REFEN > 1.4V, No Load	●	1.190	1.220	1.251	V
	I_{SOURCE} < 100µA, I_{SINK} < 10µA	●	1.184	1.220	1.252	V
Error Amp Transconductance				50		µS
Error Amp Output High	I_{LIM} Resistor = 75k			2.2		V
Error Amp Output Low				0.15		V
PGOOD Threshold (Falling Edge)	Referenced to Feedback Voltage	●	−9.5	−11.4	−13.5	%
PGOOD Hysteresis	Referenced to Feedback Voltage	●	1.5	2.5	4	%
PGOOD Low Voltage	I_{SINK} = 1mA (10mA Max)	●		0.12	0.25	V
PGOOD Leakage	V_{PGOOD} = 5.5V	●		0.01	1	µA
SS Current Source	V_{SS} = 1V			2.7		µA
Burst Threshold Voltage	Falling Edge	●	0.84	0.94	1.04	V
Burst Threshold Hysteresis				120		mV

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Current is measured into the V_{OUTS} pin since the supply current is bootstrapped to the output. The current will reflect to the input supply by V_{OUT}/(V_{IN} • Efficiency). The outputs are not switching.

Note 3: Once the output is started, the IC is not dependent on the V_{IN} supply.

Note 4: Total with all four FETs in parallel.

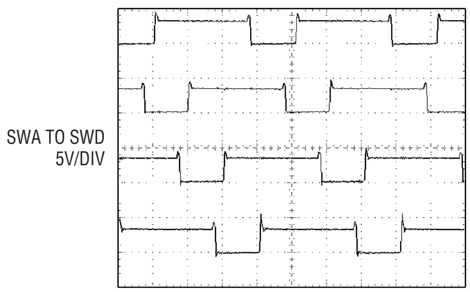
Note 5: The LTC3425E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 7: The typical logic threshold for this input is: V_{OUT}/2

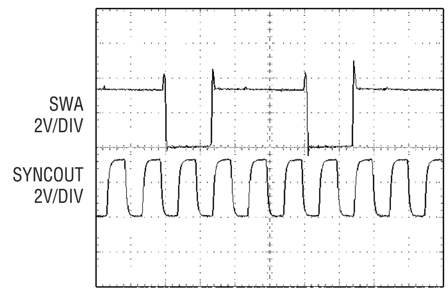
TYPICAL PERFORMANCE CHARACTERISTICS

SWA, SWB, SWC, SWD at 1MHz/Phase



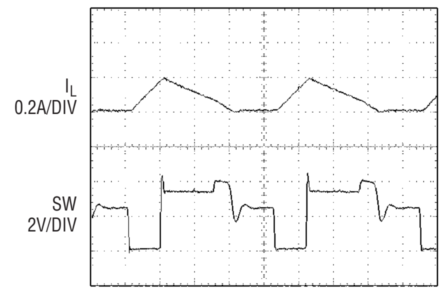
250ns/DIV 3425 G01

SW Pin and Oscillator SYNCOUT



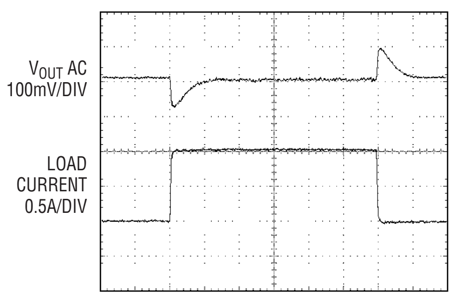
250ns/DIV 3425 G02

SW Pin and Inductor Current in Discontinous Mode. Antiring Circuit Eliminates High Frequency Ringing



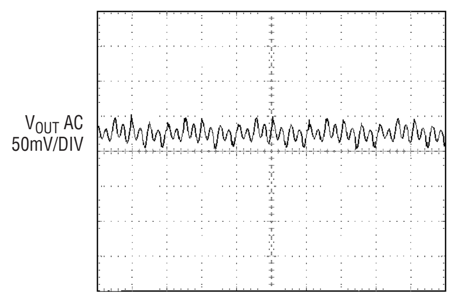
V_{IN} = 2.4V 250ns/DIV 3425 G03
V_{OUT} = 3.3V
C_{OUT} = 220µF

Transient Response 0.5A to 1.5A Fixed Frequency Mode Operation



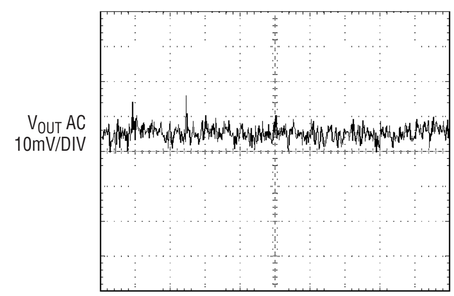
V_{IN} = 2.4V 100µs/DIV 3425 G04
V_{OUT} = 3.3V
C_{OUT} = 220µF

Output Voltage Ripple at 2.5A Load with Only Four 4.7µF Ceramic Capacitors



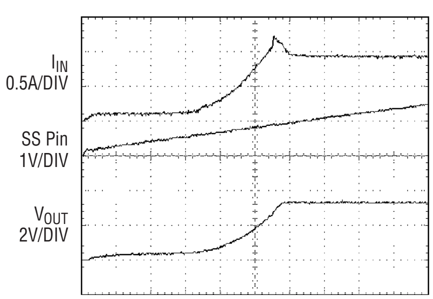
V_{IN} = 2.4V 500ns/DIV 3425 G05
V_{OUT} = 3.3V
FREQUENCY = 1MHz/PHASE

Output Voltage Ripple at 2.5A Load with a 47µF Ceramic Bulk Capacitor



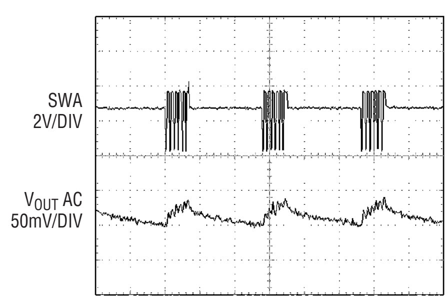
V_{IN} = 2.4V 500ns/DIV 3425 G06
V_{OUT} = 3.3V
FREQUENCY = 1MHz/PHASE

Soft-Start and Inrush Current Limiting



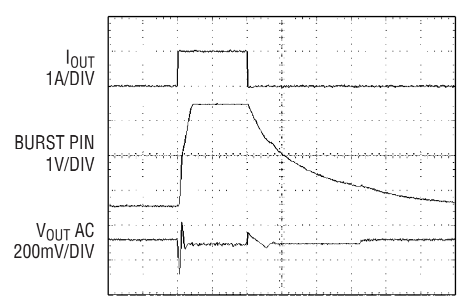
V_{IN} = 2.4V 500µs/DIV 3425 G07
V_{OUT} = 3.3V
$C_{SOFTSTART}$ = 0.015µF

Burst Mode Operation



V_{IN} = 2.4V 25µs/DIV 3425 G08
V_{OUT} = 3.3V
C_{OUT} = 220µF

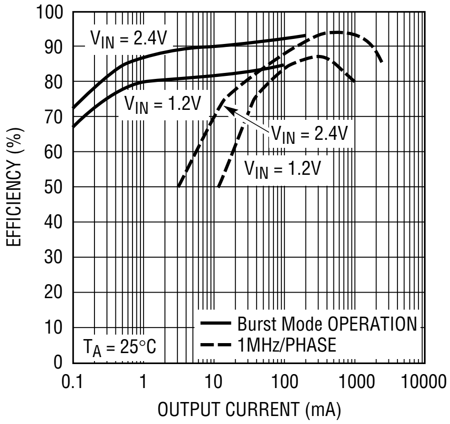
Transient Response 10mA to 1A Automatic Burst Mode Operation



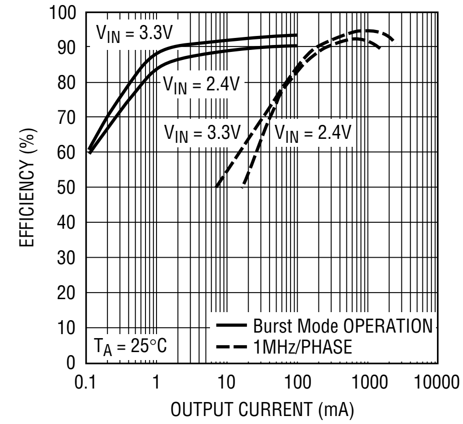
V_{IN} = 2.4V 1ms/DIV 3425 G10
V_{OUT} = 3.3V
C_{OUT} = 220µF

TYPICAL PERFORMANCE CHARACTERISTICS

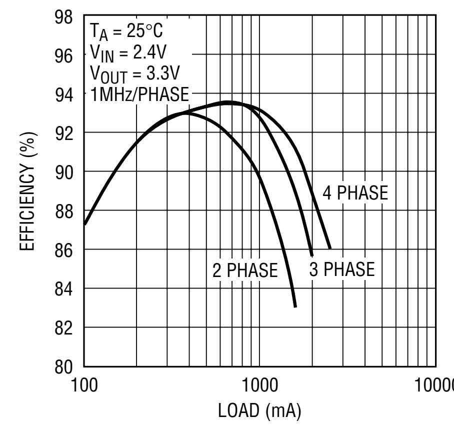
Converter Efficiency for V_{OUT} = 3.3V



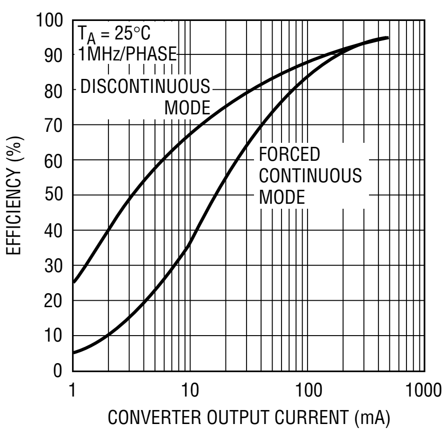
Converter Efficiency for V_{OUT} = 5V



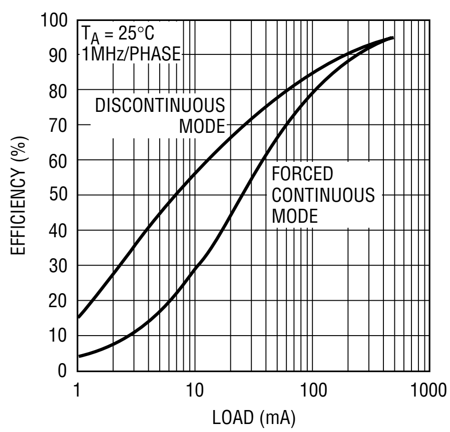
Converter Efficiency for 2-, 3- and 4-Phase Operation



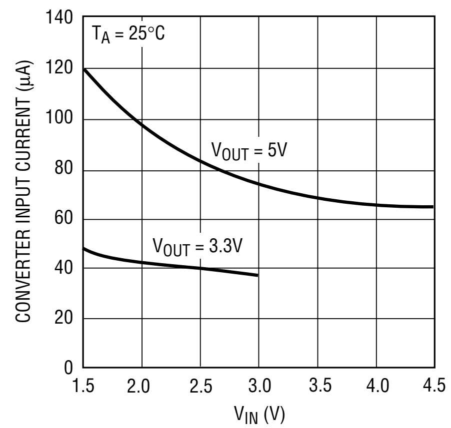
Efficiency Comparison of Discontinuous Mode and Forced Continuous Mode at Light Loads for V_{IN} = 2.4V, V_{OUT} = 3.3V



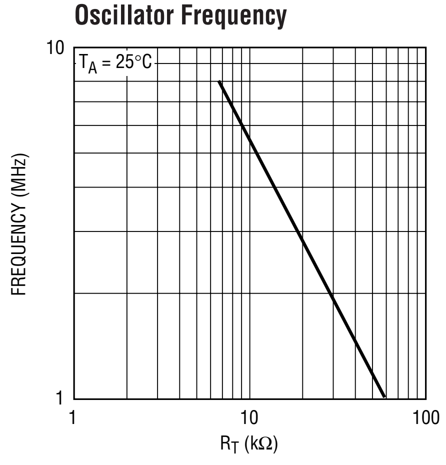
Efficiency Comparison of Discontinuous Mode and Forced Continuous Mode at Light Loads for V_{IN} = 3.3V, V_{OUT} = 5V



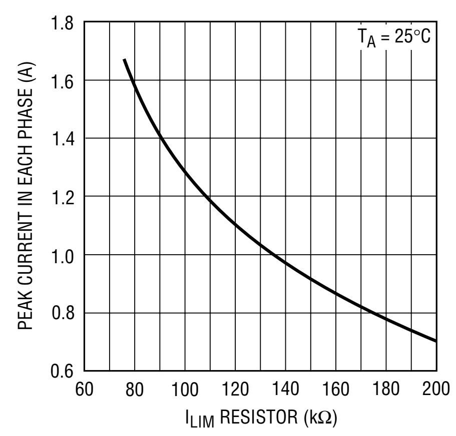
Converter No Load Input Current vs V_{IN} (Burst Mode Operation)



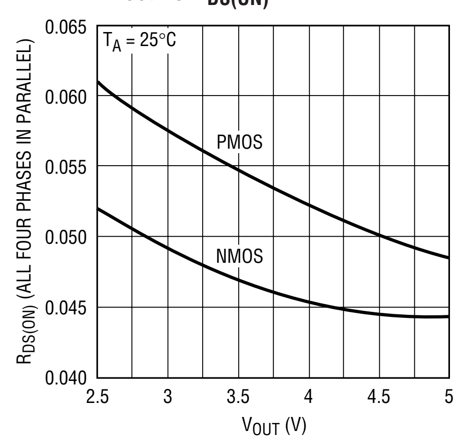
Oscillator Frequency



Peak Current Limit

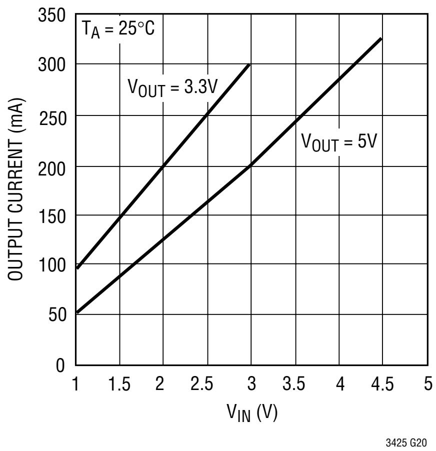


Effective $R_{DS(ON)}$

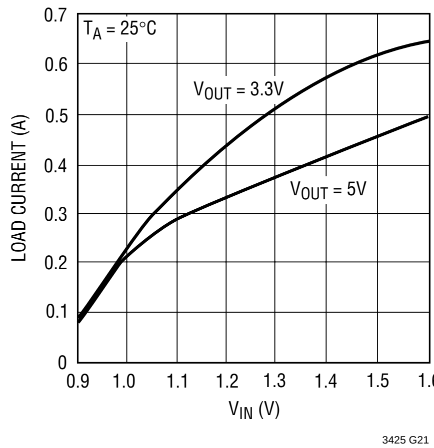


TYPICAL PERFORMANCE CHARACTERISTICS

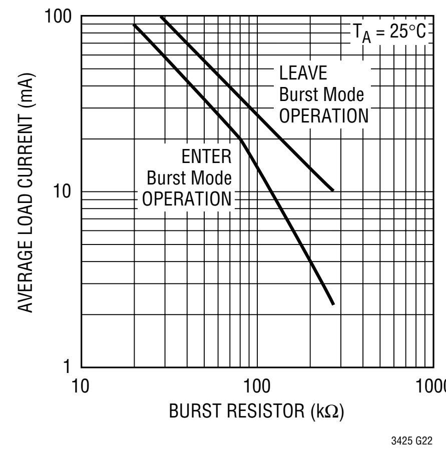
Maximum Output Current in Burst Mode Operation



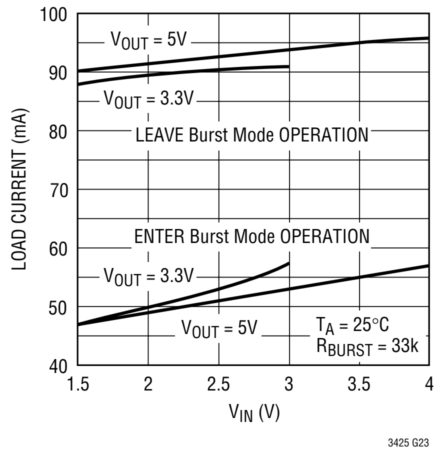
Maximum Start-Up Load vs V_{IN} (Constant Current Load)



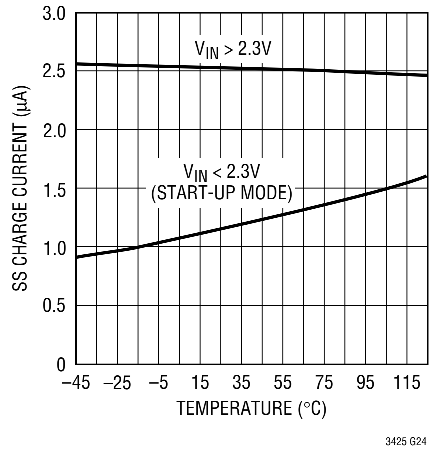
Automatic Burst Mode Current Thresholds vs R_{BURST}



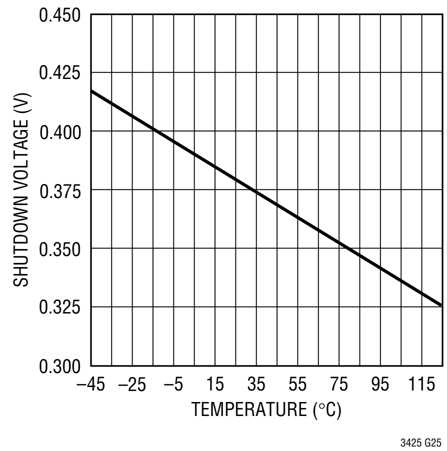
Automatic Burst Mode Thresholds vs V_{IN}



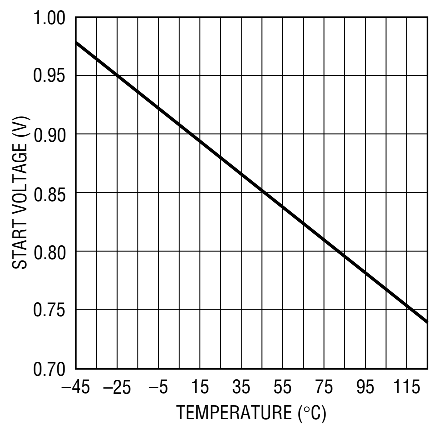
Soft-Start Charging Current vs Temperature



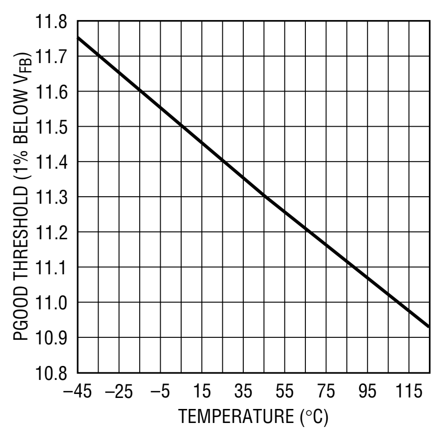
Shutdown Voltage vs Temperature



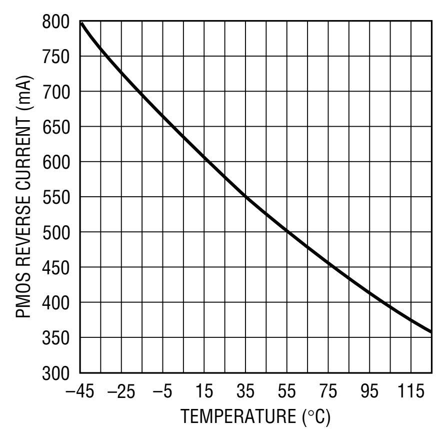
Minimum Start-Up Voltage vs Temperature



PGOOD Threshold vs Temperature

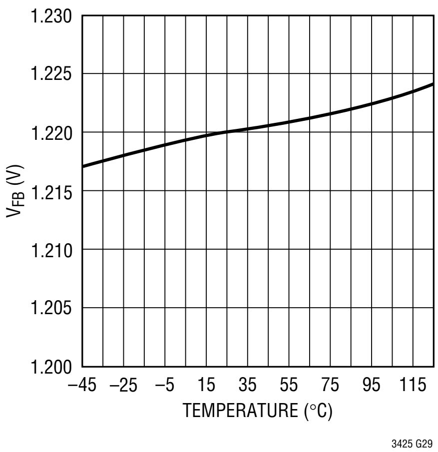


PMOS Reverse Current in Forced CCM vs Temperature

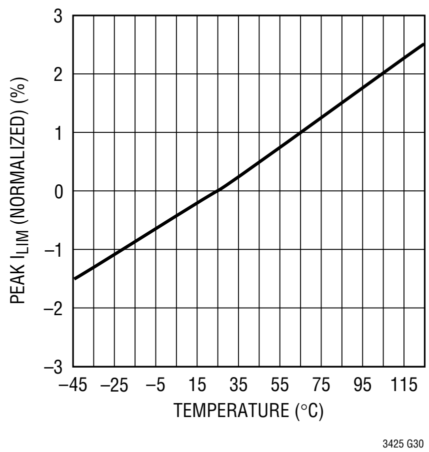


TYPICAL PERFORMANCE CHARACTERISTICS

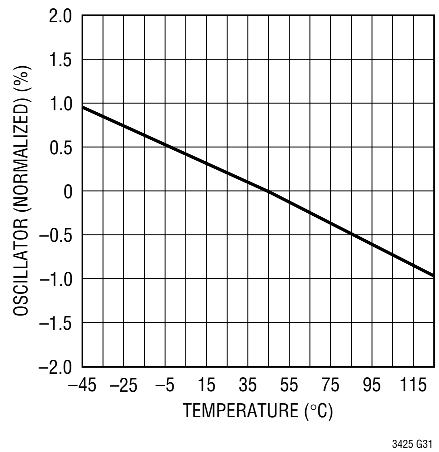
Feedback Voltage vs Temperature



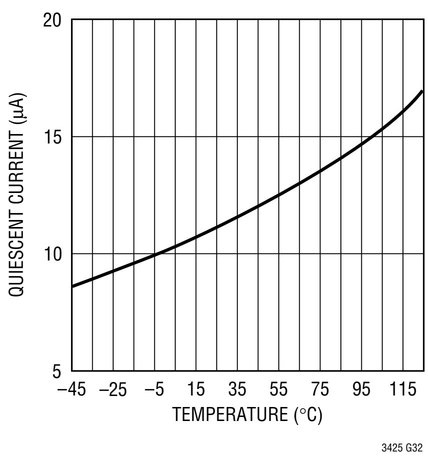
Peak Current Limit vs Temperature



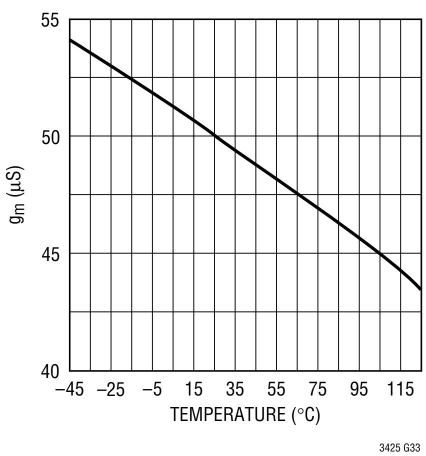
Oscillator Frequency vs Temperature



Burst Mode V_{OUT} Quiescent Current vs Temperature



Error Amplifier g_m vs Temperature



PIN FUNCTIONS

GNDA–D (Pins 1, 2, 7, 8, 17, 18, 23, 24): Power Ground for the IC and the Four Internal N-channel MOSFETs. Connect directly to the power ground plane.

SWA–D (Pins 3, 6, 19, 22): Switch Pins. Connect inductors here. Minimize trace length to keep EMI to a minimum. For discontinuous inductor current, a controlled impedance is internally connected from SW to V_{IN} to minimize EMI. For applications where $V_{OUT} > 4.3V$, it is required to have Schottky diodes from SW to V_{OUT} or a snubber circuit to stay within absolute maximum rating on the SW pins.

$V_{OUTA–D}$ (Pins 4, 5, 20, 21): Output of the Four Synchronous Rectifiers. Connect output filter capacitors to these pins. Connect one low ESR ceramic capacitor directly from each pin to the ground plane.

REFEN (Pin 9): Pull this pin above 1.4V to enable the REF output. Grounding this pin turns the REF output off to reduce quiescent current.

V_{OUTS} (Pin 10): V_{OUT} Sense Pin. Connect V_{OUTS} directly to an output filter capacitor. The top of the feedback divider network should also be tied to this point.

SGND (Pin 11): Signal Ground Pin. Connect to ground plane, near the feedback divider resistor.

FB (Pin 12): Feedback Pin. Connect FB to a resistor divider, keeping the trace as short as possible. The output voltage can be adjusted according to the following formula:

$$V_{OUT} = 1.22 \bullet \frac{R1+R2}{R1}$$

where R1 is connected from FB to SGND and R2 is connected from FB to V_{OUTS}.

COMP (Pin 13): Error Amp Output. A frequency compensation network is connected from this pin to ground to compensate the loop. See the section Closing the Feedback Loop for guidelines.

BURST (Pin 14): Burst Mode Threshold Adjust Pin. A resistor/capacitor combination from this pin to ground programs the average load current at which automatic Burst Mode operation is entered.

For manual control of Burst Mode operation, ground BURST to force Burst Mode operation or connect it to V_{OUT} to force fixed frequency PWM mode. Note that BURST must not be pulled higher than V_{OUT}.

REFOUT (Pin 15): Buffered 1.22V Reference Output. This pin can source up to 100µA and sink up to 10µA (only active when REFEN is pulled high). This pin must be decoupled with a 0.1µF capacitor for stability.

PGOOD (Pin 16): Open-Drain Output of the Power Good Comparator. This pin will go low when the output voltage drops 11% below its regulated value. Maximum sink current should be limited to 10mA.

SYNCOUT (Pin 25): Sync Output Pin. A clock is provided at the oscillator frequency, but phase-shifted 180 degrees to allow for synchronizing two devices for an 8-phase converter.

CCM (Pin 26): This pin is used to select forced continuous conduction mode. Normally this pin is grounded to allow CCM or DCM operation. To force continuous conduction mode, tie this pin to V_{OUT}. In this mode, a reverse current of up to about 0.6A will be allowed before turning off the synchronous rectifier. This will prevent pulse skipping at light load when Burst Mode operation is disabled, and will also improve the large-signal transient response when going from a heavy load to a light load. For Burst Mode operation, CCM should be low.

PIN FUNCTIONS

I_{LIM} (Pin 27): Current Limit Adjust Pin. Connect a resistor from I_{LIM} to SGND to set the peak current limit threshold for the N-channel MOSFETs, according to the formula (note that this is the peak current in each inductor):

$$I_{LIM} = \frac{130}{R}$$

where I is in Amps and R is in kΩ. Do not use values less than 75k.

R_T (Pin 28): Connect a resistor from R_T to SGND (or SGND plane) to program the oscillator frequency, according to the formula:

$$f_{OSC} = \frac{60}{R_T}$$

$$f_{SWITCH} = \frac{f_{OSC}}{4} = \frac{15}{R_T}$$

where f_{OSC} is in MHz and R_T is in kΩ.

V_{IN} (Pin 29): Input Supply Pin. Connect this to the input supply and decouple with 1μF minimum low ESR ceramic capacitor.

SYNCIN (Pin 30): Oscillator Synchronization Pin. A clock pulse width of 100ns minimum is required to synchronize the internal oscillator. If not used, SYNCIN should be grounded. The typical logic threshold for this input is:

$$\frac{V_{OUT}}{2}$$

The SYNCIN is ignored in Burst Mode operation.

$\overline{\text{SHDN}}$ (Pin 31): Shutdown Pin. Grounding $\overline{\text{SHDN}}$ (or pulling it below 0.25V) shuts down the IC. Pull pin up to ≥1V to enable. Once enabled, the pin only needs to be ≥0.65V.

SS (Pin 32): Soft-Start pin. Connect a capacitor from this pin to ground to set the soft-start time, according to the formula:

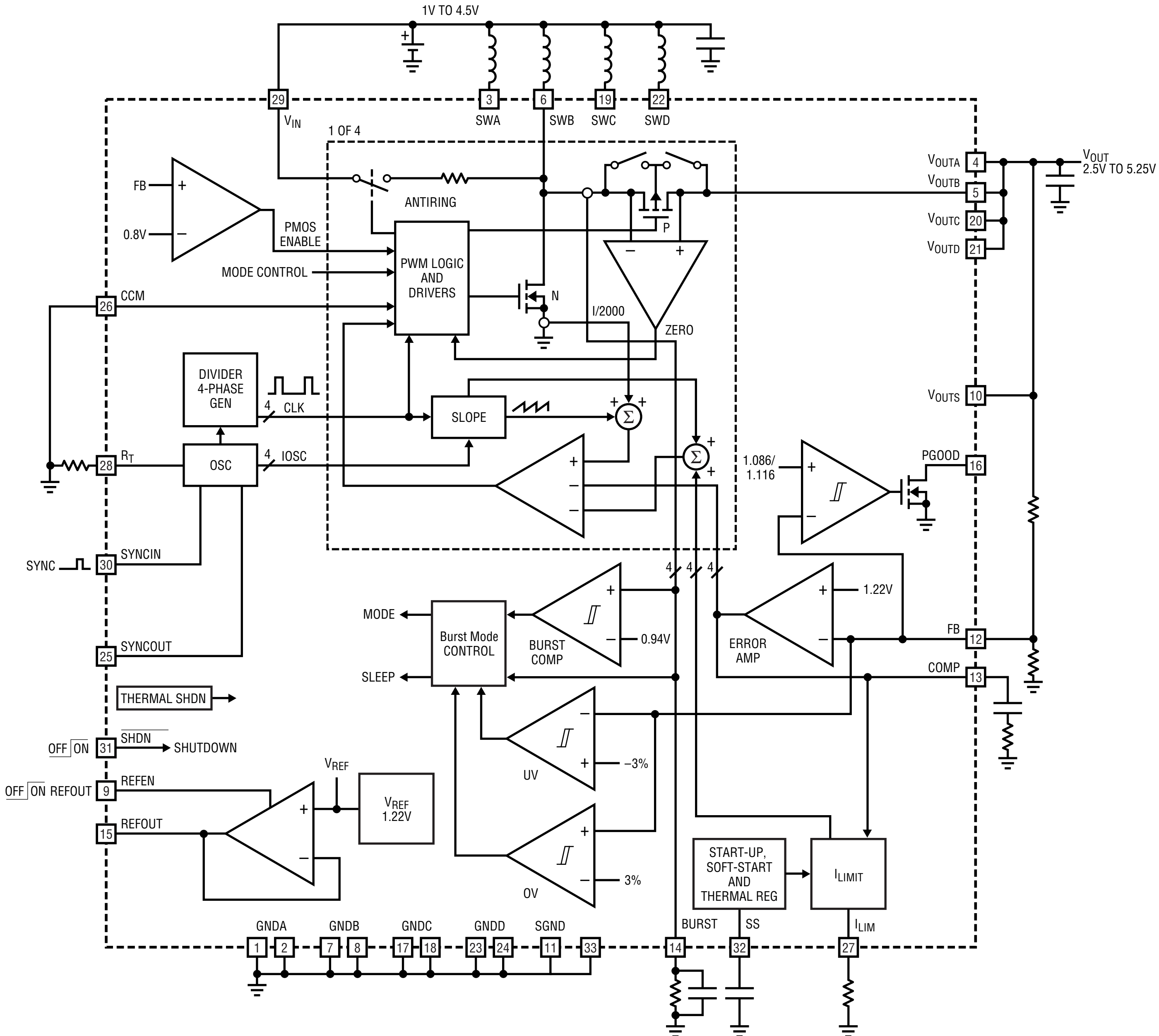
$$t(ms) = C_{SS}\ (\mu F) \bullet 320$$

The nominal soft-start charging current is 2.5μA. The active range of SS is from 0.8V to 1.6V. Note that this is the rise time of SS. The actual rise time of V_{OUT} will be a function of load and output capacitance.

Exposed Pad (Pin 33): Additional Power Ground for the IC. Connect directly to the power ground plane.

OPERATING MODE	BURST PIN	CCM PIN
Automatic Burst (Operating Mode is Load Dependent)	RC Network to Ground	Low
Forced Burst	Low	Low
Forced Fixed Frequency with Pulse Skipping at Light Load	High	Low
Forced Fixed Frequency, Low Noise (No Pulse Skipping)	High	High

BLOCK DIAGRAM



OPERATION

DETAILED DESCRIPTION

The LTC3425 provides high efficiency, low noise power for high current boost applications such as cellular phones and PDAs. The true output disconnect feature eliminates inrush current and allows V_{OUT} to go to zero during shutdown. The current mode architecture with adaptive slope compensation provides ease of loop compensation with excellent transient load response. The low $R_{DS(ON)}$, low gate charge synchronous switches eliminate the need for an external Schottky rectifier, and provide efficient high frequency pulse width modulation (PWM) control. High efficiency is achieved at light loads when Burst Mode operation is entered, where the IC's quiescent current is a low 12µA typical on V_{OUT}.

MULTIPHASE OPERATION

The LTC3425 uses a 4-phase architecture, rather than the conventional single phase of other boost converters. By having multiple phases equally spaced (90° apart), not only is the output ripple frequency increased by a factor of four, but the output capacitor ripple current is greatly reduced. Although this architecture requires four inductors, rather than a single inductor, there are a number of important advantages.

- Much lower peak inductor current allows the use of smaller, lower cost inductors.
- Greatly reduced output ripple current minimizes output capacitance requirement.
- Higher frequency output ripple is easier to filter for low noise applications.
- Input ripple current is also reduced for lower noise on V_{IN}.

The peak boost inductor current is given by:

$$I_{LPEAK} = \frac{I_O}{(1-D)\bullet N} + \frac{di}{2}$$

Where I_O is the average load current, D is the PWM duty cycle, N is the number of phases and di is the inductor ripple current. This relationship is shown graphically in Figure 1 using a single phase and a 4-phase example.

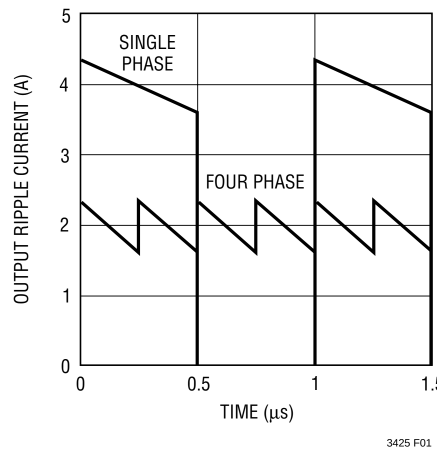


Figure 1. Comparison of Output Ripple Current with Single Phase and 4-Phase Boost Converter in a 2A Load Application Operating at 50% Duty Cycle

Example:

The following example, operating at 50% duty cycle, illustrates the advantages of multiphase operation over a conventional single-phase design.

V_{IN} = 1.9V, V_{OUT} = 3.6V, Efficiency = 90% (approx), I_{OUT} = 2A, Frequency = 1MHz, L = 2.2µH

Table 1

PARAMETER	SINGLE PHASE	FOUR PHASE	CHANGE FROM 1 TO 4 PHASE
Peak-Peak Output Ripple Current	4.227A	0.450A	Reduced by 89%
RMS Output Ripple Current	2.00A	0.184A	Reduced by 91%
Peak Inductor Current	4.227A	1.227A	Reduced by 71%
Output Ripple Frequency	1MHz	4MHz	Increased by 4×

With 4-phase operation, at least one of the phases will be delivering current to the load whenever V_{IN} is greater than one quarter V_{OUT} (duty cycles less than 75%). For lower duty cycles, there can be as many as two or three phases delivering load current simultaneously. This greatly reduces both the output ripple current and the peak current in each inductor, compared with a single-phase converter. This is illustrated in the waveforms of Figures 2 and 3.

Operation Using Only Two or Three Phases

The LTC3425 can operate as a 2- or 3-phase converter by simply eliminating the inductor from the unused phase(s).

OPERATION

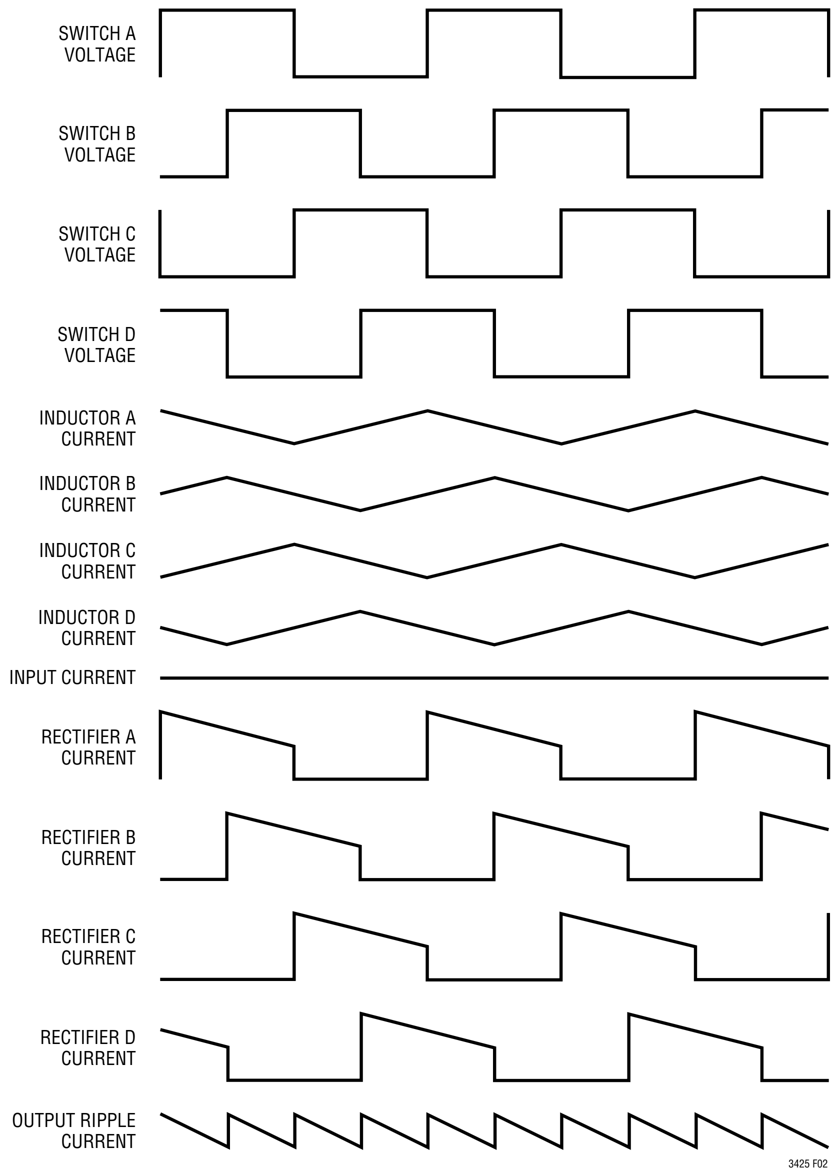


Figure 2. Simplified Voltage and Current Waveforms for 4-Phase Operation at 50% Duty Cycle

This approach can be used to reduce solution cost and board area in applications not requiring the full power capability of the LTC3425, or where peak efficiency may not be as important as cost and size. In this case, phase A should always be used, since this is the only phase active in Burst Mode operation and phase C is recommended as the second phase for the lowest output ripple, since it is 180° out of phase with phase A. Figure 4 illustrates the efficiency differences with two, three and four phases in a typical 2-cell to 3.3V boost application. In this example, you can see that for maximum loads less than 1A, the efficiency penalty for using only two or three phases is fairly small. Keep in mind, however, that this penalty will grow larger as the input voltage drops. Output ripple will also increase with each phase that is eliminated.

Low Voltage Start-Up

The LTC3425 includes an independent start-up oscillator designed to start up at input voltages as low as 0.88V. The frequency and peak current limit during start-up are

OPERATION

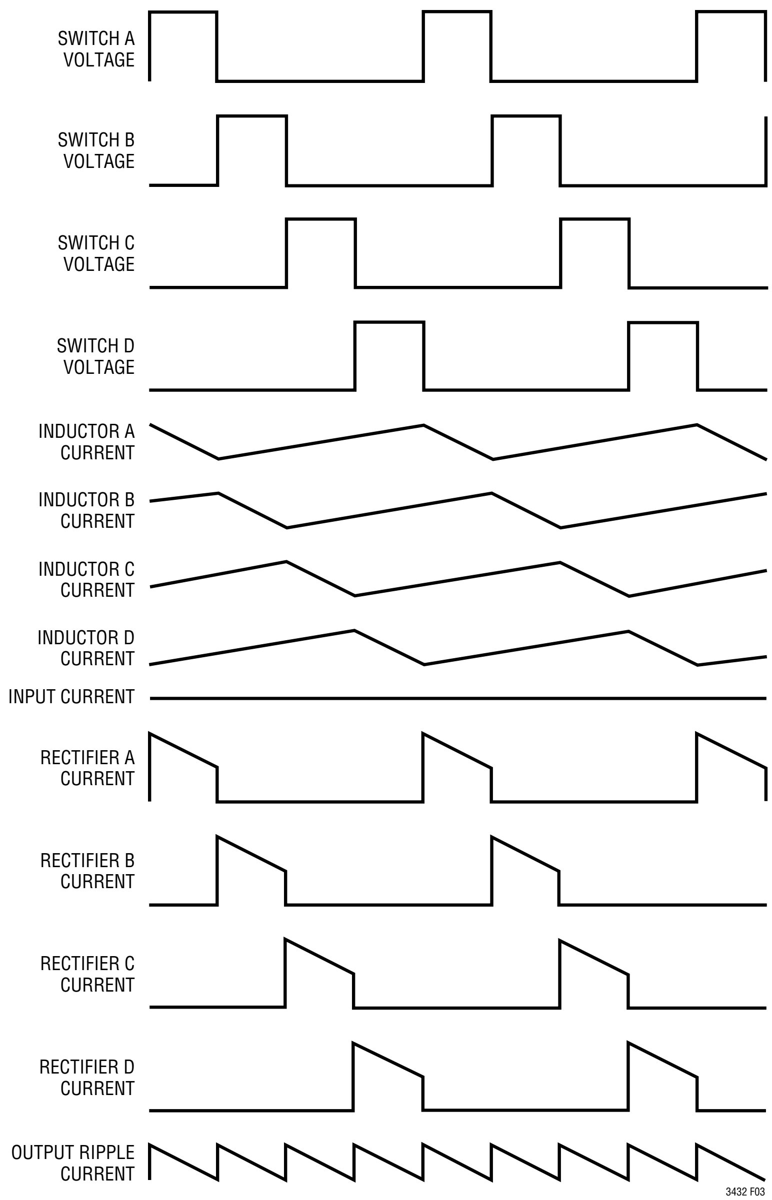


Figure 3. Simplified Voltage and Current Waveforms for 4-Phase Operation at 75% Duty Cycle

internally controlled. The device can start up under some load (see the graph Start-Up Current vs Input Voltage). Soft-start and inrush current limiting is provided during start-up as well as normal mode. The same soft-start capacitor is used for each operating mode.

During start-up, all four phases switch in unison. When either V_{IN} or V_{OUT} exceeds 2.3V, the IC enters normal operating mode. Once the output voltage exceeds the input by 0.3V, the IC powers itself from V_{OUT} instead of V_{IN}. At this point the internal circuitry has no dependency on the V_{IN} input voltage, eliminating the requirement for a large input capacitor. The input voltage can drop as low as 0.5V without affecting circuit operation. The limiting factor for the application becomes the ability of the power source to supply sufficient energy to the output at the low voltages, and the maximum duty cycle that is clamped at 90%.

OPERATION

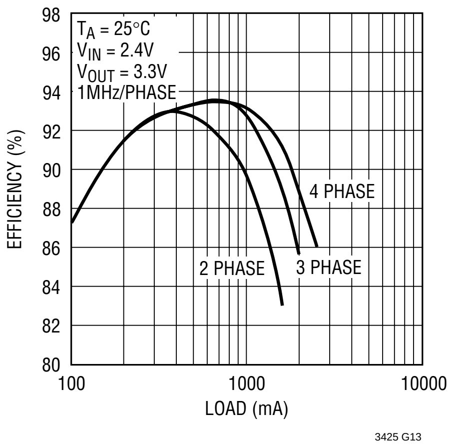


Figure 4. LTC3425 Efficiency vs Load for 2-, 3- and 4-Phase Operation

Low Noise Fixed Frequency Operation

Shutdown: The part is shut down by pulling $\overline{SHDN}$ below 0.25V and made active by pulling the pin above 1V. Note that $\overline{SHDN}$ can be driven above V_{IN} or V_{OUT}, as long as it is limited to less than 5.5V.

Soft-Start: The soft-start time is programmed with an external capacitor to ground on SS. An internal current source charges it with a nominal 2.5µA (1µA while in start-up mode when V_{IN} and V_{OUT} are both below 2.3V). The voltage on the soft-start pin (in conjunction with the external resistor on the I_{LIM} pin) is used to control the peak current limit until the voltage on the capacitor exceeds 1.6V, at which point the external resistor sets the peak current. In the event of a commanded shutdown or a thermal shutdown, the capacitor is discharged automatically. Note that Burst Mode operation is inhibited during the soft-start time.

$$t(ms) = C_{SS}(\mu F) \bullet 320$$

Oscillator: The frequency of operation is set through a resistor from the R_T pin to ground. An internally trimmed timing capacitor resides inside the IC. The internal oscillator frequency is then divided by four to generate the four phases, each phase shifted by 90°. The oscillator frequency and resulting switching frequency of each of the four phases are calculated using the following formula:

$$f_{OSC} = \frac{60}{R_T}$$

$$f_{SWITCH} = \frac{f_{OSC}}{4} = \frac{15}{R_T}$$

where f_{OSC} is in MHz and R_T is in kΩ.

The oscillator can be synchronized with an external clock applied to SYNCIN. When synchronizing the oscillator, the free running frequency must be set to an approximately 30% lower frequency than the desired synchronized frequency. SYNCOUT is provided for synchronizing two or more devices. The output sync pulse is 180° out of phase from the internal oscillator, allowing two devices to be synchronized to create an 8-phase converter. Note that in Burst Mode operation, the oscillator is turned off and SYNCOUT is driven low.

In fixed frequency operation, the minimum on-time before pulse skipping occurs (at light load) is typically 110ns.

Current Sensing: Lossless current sensing converts the peak current signal to a voltage to sum in with the internal slope compensation. This summed signal is compared to the error amplifier output to provide a peak current control command for the PWM. The internal slope-compensation is adaptive to the input and output voltage, therefore the converter provides the proper amount of slope compensation to ensure stability, but not an excess to cause a loss of phase margin in the converter.

Error Amp: The error amplifier is a transconductance amplifier with its positive input internally connected to the 1.22V reference and its negative input connected to FB. A simple compensation network is placed from COMP to ground. Internal clamps limit the minimum and maximum error amp output voltage for improved large-signal transient response. During Burst Mode operation, the compensation pin is high impedance, however clamps limit the voltage on the external compensation network, preventing the compensation capacitor from discharging to zero.

OPERATION

Current Limit: The programmable current limit circuit sets the maximum peak current in the NMOS switches. The current limit level is programmed using a resistor to ground on the I_{LIM} pin. Do not use values below 75k. In Burst Mode operation, the current limit is automatically set to a nominal value of 0.6A peak for optimal efficiency.

$$I_{LIM} = \frac{130}{R} \text{ per Phase}$$

where I is in Amps and R is in kΩ.

Synchronous Rectifier and Zero Current Amp: To prevent the inductor current from running away, the PMOS synchronous rectifier is only enabled when $V_{OUT} > (V_{IN} + 0.3V)$ and FB is > 0.8V. The zero current amplifier monitors the inductor current to the output and shuts off the synchronous rectifier once the current is below 50mA typical, preventing negative inductor current. If CCM is tied high, the amplifier will allow up to 0.6A of negative current in the synchronous rectifier.

Antiringing Control: The antiringing control connects a resistor across the inductor to damp the ringing on SW in discontinuous conduction mode. The LC_{SW} ringing (L = inductor, C_{SW} = Capacitance on Switch pin) is low energy, but can cause EMI radiation.

Power Good: An internal comparator monitors the FB voltage. If FB drops 11.4% below the regulation value, PGOOD will pull low (sink current should be limited to 10mA max). The output will stay low until the FB voltage is within 9.5% of the regulation voltage. A filter prevents noise spikes from causing nuisance trips.

Reference Output: The internal 1.22V reference is buffered and brought out to REFOUT. It is active when REFEN is pulled high (above 1.4V). For stability, a minimum of 0.1µF capacitor must be placed on REFOUT. The output can source up to 100µA and sink up to 10µA. For the lowest possible quiescent current in Burst Mode operation, the reference output should be disabled by grounding REFEN.

Thermal Shutdown: An internal temperature monitor will start to reduce the programmed peak current limit if the die temperature exceeds 135°C. If the die temperature continues to rise and reaches 150°C, the part will go into thermal shutdown and all switches will be turned off and the soft-start capacitor will be reset. The part will be enabled again when the die temperature has dropped about 10°C. Note: Overtemperature protection is intended to protect the device during momentary overload conditions. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Burst Mode Operation

Burst Mode operation can be automatic or user controlled. In automatic operation, the IC will automatically enter Burst Mode operation at light load and return to fixed frequency PWM mode for heavier loads. The user can program the average load current at which the mode transition occurs using a single resistor.

During Burst Mode operation, only Phase A is active and the other three phases are turned off, reducing quiescent current and switching losses by 75%. Note that the oscillator is also shut down in this mode, since the on time is determined by the time it takes the inductor current to reach a fixed peak current, and the off time is determined by the time it takes for the inductor current to return to zero.

In Burst Mode operation, the IC delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the IC is consuming only 12µA of quiescent current. In this mode, the output ripple has a variable frequency component with load current and will be typically 2% peak-peak. This maximizes efficiency at very light loads by minimizing switching and quiescent losses. Burst Mode ripple can be reduced slightly by using more output capacitance (47µF or greater). This capacitor does not need to be a low ESR type if low ESR ceramics are also used. Another method of reducing Burst Mode ripple is to place a small feedforward capacitor across the upper resistor in the V_{OUT} feedback divider network.

During Burst Mode operation, COMP is disconnected from the error amplifier in an effort to hold the voltage on the external compensation network where it was before entering Burst Mode operation. To minimize the effects of leakage current and stray resistance, voltage clamps limit the min and max voltage on COMP during Burst Mode operation. This minimizes the transient experienced when

OPERATION

a heavy load is suddenly applied to the converter after being in Burst Mode operation for an extended period of time.

For automatic operation, an RC network should be connected from BURST to ground. The value of the resistor will control the average load current (I_{BURST}) at which Burst Mode operation will be entered and exited (there is hysteresis to prevent oscillation between modes). The equation given for the capacitor on BURST is for the minimum value, to prevent ripple on BURST from causing the part to oscillate in and out of Burst Mode operation at the current where the mode transition occurs.

$$I_{BURST} = \frac{2.75}{R_{BURST}} \text{ to leave Burst Mode operation}$$

$$I_{BURST} = \frac{1.7}{R_{BURST}} \text{ to enter Burst Mode operation}$$

where R_{BURST} is in kΩ and I_{BURST} is in Amps. For load currents under 20mA, refer to the curve Automatic Burst Mode Thresholds vs R_{BURST}.

$$C_{BURST} = \frac{C_{OUT} \bullet V_{OUT}}{10{,}000}$$

where $C_{BURST(MIN)}$ and C_{OUT} are in µF.

When the voltage on BURST drops below 0.94V, the part will enter Burst Mode operation. When the BURST pin voltage is above 1.06V, it will be in fixed frequency mode.

In the event that a sudden load transient causes the feedback pin to drop by more than 4% from the regulation value, an internal pull-up is applied to BURST, forcing the part quickly out of Burst Mode operation. For optimum transient response when going between Burst Mode operation and PWM mode, the mode should be controlled manually by the host. This way PWM mode can be commanded before the load step occurs, minimizing output voltage droop. For manual control of Burst Mode operation, the RC network can be eliminated. To force fixed frequency PWM mode, BURST should be connected to V_{OUT}. To force Burst Mode operation, BURST should be grounded. The circuit connected to BURST should be able to sink up to 2mA. Note that Burst Mode operation is inhibited during start-up and soft-start.

Note that if V_{IN} is raised to within 200mV or less below V_{OUT}, the part will exit Burst Mode operation and the synchronous rectifier will be disabled. It will remain in fixed frequency mode until V_{IN} is at least 300mV below V_{OUT}.

If the load applied during forced Burst Mode operation (BURST = GND) exceeds the current that can be supplied, the output voltage will start to droop and the part will automatically come out of Burst Mode operation and enter fixed frequency mode, raising V_{OUT}. The part will then enter Burst Mode operation once again, the cycle will repeat, resulting in about 4% output ripple. The maximum current that can be supplied in Burst Mode operation is given by:

$$I_{O(MAX)} = \frac{0.60}{2 \bullet \left(1 + \frac{V_{OUT} - V_{IN}}{V_{IN}}\right)} \text{ in Amps}$$

Output Disconnect and Inrush Limiting

The LTC3425 is designed to allow true output disconnect by eliminating body diode conduction of the internal PMOS rectifiers. This allows V_{OUT} to go to zero volts during shutdown, drawing no current from the input source. It also allows for inrush current limiting at turn-on, minimizing surge currents seen by the input supply. Note that to obtain the advantages of output disconnect, there cannot be any external Schottky diodes connected between the switch pins and V_{OUT}.

Note: Board layout is extremely critical to minimize voltage overshoot on the switch pins due to stray inductance. Keep the output filter capacitors as close as possible to the V_{OUT} pins, and use very low ESR/ESL ceramic capacitors tied to a good ground plane.

For applications with V_{OUT} over 4.3V, Schottky diodes are required to limit the peak switch voltage to less than 6V. These must also be very close to minimize stray inductance. See the section Applications Where V_{OUT} > 4.3V.

APPLICATIONS INFORMATION

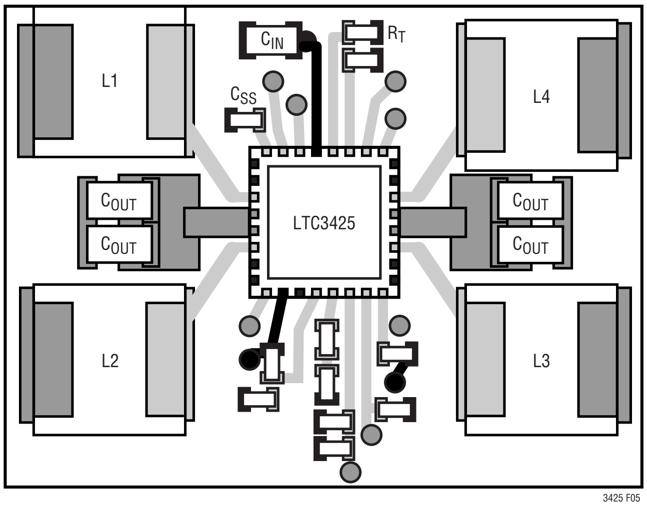


Figure 5. Typical Board Layout

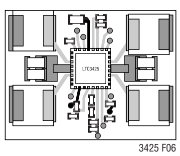


Figure 6. Example Board Layout for a 10W, 4-Phase Boost Converter. Total Area = 0.50in^2 (with All Components Mounted on the Topside of Board)

COMPONENT SELECTION

Inductor Selection

The high frequency, multiphase operation of the LTC3425 allows the use of small surface mount inductors. The minimum inductance value is proportional to the operating frequency and is limited by the following constraints:

$$L > \frac{2}{f} \quad \text{and} \quad L > \frac{V_{IN(MIN)} \bullet \left(V_{OUT(MAX)} - V_{IN(MIN)}\right)}{f \bullet \text{Ripple} \bullet V_{OUT(MAX)}}$$

where:

f = Operating frequency in MHz (of each phase)

Ripple = Allowable inductor current ripple (amps peak-peak)

$V_{IN(MIN)}$ = Minimum input voltage

$V_{OUT(MAX)}$ = Maximum output voltage

The inductor current ripple is typically set to 20% to 40% of the maximum inductor current.

For high efficiency, choose an inductor with high frequency core material, such as ferrite to reduce core loses. The inductor should have low ESR (equivalent series resistance) to reduce the I^{2}R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor. (Note that the inductance of shielded types will drop more as current increases, and will saturate more easily). See Table 2 for a list of inductor manufacturers.

Table 2. Inductor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
Coilcraft	(847) 639-6400	(847) 639-1469	www.coilcraft.com
Murata	USA: (814) 237-1431	USA: (814) 238-0490	www.murata.com
Sumida	USA: (847) 956-0666 Japan: 81-3-3607-5111	USA: (847) 956-0702 Japan: 81-3-3607-5144	www.japanlink.com/ sumida
TDK	(847) 803-6100	(847) 803-6296	www.component. tdk.com

Some example inductor part types are:

Coilcraft DO-1608, DS-1608 and DT-1608 series

Murata LQH3C, LQH4C, LQH32C and LQN6C series

Sumida CDRH3D16, CDRH4D18, CDRH4D28, CR32, CR43 series

TDK RLF5018T and NLFC453232T series

Output Capacitor Selection

The output voltage ripple has three components to it. The bulk value of the capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The max ripple due to charge is given by:

$$V_{RBULK} = \frac{I_P \bullet V_{IN}}{C_{OUT} \bullet V_{OUT} \bullet f \bullet 4}$$

where:

I_P = peak inductor current

f = switching frequency of one phase

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The ESR (equivalent series resistance) is usually the most dominant factor for ripple in most power converters. The ripple due to capacitor ESR is given by:

$$V_{RCESR} = I_P \bullet C_{ESR}$$

where C_{ESR} = Capacitor Series Resistance

The ESL (equivalent series inductance) is also an important factor for high frequency converters. Using small, surface mount ceramic capacitors, placed as close as possible to the V_{OUT} pins, will minimize ESL.

Low ESR/ESL capacitors should be used to minimize output voltage ripple. For surface mount applications, AVX TPS Series tantalum capacitors, Sanyo POSCAP or X5R type ceramic capacitors are recommended.

In all applications, a minimum of 1µF, low ESR ceramic capacitor should be placed as close to each of the four V_{OUT} pins as possible, and grounded to a local ground plane.

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the input source and reduces input switching noise. Since the IC can operate at voltages below 0.5V once the output is regulated (as long as $\overline{SHDN}$ is above 0.65V), the demand on the input capacitor to lower ripple is much less. Taiyo Yuden offers very low ESR capacitors, for example the 2.2µF in a 0603 case (JMK107BJ22MA). See Table 3 for a list of capacitor manufacturers for input and output capacitor selection.

Table 3. Capacitor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
AVX	(803) 448-9411	(803) 448-1943	www.avxcorp.com
Sanyo	(619) 661-6322	(619) 661-1055	www.sanyovideo.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com
Murata	USA: (814) 237-1431 (800) 831-9172	USA: (814) 238-0490	www.murata.com
Taiyo Yuden	(408) 573-4150	(408) 573-4159	www.t-yuden.com

Applications Where V_{OUT} > 4.3V

Due to the very high slew rates associated with the switch nodes, Schottky diode clamps are required in any application where V_{OUT} can exceed 4.3V to prevent the switch voltage from exceeding its maximum rating during the break-before-make time. Surface mount diodes, such as the MBR0520L or equivalent, must be used and must be located very close to the pins to minimize stray inductance. Two example application circuits are shown in Figures 7 and 8, one with output disconnect and one without.

Operating Frequency Selection

There are several considerations in selecting the operating frequency of the converter. The first is, which are the sensitive frequency bands that cannot tolerate any spectral noise? For example, in products incorporating RF communications, the 455kHz IF frequency is sensitive to any noise, therefore switching above 600kHz is desired. Some communications have sensitivity to 1.1MHz, and in that case, a 1.5MHz converter frequency may be employed.

The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter capacitors go down in value and size. The trade off is in efficiency, since the switching losses increase proportionally with frequency.

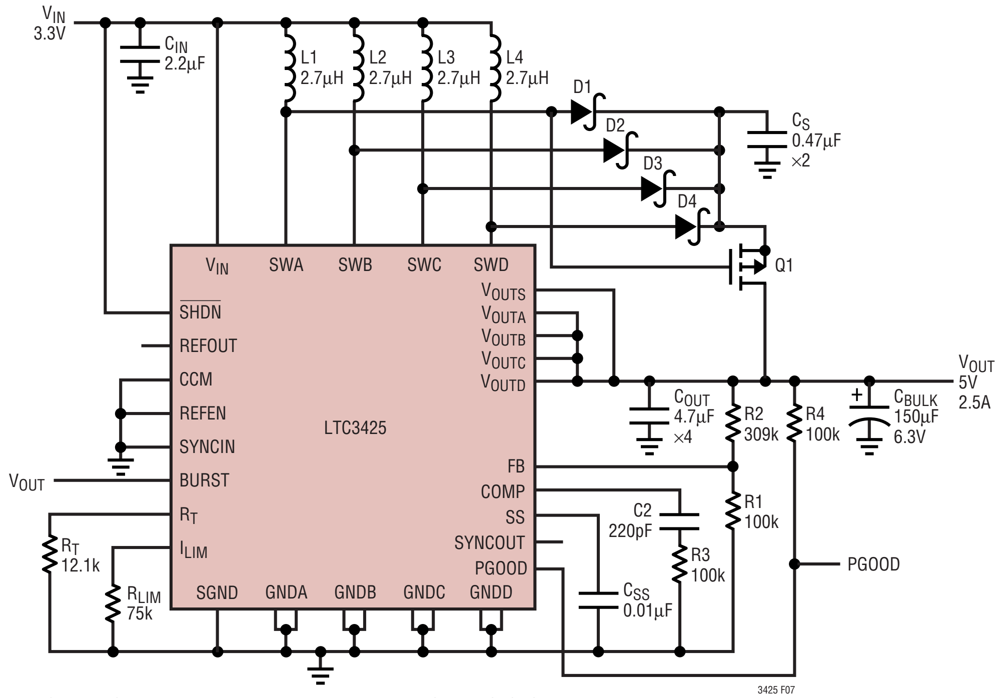
Thermal Considerations

To deliver the power that the LTC3425 is capable of, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the large thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible. In the event that the junction temperature gets too high, the peak current limit will automatically be decreased. If the junction temperature continues to rise, the part will go into thermal shutdown, and all switching will stop until the temperature drops.

Closing the Feedback Loop

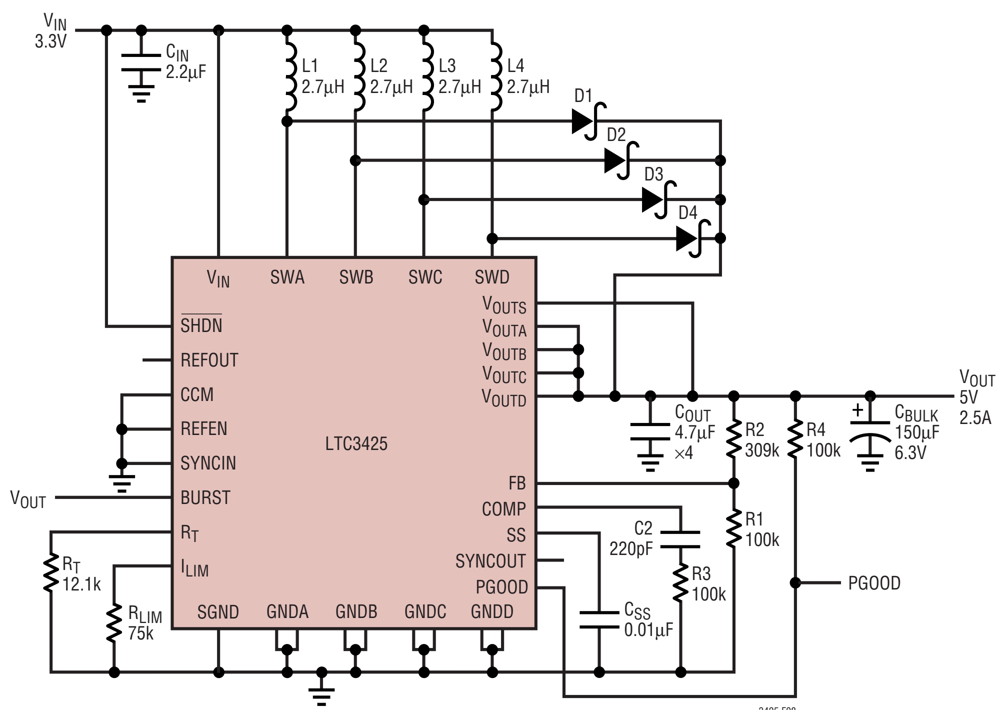
The LTC3425 uses current mode control with internal adaptive slope compensation. Current mode control eliminates the 2nd order filter, due to the inductor and output capacitor exhibited in voltage mode controllers, and simplifies it to a single pole filter response. The product of the

APPLICATIONS INFORMATION



CIN: TAIYO YUDEN JMK107BJ225MA
CS: TAIYO YUDEN LMK107BJ474KA
COUT: TAIYO YUDEN JMK212BJ475MG (×4)
CBULK: AVX TPSD157M006R0050
D1 TO D4: MOTOROLA MBR0520L
L1 TO L4: TDK RLF5018T-2R7M1R8
Q1: ZETEX ZXM61P02F

Figure 7. Application Circuit for V_{OUT} > 4.3V with Inrush Limiting and Output Disconnect



CIN: TAIYO YUDEN JMK107BJ225MA
COUT: TAIYO YUDEN JMK212BJ475MG (×4)
CBULK: AVX TPSD157M006R0050
D1 TO D4: MOTOROLA MBR0520LT1
L1 TO L4: TDK RLF5018T-2R7M1R8

Figure 8. Application Circuit for V_{OUT} > 4.3V When Inrush Limiting and Output Disconnect are Not Required

APPLICATIONS INFORMATION

modulator control to output DC gain, and the error amp open-loop gain gives the DC gain of the system:

$$G_{DC} = G_{CONTROLOUTPUT} \bullet G_{EA} \bullet \frac{V_{REF}}{V_{OUT}}$$

$$G_{CONTROL} = \frac{8 \bullet V_{IN}}{I_{OUT}}, \ G_{EA} \approx 5{,}000$$

The output filter pole is given by:

$$F_{FILTERPOLE} = \frac{I_{OUT}}{\pi \bullet V_{OUT} \bullet C_{OUT}}$$

where C_{OUT} is the output filter capacitor.
The output filter zero is given by:

$$F_{FILTERZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}}$$

where R_{ESR} is the output capacitor equivalent series resistance.

A troublesome feature of the boost regulator topology is the right half plane zero (RHP), and is given by:

$$F_{RHPZ} = \frac{V_{IN}^2}{2 \bullet \pi \bullet I_{OUT} \bullet L}$$

At heavy loads this gain increase with phase lag can occur at a relatively low frequency. The loop gain is typically rolled off before the RHP zero frequency.

The typical error amp compensation is shown in Figure 9. The equations for the loop dynamics are as follows:

$$F_{POLE1} \approx \frac{1}{2 \bullet \pi \bullet 100e^6 \bullet C_{C1}}$$

which is extremely close to DC

$$F_{ZERO1} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{C1}}$$

$$F_{POLE2} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{C2}}$$

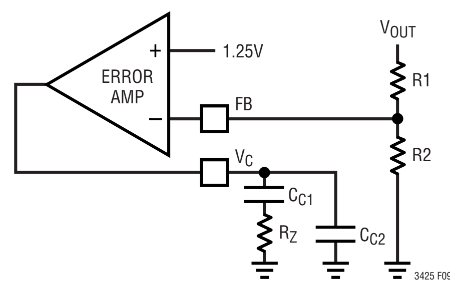
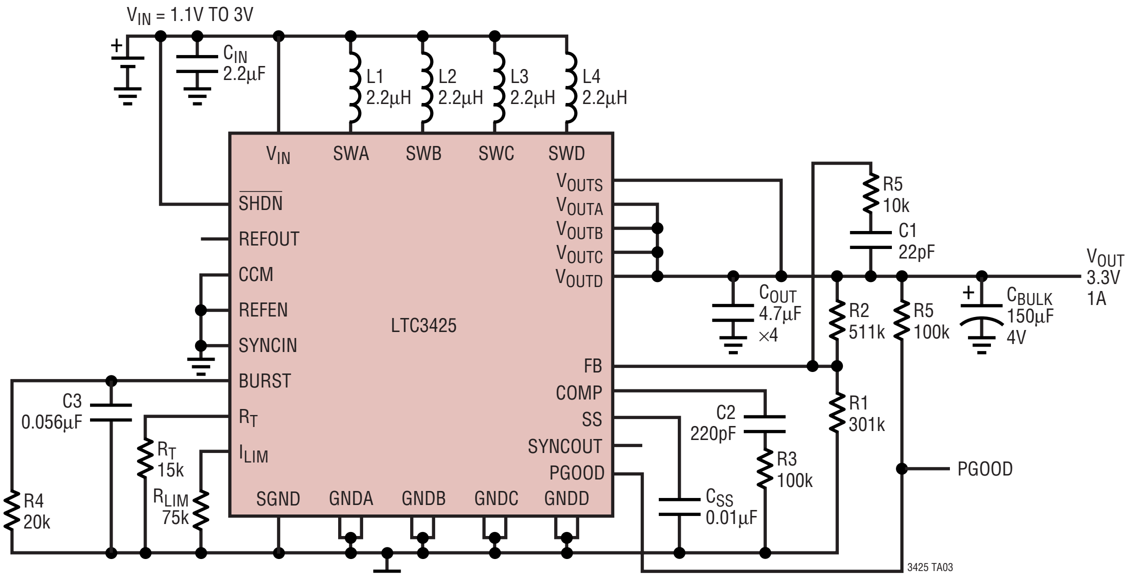


Figure 9

TYPICAL APPLICATIONS

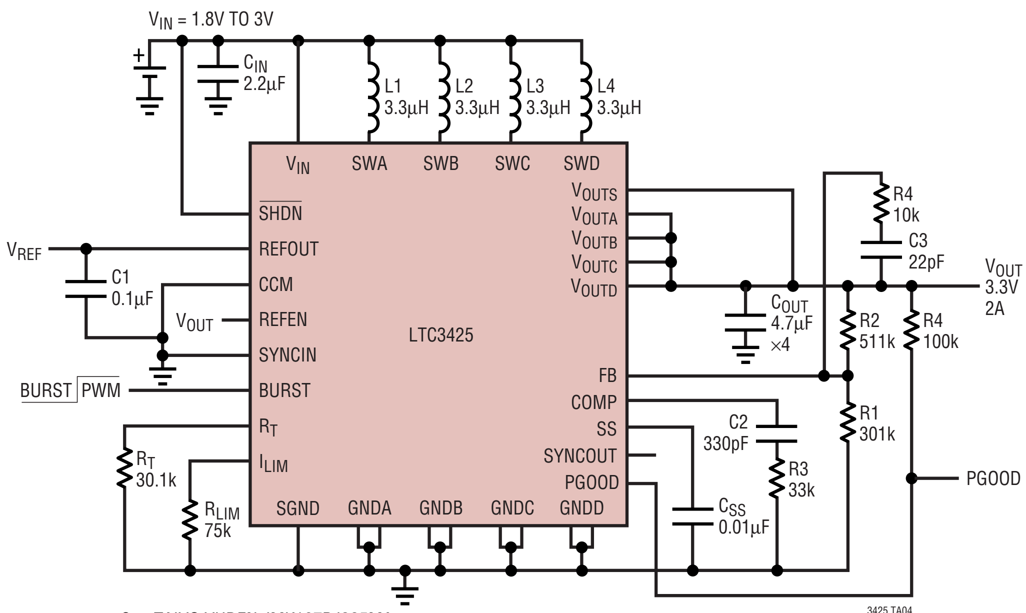
Single or Dual Cell to 3.3V Boost with Automatic Burst Mode Operation



C_{BULK}: AVX TPSD157M004R0050
C_{IN}: TAIYO YUDEN JMK107BJ225MA
C_{OUT}: TAIYO YUDEN JMK212BJ475MG (×4)
L1 TO L4: MURATA LQH4C2R2M04

TYPICAL APPLICATIONS

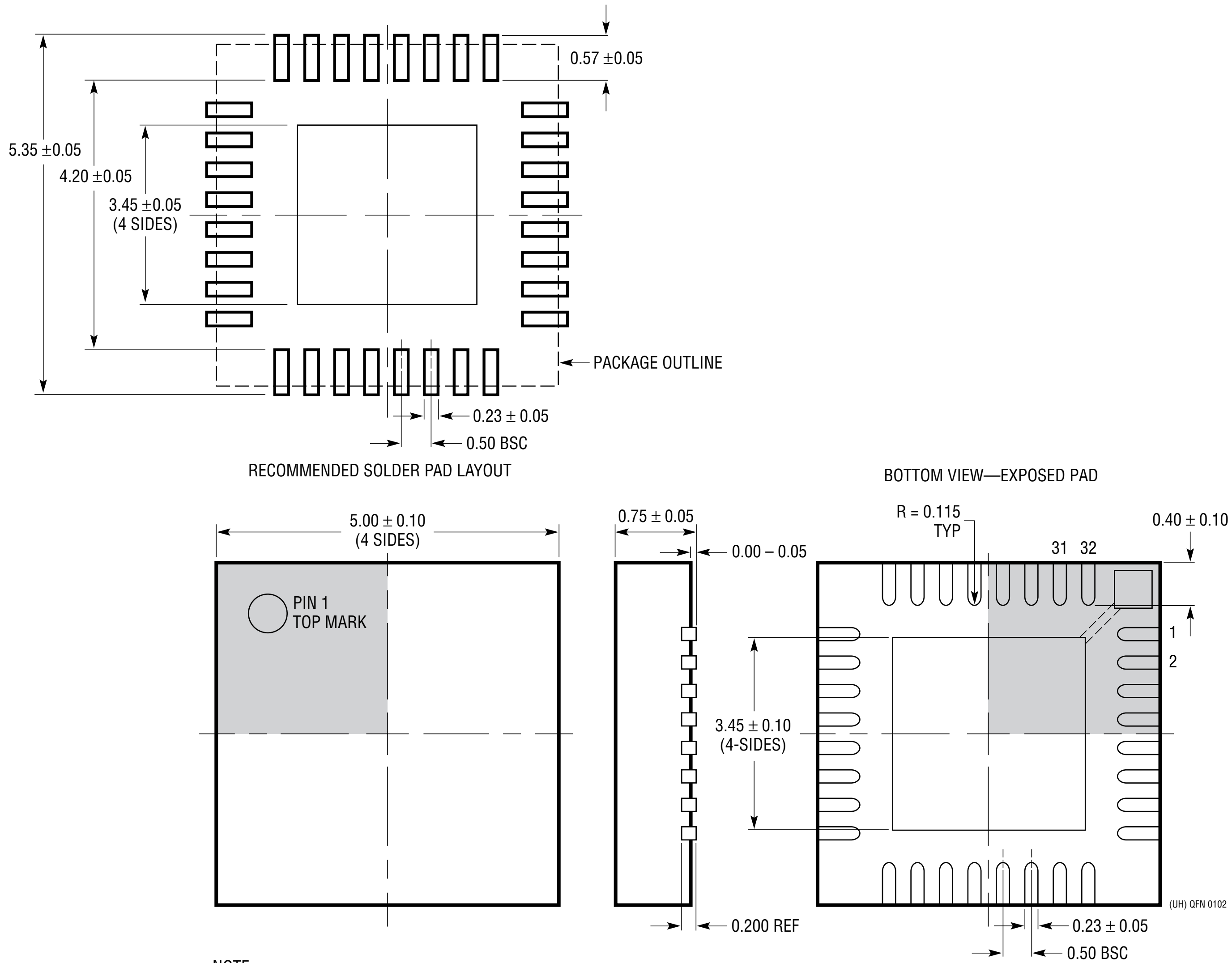
Application with User Commanded Burst Mode Operation and Buffered Reference Output Enabled



C_{IN}: TAIYO YUDEN JMK107BJ225MA
C_{OUT}: TAIYO YUDEN JMK212BJ475MG (×4)
L1 TO L4: SUMIDA CDRH4D28

PACKAGE DESCRIPTION

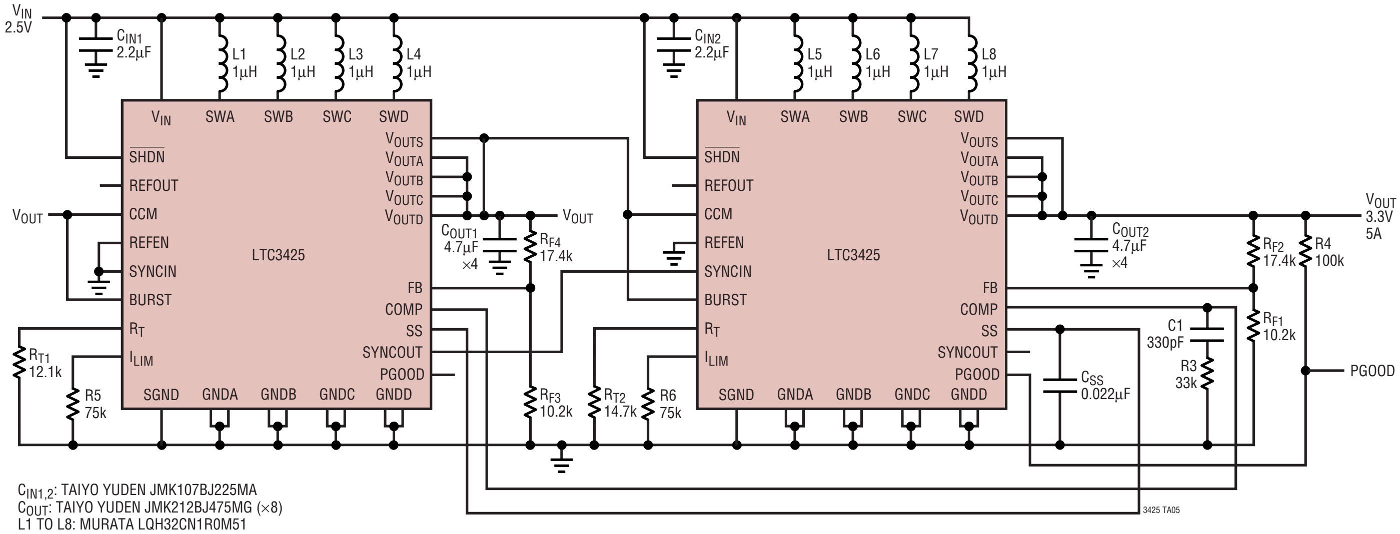
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693)



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED

TYPICAL APPLICATION

10MHz, High Current, Very Low Profile, 8-Phase Converter Using Two LTC3425s Operating in Fixed Frequency Mode with Forced CCM (Max Component Height = 1.6mm)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1370/LT1370HV	6A (I_{SW}) 500kHz, High Efficiency Step-Up DC/DC Converters	V_{IN}: 2.7V to 30V, $V_{OUT(MAX)}$: 35V/42V, I_Q: 4.5mA, I_{SD}: <12µA, DD, TO220-7
LT1371/LT1371HV	3A (I_{SW}) 500kHz, High Efficiency Step-Up DC/DC Converters	V_{IN}: 2.7V to 30V, $V_{OUT(MAX)}$: 35V/42V, I_Q: 4mA, I_{SD}: <12µA, DD, TO220-7, S20
LT1613	550mA (I_{SW}) 1.4MHz, High Efficiency Step-Up DC/DC Converter	90% Efficiency, V_{IN}: 0.9V to 10V, $V_{OUT(MAX)}$: 34V, I_Q: 3mA, I_{SD}: <1µA, ThinSOT
LT1618	1.5A (I_{SW}) 1.25MHz, High Efficiency Step-Up DC/DC Converter	90% Efficiency, V_{IN}: 1.6V to 18V, $V_{OUT(MAX)}$: 35V, I_Q: 1.8mA, I_{SD}: <1µA, MS10
LTC1700	No R_{SENSE}™ 530kHz, Synchronous Step-Up DC/DC Controller	95% Efficiency, V_{IN}: 0.9V to 5V, I_Q: 200µA, I_{SD}: <10µA, MS10
LTC1871	Wide Input Range, 1MHz, No R_{SENSE} Current Mode Boost, Flyback and SEPIC Controller	92% Efficiency, V_{IN}: 2.5V to 36V, I_Q: 250µA, I_{SD}: <10µA, MS10
LT1930/LT1930A	1A (I_{SW}) 1.2MHz/2.2MHz, High Efficiency Step-Up DC/DC Converters	High Efficiency, V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$: 34V, I_Q: 4.2mA/5.5mA, I_{SD}: <1µA, ThinSOT
LT1946/LT1946A	1.5A (I_{SW}) 1.2MHz/2.7MHz, High Efficiency Step-Up DC/DC Converters	High Efficiency, V_{IN}: 2.45V to 16V, $V_{OUT(MAX)}$: 34V, I_Q: 3.2mA, I_{SD}: <1µA, MS8
LT1961	1.5A (I_{SW}) 1.25MHz, High Efficiency Step-Up DC/DC Converter	90% Efficiency, V_{IN}: 3V to 25V, $V_{OUT(MAX)}$: 35V, I_Q: 0.9mA, I_{SD}: 6µA, MS8E
LTC3400/LTC3400B	600mA (I_{SW}) 1.2MHz, Synchronous Step-Down DC/DC Converters	92% Efficiency, V_{IN}: 0.85V to 5V, $V_{OUT(MAX)}$: 5V, I_Q: 19µA/300µA, I_{SD}: <1µA, ThinSOT
LTC3401/LTC3402	1A/2A (I_{SW}) 3MHz, Synchronous Step-Up DC/DC Converters	97% Efficiency, V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$: 6V, I_Q: 38µA, I_{SD}: <1µA, MS10
LTC3701	2-Phase, 550kHz, Low Input Voltage, Dual Step-Down DC/DC Controller	97% Efficiency, V_{IN}: 2.5V to 10V, I_Q: 460µA, I_{SD}: <9µA, SSOP-16

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