

HF/VHF/UHF RF power N-channel MOSFETs

Datasheet - production data

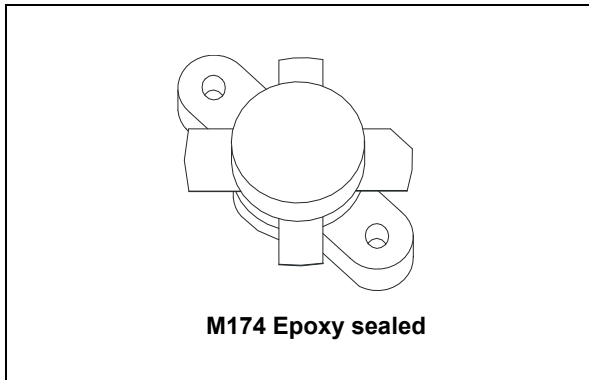
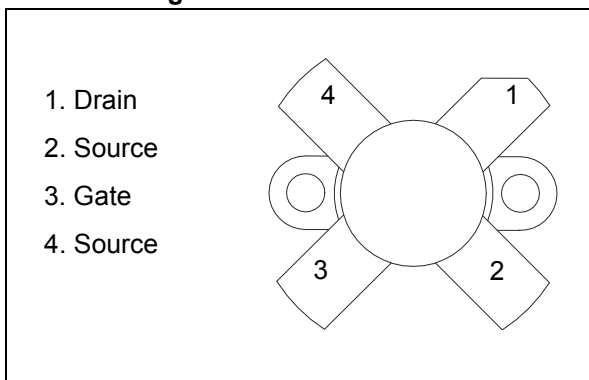


Figure 1. Pin connection



Features

- Gold metallization
- Excellent thermal stability
- Common source configuration
- $P_{OUT} = 175$ W min. with 15 dB gain @ 175 MHz, 50 V
- $P_{OUT} = 135$ W typ. with 14 dB gain @ 123 MHz, 28 V
- Low $R_{DS(on)}$
- Thermally enhanced packaging for lower junction temperatures
- In compliance with the 2002/95/EC1 European directive

Description

The SD2941-10 is a gold metallized N-channel MOS field-effect RF power transistor, intended for use in 28 V to 50 V dc large signal applications up to 230 MHz. It offers 25% lower $R_{DS(on)}$ than the industry standard, with 20% higher P_{SAT} than ST's SD2931-10 device. The SD2941-10 is housed in the low thermal M174 non-pedestal package, offering 25% lower thermal resistance than the industry standard, thus rendering it the "best-in-class" transistor for ISM applications, where reliability and ruggedness are critical factor.

Table 1. Device summary

Order code	Marking	Base qty.	Package	Packaging ⁽¹⁾
SD2941-10W	SD2941-10 ⁽¹⁾	25 pcs	M174	Plastic tray

1. For more details please refer to [Chapter 7: Marking, packing and shipping specifications](#).

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1 Electrical data

1.1 Maximum rating

($T_{CASE} = 25\text{ °C}$)

Table 2. Absolute maximum rating

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}^{(1)}$	Drain source voltage	130	V
$V_{DGR}^{(1)}$	Drain-gate voltage ($R_{GS} = 1M\Omega$)	130	V
V_{GS}	Gate-source voltage	± 40	V
I_D	Drain current	20	A
P_{DISS}	Power dissipation	389	W
T_J	Max. operating junction temperature	200	$^{\circ}C$
T_{STG}	Storage temperature	-65 to +150	$^{\circ}C$

1. $T_J = 150\text{ °C}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction to case thermal resistance	0.45	$^{\circ}C/W$

2 Electrical characteristics

(T_{CASE} = 25 °C)

Table 4. Static

Symbol	Test conditions		Min.	Typ.	Max.	Unit
V _{(BR)DSS} ⁽¹⁾	V _{GS} = 0 V	I _{DS} = 100 mA	130			V
I _{DSS}	V _{GS} = 0 V	V _{DS} = 50 V			50	mA
I _{GSS}	V _{GS} = 20 V	V _{DS} = 0 V			250	nA
V _{GS(Q)} ⁽²⁾	V _{DS} = 10 V	I _D = 250 mA				V
V _{DS(ON)}	V _{GS} = 10 V	I _D = 10 A			2.0	V
G _{FS}	V _{DS} = 10 V	I _D = 5 A	5	6		mho
C _{ISS}	V _{GS} = 0 V	V _{DS} = 50 V f = 1 MHz		415		pF
C _{OSS}	V _{GS} = 0 V	V _{DS} = 50 V f = 1 MHz		236		pF
CRSS	V _{GS} = 0 V	V _{DS} = 50 V f = 1 MHz		17		pF

1. T_J = 150°C
2. V_{GS(Q)} sorted with alpha/numeric code marked on unit.

Table 5. Dynamic

Symbol	Test conditions		Min.	Typ.	Max.	Unit	
P _{OUT}	V _{DD} = 28 V I _{DQ} = 250 mA f = 123 MHz			135	-	W	
	V _{DD} = 50 V I _{DQ} = 250 mA f = 175 MHz		175	200			
G _{PS}	V _{DD} = 28 V I _{DQ} = 250 mA P _{OUT} = 135 W f = 123 MHz			14		-	dB
	V _{DD} = 50 V I _{DQ} = 250 mA P _{OUT} = 175 W f = 175 MHz		14	15.8			
h _D	V _{DD} = 28 V I _{DQ} = 250 mA P _{OUT} = 135 W f = 123 MHz			65		-	%
	V _{DD} = 50 V I _{DQ} = 250 mA P _{OUT} = 175 W f = 175MHz		55	65			
Load Mismatch	V _{DD} = 50 V I _{DQ} = 250 mA P _{OUT} = 175 W f = 175MHz All phase angles		10:1		-	VSWR	
	V _{DD} = 28 V I _{DQ} = 250 mA P _{OUT} = 135 W f = 123 MHz All phase angles		25:1				

Table 6. V_{GS} sorts

Symbol	Value	Symbol	Value	Symbol	Value
AA	1.5 - 1.6	E	2.4 - 2.5	P	3.3 - 3.4
BB	1.6 - 1.7	F	2.5 - 2.6	Q	3.4 - 3.5
CC	1.7 - 1.8	G	2.6 - 2.7	R	3.5 - 3.6
DD	1.8 - 1.9	H	2.7 - 2.8	S	3.6 - 3.7
EE	1.9 - 2.0	J	2.8 - 2.9	T	3.7 - 3.8
A	2.0 - 2.1	K	2.9 - 3.0	U	3.8 - 3.9
B	2.1 - 2.2	L	3.0 - 3.1	V	3.9 - 4.0
C	2.2 - 2.3	M	3.1 - 3.2		
D	2.3 - 2.4	N	3.2 - 3.3		

3 Impedance

Figure 2. Impedance data schematic

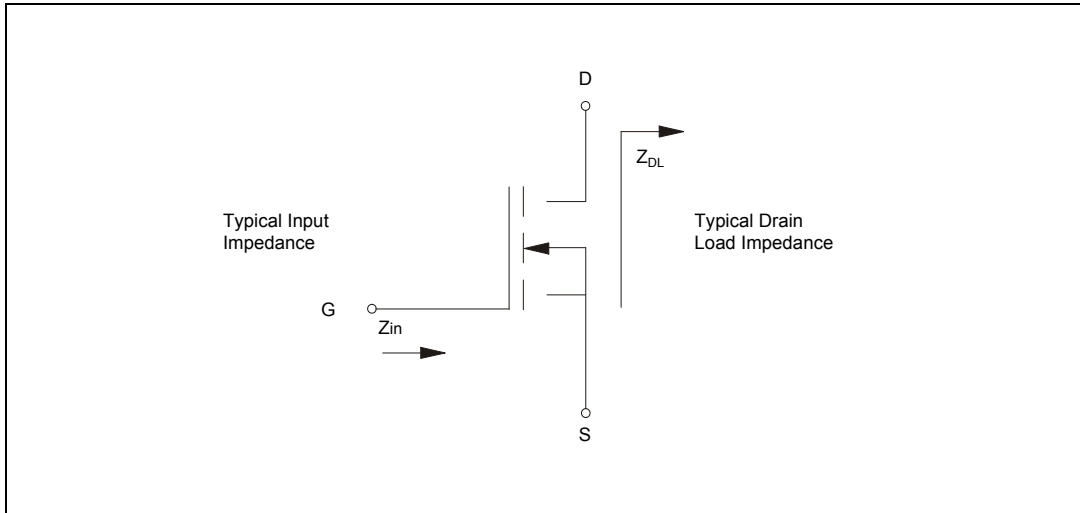


Table 7. Impedance data @ 28 V

f	Z_{IN} (Ω)	Z_{DL} (100W) (Ω)	Z_{DL} (140W) (Ω)
123 MHz	$1.2 - j 3.3$	$2.0 + j 1.4$	$2.0 + j 0.73$

Table 8. Impedance data @ 50 V

f	Z_{IN} (Ω)	Z_{DL} (Ω)
30 MHz	$1.7 - j 5.7$	$6.8 + j 0.9$
175 MHz	$1.2 - j 2.0$	$2.0 + j 2.4$

4 Typical performance

Figure 3. Capacitance vs drain voltage

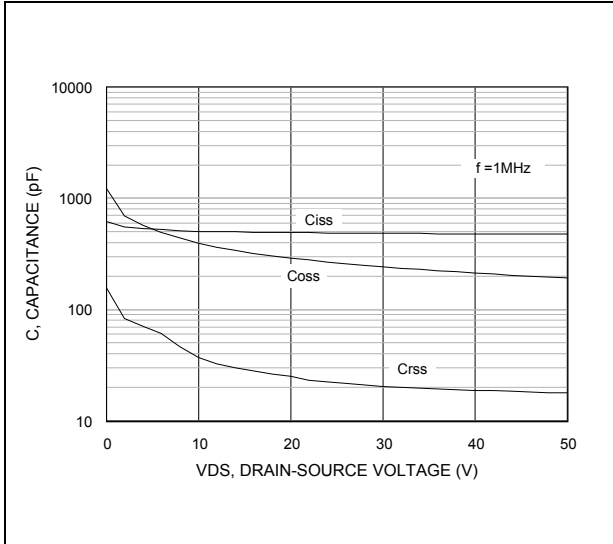


Figure 4. Drain current vs gate voltage

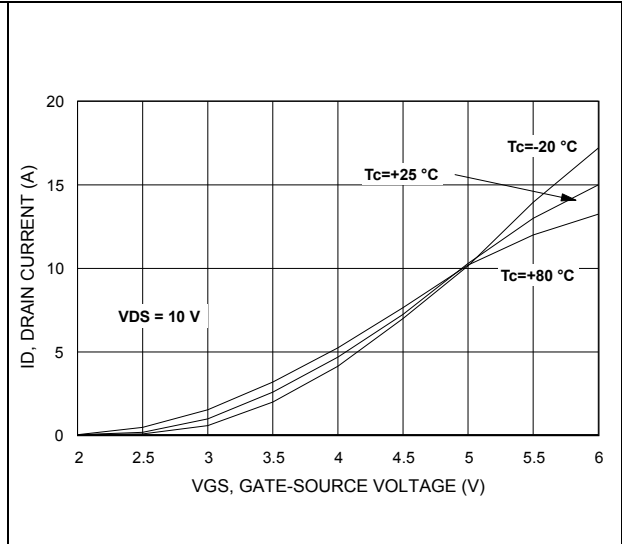


Figure 5. Maximum thermal resistance vs case temperature

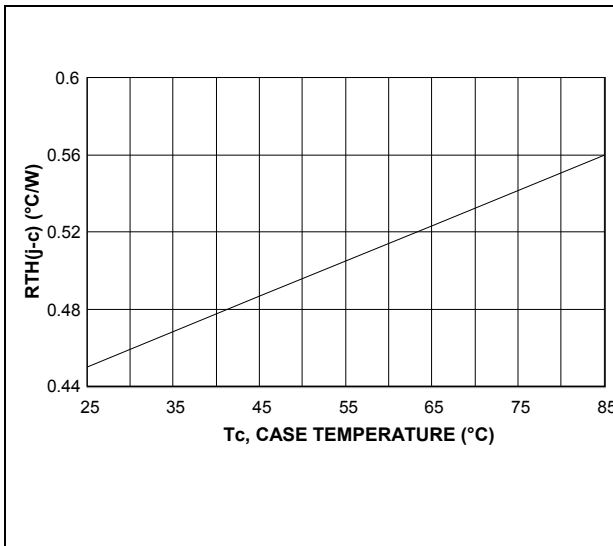


Figure 6. Safe operating area

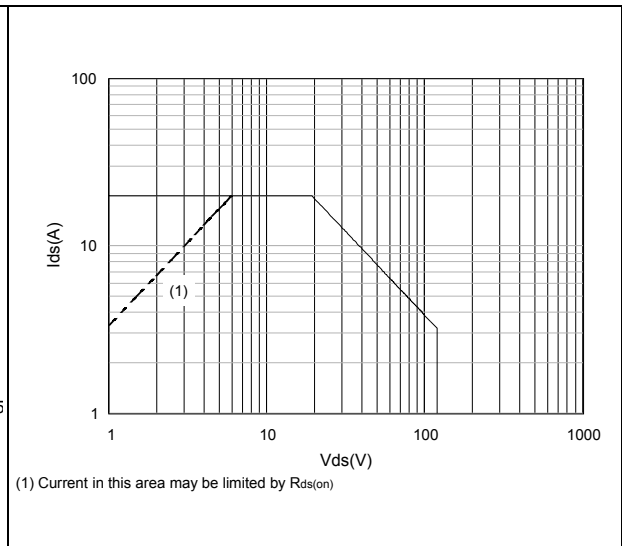


Figure 7. Power gain vs output power

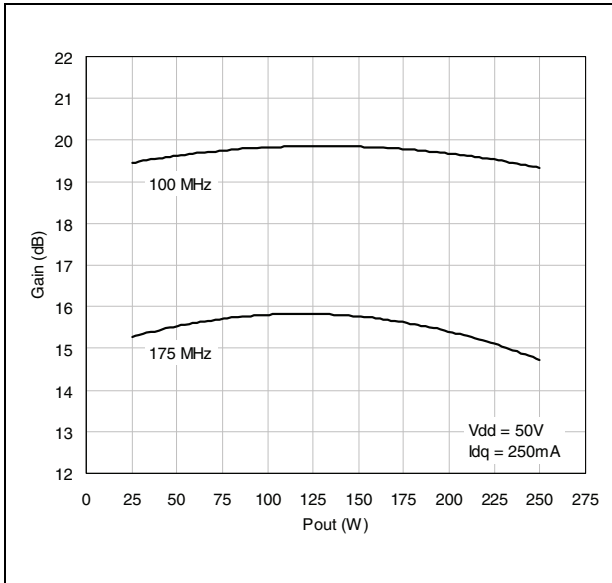


Figure 8. Efficiency vs output power

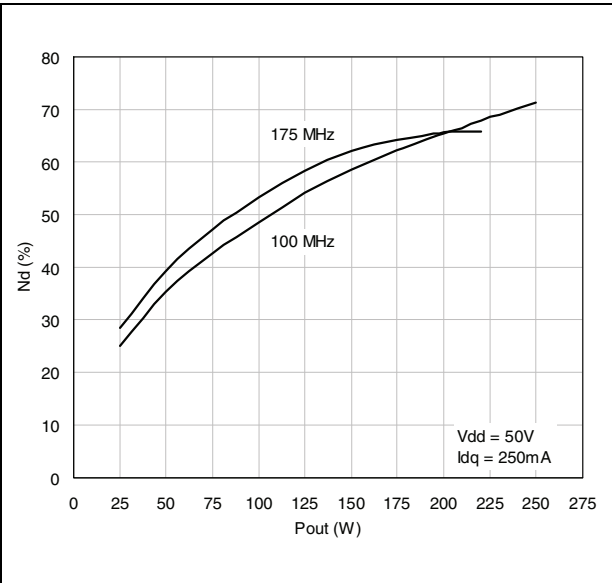


Figure 9. Input return loss vs output power

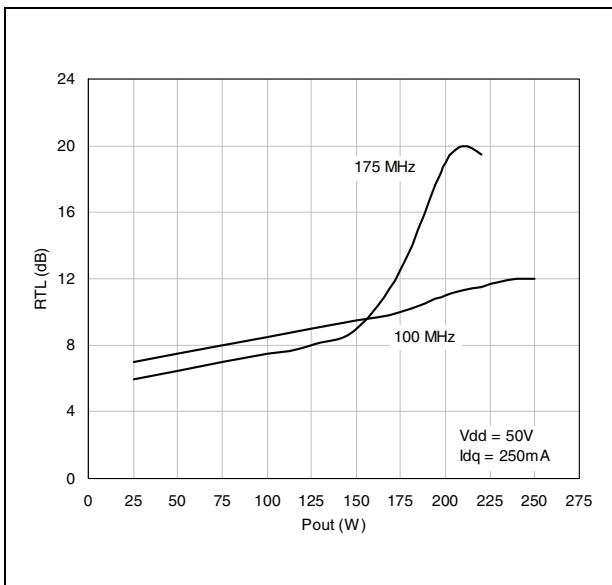


Figure 10. Gain and efficiency vs output power @ 28V and 100W load line

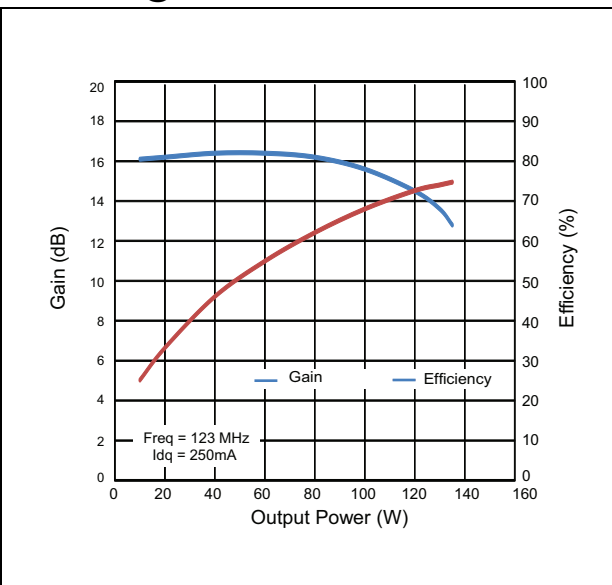
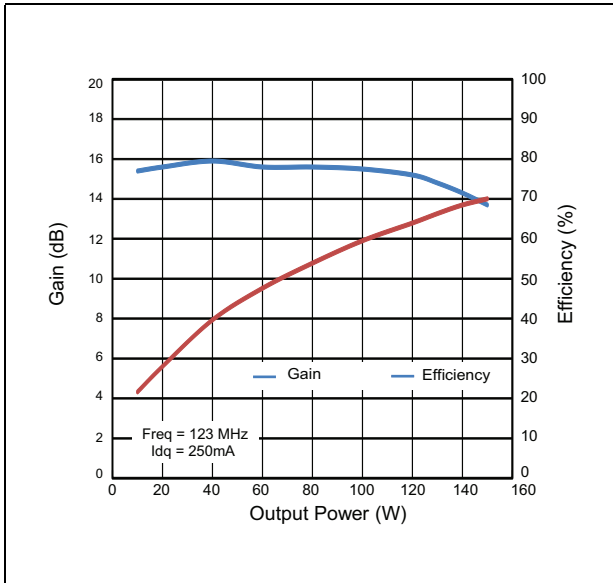
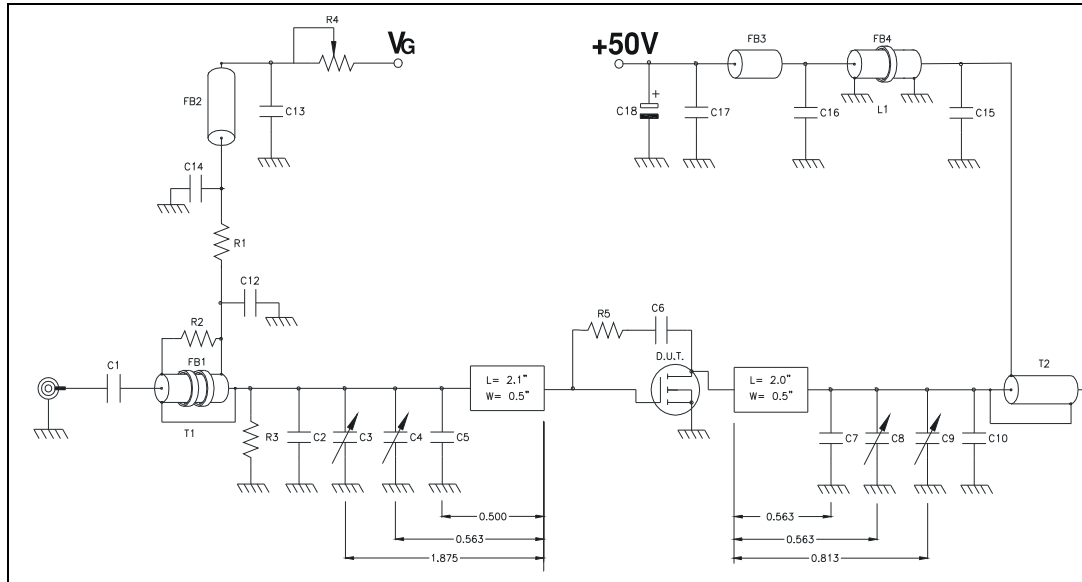


Figure 11. Gain and efficiency vs output power @ 28V and 140W load line



5 Test circuit

Figure 12. 30 MHz test circuit schematic (engineering test circuit)



Note: All dimension are in inches.

Table 9. 30 MHz test circuit component part list

Symbol	Description
T2	1:4 transformer, 25 Ω semi-rigid coax.141 OD 6" Long
FB1	Toroid X 2, 0.5" OD.312" ID 850μ 2 turns
FB2, FB3	VK200
FB4	Shield bead, 1" OD 0.5" ID 850μ 3 Turns
L1	1/4 Wave Choke, 50W Semi-rigid coax.141 OD 12" Long
PCB	0.62" woven fiberglass, 1 oz. copper, 2 sides, $\epsilon_r = 2.55$
R1, R3	470 Ω 1 W chip resistor
R2	360 Ω 1/2 W resistor
R4	20 KΩ 10 turn potentiometer
R5	560 Ω 1 W resistor
C1, C11	470 pF ATC chip cap
C2	43 pF ATC chip cap
C3, C8, C9	Arco 404, 12-65 pF
C4	Arco 423, 16-100 pF
C5	120 pF ATC chip cap
C6	0.01 μF ATC chip cap
C7	30 pF ATC chip cap

Table 9. 30 MHz test circuit component part list (continued)

Symbol	Description
C10	91 pF ATC chip cap
C12, C15	1200 pF ATC chip cap
C13, C14,C16, C17	0.01 mF / 500 V chip cap
C18	10 mF 63 V electrolytic capacitor

Figure 13. 175 MHz test circuit photomaster

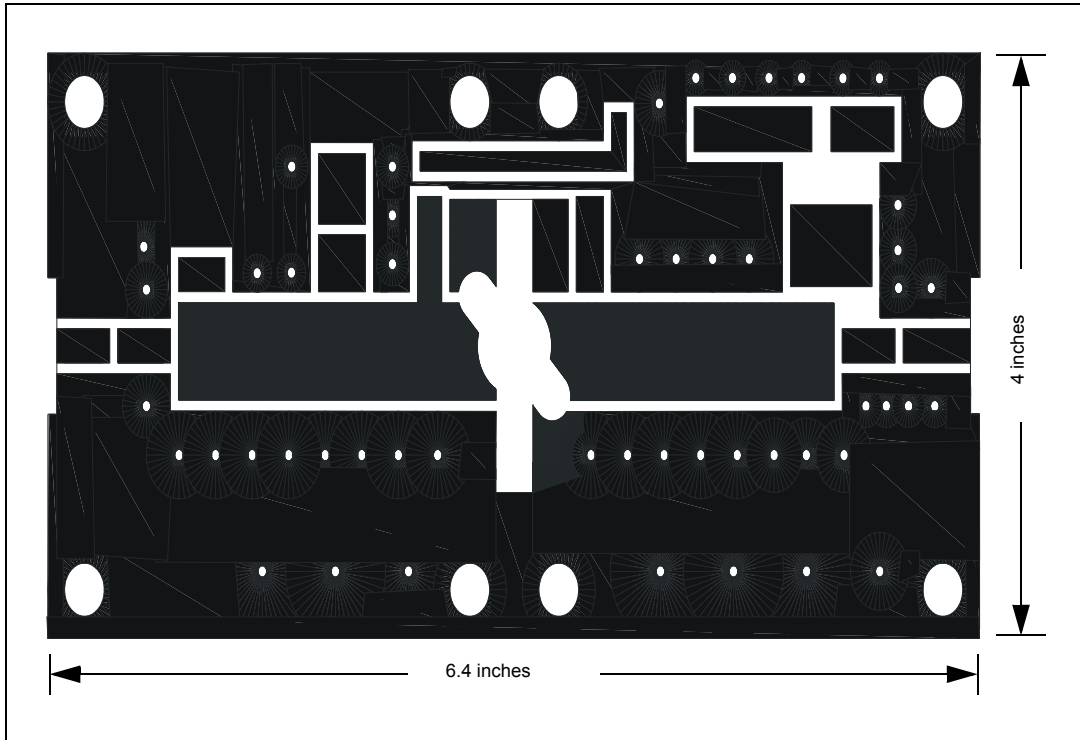
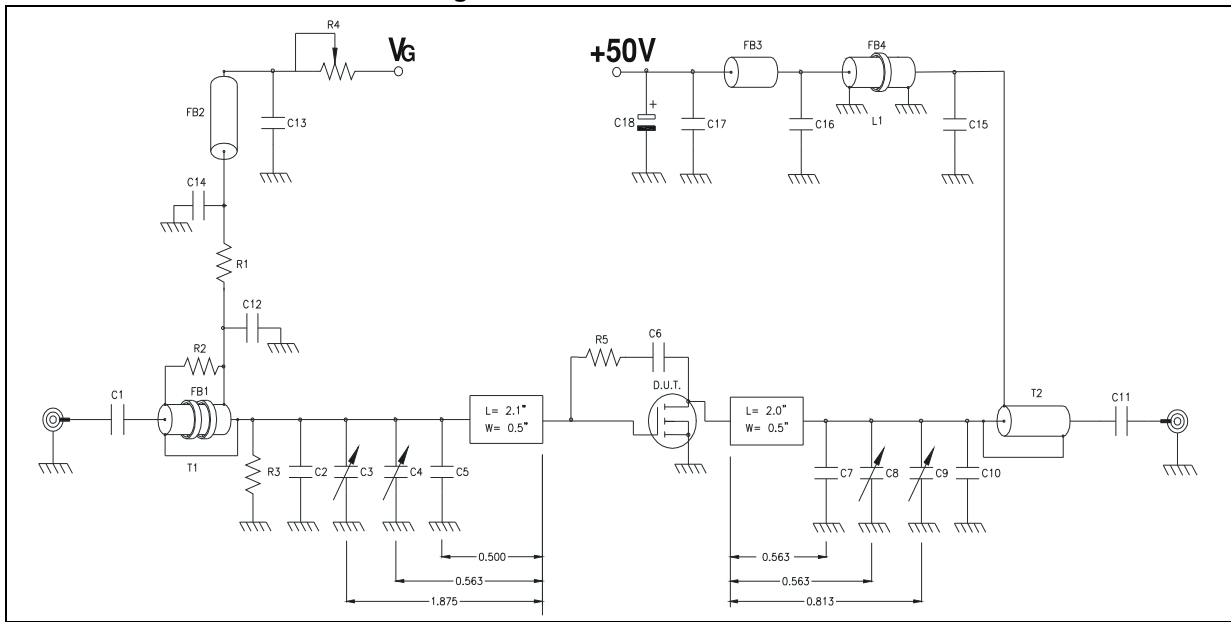


Figure 14. 175 MHz test circuit



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 15. M174 package dimensions

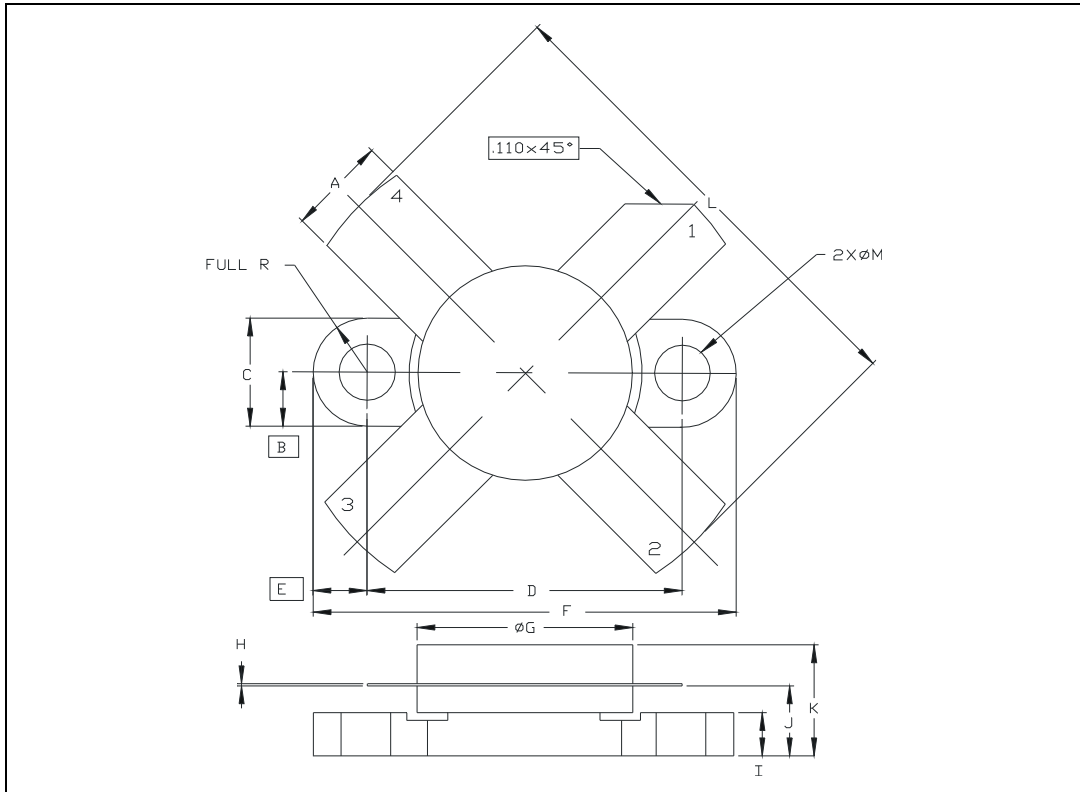


Table 10. M174 (.500 DIA 4/L N/HERM W/FLG)

DIM.	mm.			inch		
	min.	typ.	max	min.	typ.	max
A	5.56		5.584	0.219		0.230
B		3.18			0.125	
C	6.22		6.48	0.245		0.255
D	18.28		18.54	0.720		0.730
E		3.18			0.125	
F	24.64		24.89	0.970		0.980
G	12.57		12.83	0.495		0.505
H	0.08		0.18	0.003		0.007
I	2.11		3.00	0.083		0.118
J	3.81		4.45	0.150		0.175
K			7.11			0.280
L	25.53		26.67	1.005		1.050
M	3.05		3.30	0.120		0.130

7 Marking, packing and shipping specifications

Table 11. Packing and shipping specifications

Order code	Packaging	Pcs per tray	Dry pack humidity	V _{GS} code	Lot code
SD2941-10W	Plastic tray	25	< 10%	Not mixed	Not mixed

Figure 16. Marking layout

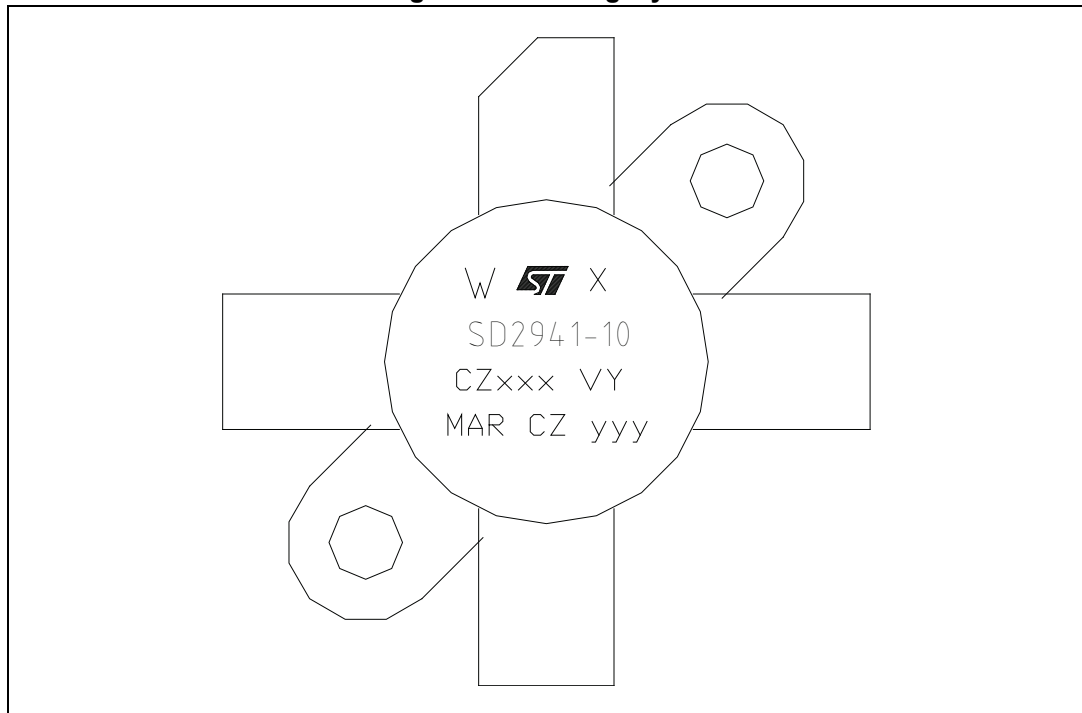


Table 12. Marking specifications

Symbol	Description
W	Wafer process code
X	V _{GS} sort
CZ	Assembly plant
xxx	Last 3 digit of diffusion lot
VY	Diffusion plant
MAR	Country of origin
CZ	Test and finishing plant
y	Assembly year
yy	Assembly week

8 Revision history

Table 13. Document revision history

Date	Revision	Changes
15-Nov-2005	1	Initial release
06-Apr-2006	2	Complete version
13-Apr-2006	3	V _{DS(ON)} updated
19-Oct-2011	4	Inserted Section 7: Marking, packing and shipping specifications . Minor text changes in the title and description on the coverpage.
04-Aug-2014	5	Added performances at 28 V.
14-Aug-2015	6	Updated Table 2.: Absolute maximum rating . Minor text changes.

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