PESD5V0S1ULD

Unidirectional ESD protection diode

8 March 2017 **Product data sheet**

1. General description

Unidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a SOD882D leadless ultra small Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

2. Features and benefits

- ESD protection of one line
- ESD protection up to 30 kV
- Ultra small SMD plastic package
- IEC 61000-4-2; level 4 (ESD)
- Solderable side pads
- IEC 61000-4-5 (surge); I_{PP} = 15 A
- Package height typ. 0.37 mm
- Max. peak pulse power: P_{PP} = 150W
- Low clamping voltage: V_{CL} = 20 V
- Ultra low leakage current: I_{RM} = 100 nA
- AEC-Q101 qualified

3. Applications

- Computers and peripherals
- Communication systems
- Audio and video equipment
- Portable electronics

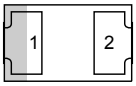
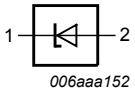
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5.5	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	152	200	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode[1]	 Transparent top view **DFN1006D-2 (SOD882D)**	
2	A	anode		

[1] The marking bar indicates the cathode.

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0S1ULD	DFN1006D-2	DFN1006D-2: leadless ultra small plastic package; 2 terminals	SOD882D

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0S1ULD	0100 0000

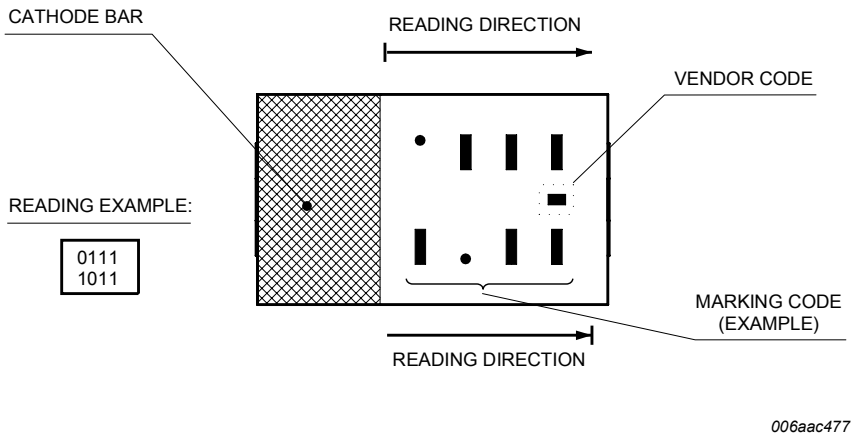


Fig. 1. SOD882D binary marking code description

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{PPM}	rated peak pulse power	t_p = 8/20 µs	[1]	-	150	W
I_{PPM}	rated peak pulse current		[1]	-	15	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	125	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[2] [3]	-	30	kV
		MIL-STD-883 (human body model)		-	10	kV

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[2] Device stressed with ten non-repetitive ESD pulses.
[3] Measured from pin 1 to pin 2.

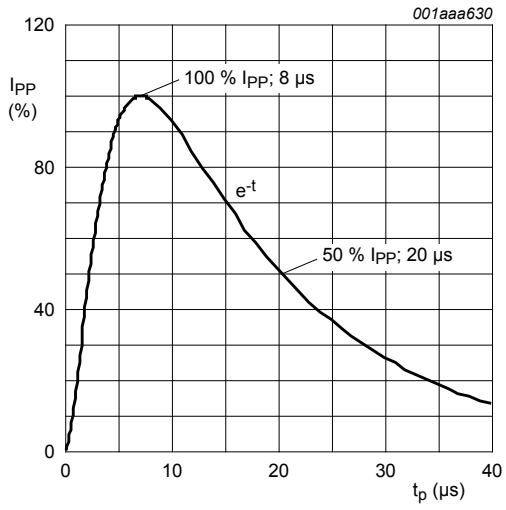


Fig. 2. 8/20 µs pulse waveform according to IEC 61000-4-5

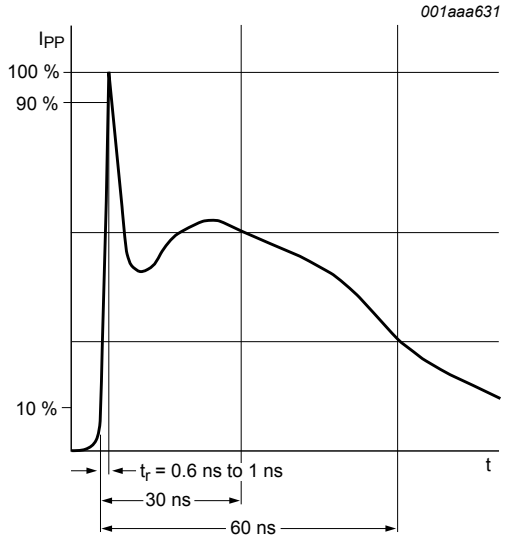


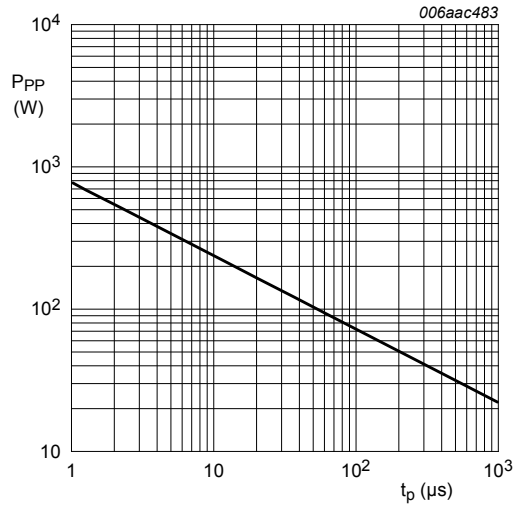
Fig. 3. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5.5	V
V_{BR}	breakdown voltage	I_R = 5 mA; T_{amb} = 25 °C		6.4	6.8	7.2	V
I_{RM}	reverse leakage current	V_{RWM} = 5.5 V; T_{amb} = 25 °C	[1]	-	0.1	1	µA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	152	200	pF
V_{CL}	clamping voltage	I_{PP} = 1 A; T_{amb} = 25 °C	[2] [1]	-	-	9	V
		I_{PP} = 15 A; T_{amb} = 25 °C	[2] [1]	-	-	20	V
R_{dyn}	dynamic resistance	I_R = 10 A; T_{amb} = 25 °C	[1] [3]	-	0.3	-	Ω

[1] Measured from pin 1 or 2 to pin 3.
[2] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[3] Non-repetitive current pulse; Transmission Line Pulse (TLP) t_p = 100 ns; square pulse.



T_{amb} = 25 °C

Fig. 4. Peak pulse power as a function of exponential pulse duration; typical values

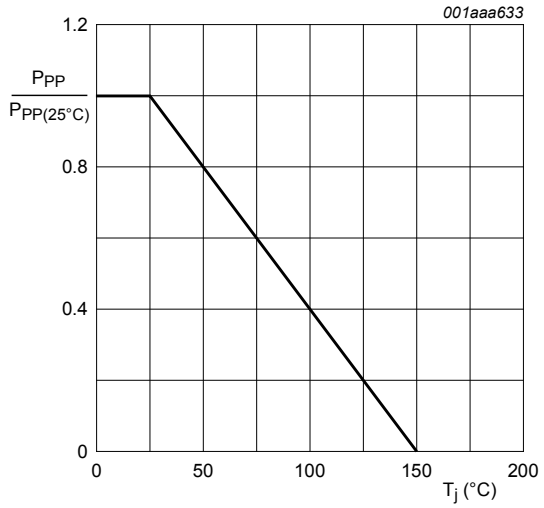
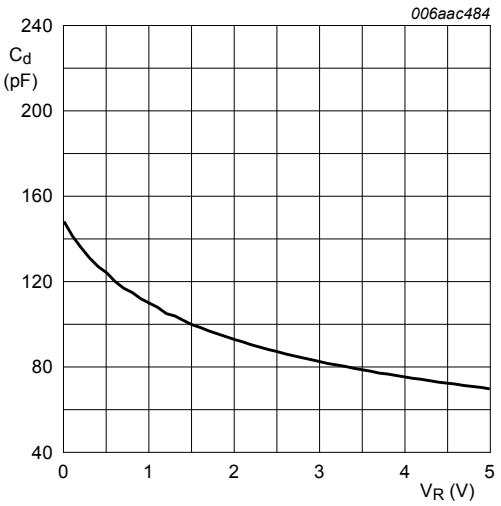


Fig. 5. Relative variation of peak pulse power as a function of junction temperature; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig. 6. Diode capacitance as a function of reverse voltage; typical values

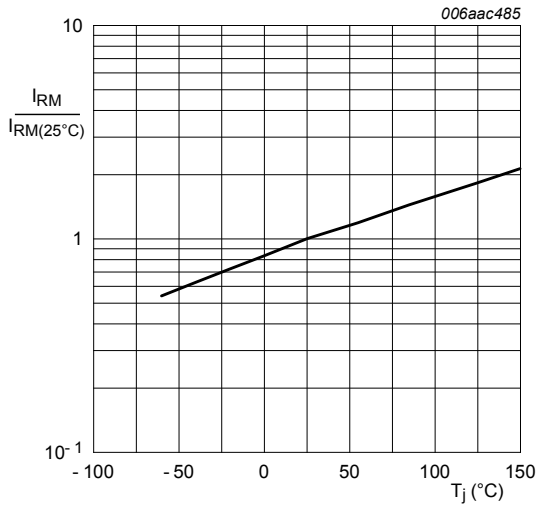


Fig. 7. Relative variation of reverse leakage current as a function of junction temperature; typical values

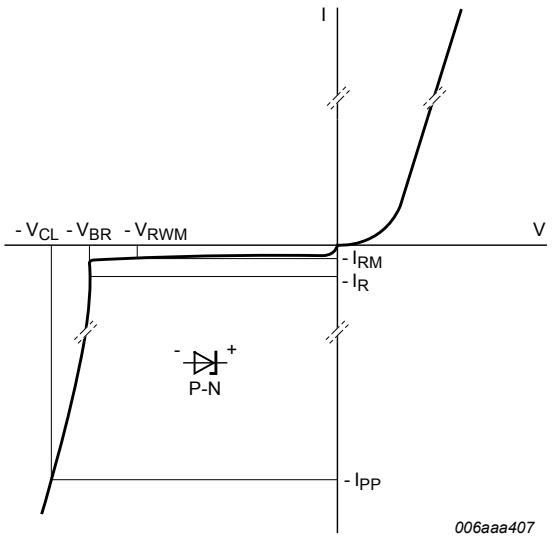


Fig. 8. V-I characteristics for unidirectional ESD protection diode

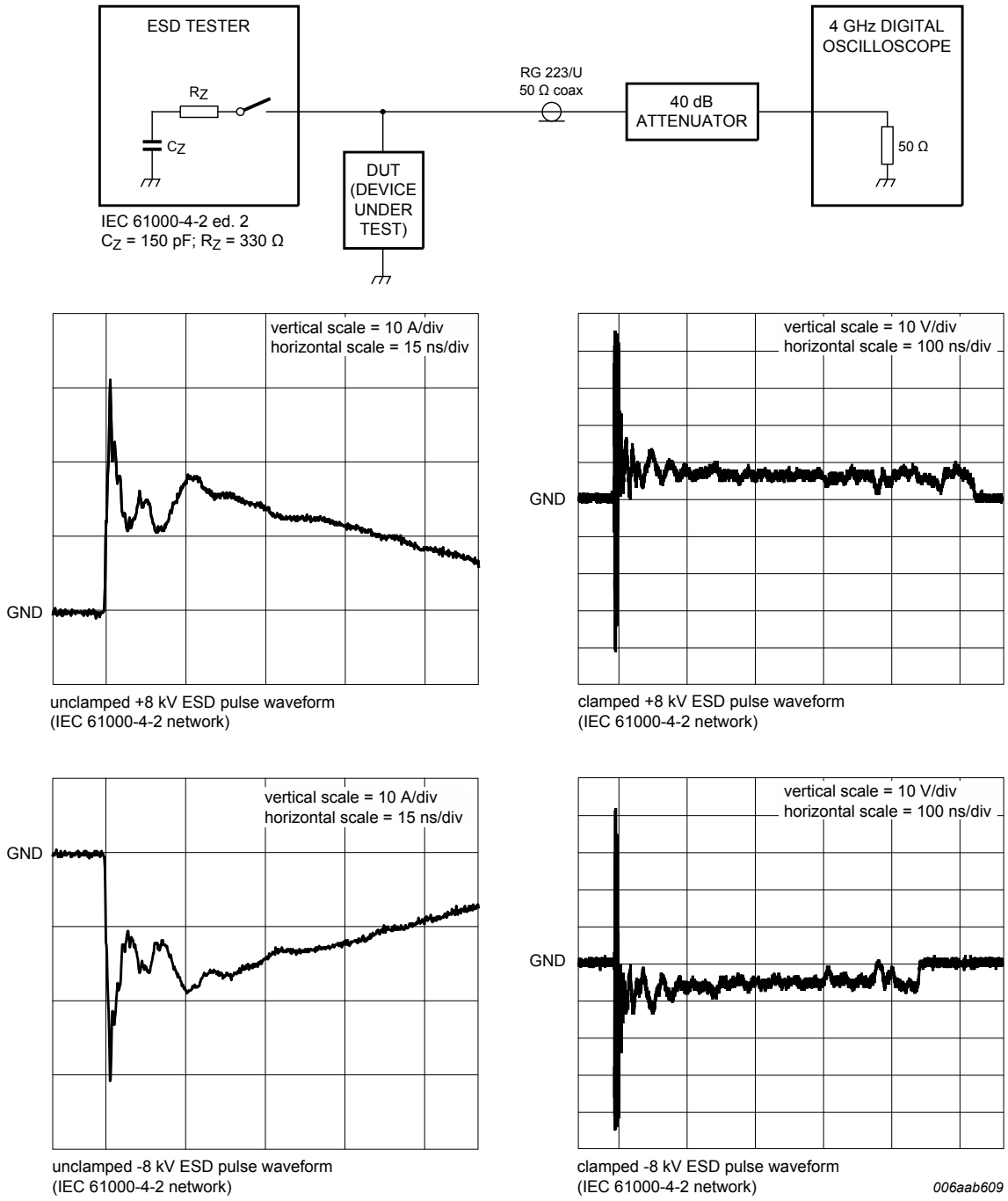


Fig. 9. ESD clamping test setup and waveforms

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

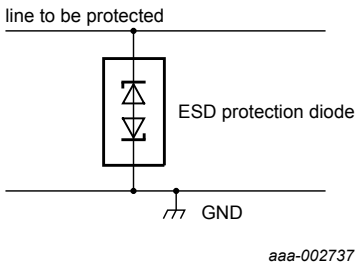


Fig. 10. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

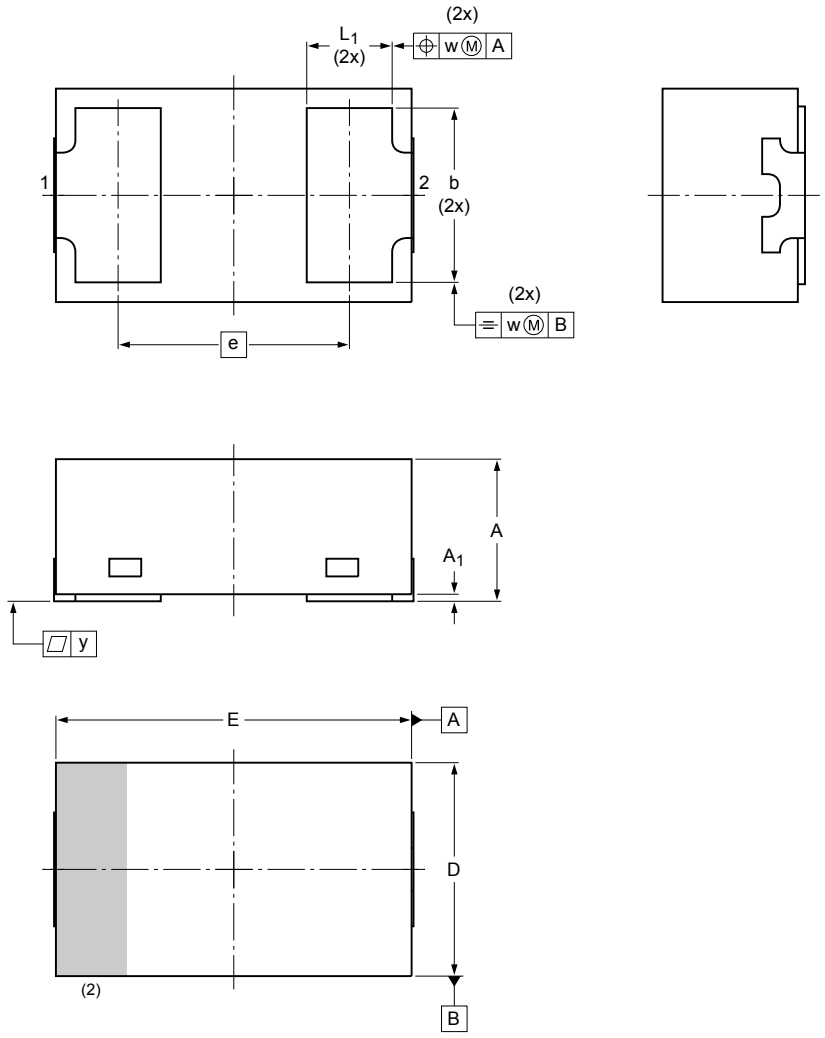
11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

DFN1006D-2: Leadless ultra small plastic package; 2 terminals; body 1 x 0.6 x 0.4 mm **SOD882D**



Dimensions

Unit		A(1)	A1	b	D	E	e	L1	w	y
mm	max	0.4	0.04	0.55	0.65	1.05		0.30	0.1	0.03
	nom			0.50	0.60	1.00	0.65	0.25		
	min			0.45	0.55	0.95		0.22		

0 0.5 1 mm
scale

Note
1. Dimension including plating thickness.
2. The marking bar indicates the cathode (if applicable).

sod882d_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD882D						~~10-09-27~~ 12-05-01

Fig. 11. Package outline DFN1006D-2 (SOD882D)

13. Soldering

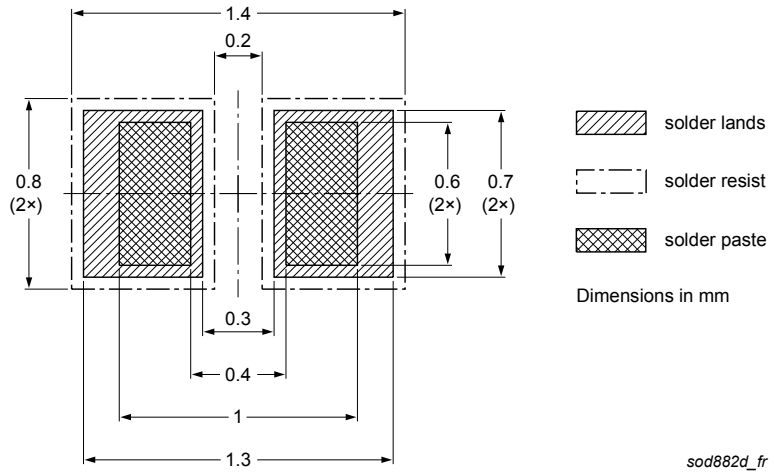


Fig. 12. Reflow soldering footprint for DFN1006D-2 (SOD882D)

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0S1ULD v.2	20170308	Product data sheet	-	PESD5V0S1ULD v.1
Modifications:	• Revise V_{RWM} to 5.5 V • Figure 9 updated			
PESD5V0S1ULD v.1	20101019	Product data sheet	-	

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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16. Contents

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Date of release: 8 March 2017