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# FDMC7200

## Dual N-Channel PowerTrench® MOSFET 30 V, 12 mΩ and 23.5 mΩ

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 23.5 mΩ at  $V_{GS} = 10$  V,  $I_D = 6$  A
- Max  $r_{DS(on)}$  = 38 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 5$  A

Q2: N-Channel

- Max  $r_{DS(on)}$  = 12 mΩ at  $V_{GS} = 10$  V,  $I_D = 8$  A
- Max  $r_{DS(on)}$  = 18 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 7$  A
- RoHS Compliant

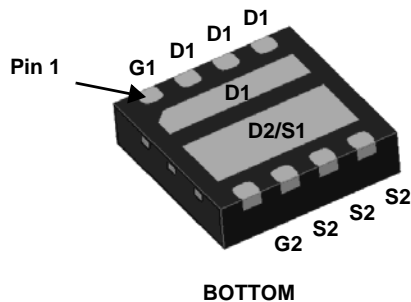


### General Description

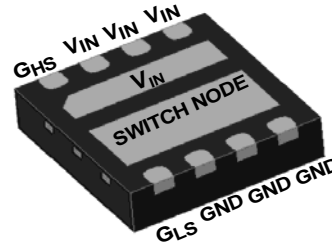
This device includes two specialized N-Channel MOSFETs in a dual Power33 (3mm x 3mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

### Applications

- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load

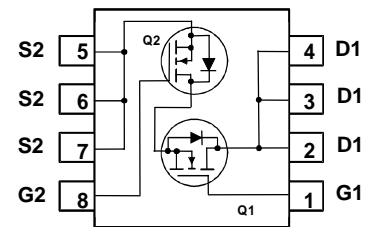


BOTTOM



BOTTOM

Power 33



### MOSFET Maximum Ratings $T_C = 25$ °C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	30	30	V
$V_{GS}$	Gate to Source Voltage (Note 3)	±20	±20	V
$I_D$	Drain Current - Continuous (Package limited) $T_C = 25$ °C	8	8	A
	- Continuous (Silicon limited) $T_C = 25$ °C	20	40	
	- Continuous $T_A = 25$ °C	6 <sup>1a</sup>	8 <sup>1b</sup>	
	- Pulsed	40	40	
$P_D$	Power Dissipation $T_A = 25$ °C	1.9 <sup>1a</sup>	2.2 <sup>1b</sup>	W
	Power Dissipation $T_A = 25$ °C	0.7 <sup>1c</sup>	0.9 <sup>1d</sup>	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	65 <sup>1a</sup>	55 <sup>1b</sup>	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	180 <sup>1c</sup>	145 <sup>1d</sup>	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	7.5	4	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7200	FDMC7200	Power 33	13"	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$ $I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		14 14		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2			1 1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2			100 100	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	Q1 Q2	1.0 1.0	2.3 2.3	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-5 -6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 6\text{ A}, T_J = 125\text{ }^\circ\text{C}$	Q1		19 28 29	23.5 38 35.5	m $\Omega$
		$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 8\text{ A}, T_J = 125\text{ }^\circ\text{C}$	Q2		10 13 15	12 18 18	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{ V}, I_D = 6\text{ A}$ $V_{DD} = 5\text{ V}, I_D = 8\text{ A}$	Q1 Q2		29 56		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance		Q1 Q2		495 1180	660 1570	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1 Q2		145 330	195 440	pF
$C_{riss}$	Reverse Transfer Capacitance		Q1 Q2		20 30	30 45	pF
$R_g$	Gate Resistance		Q1 Q2		1.4 1.4		$\Omega$

**Switching Characteristics**

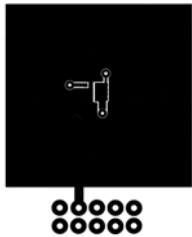
$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1 Q2		11 13	20 23	ns	
$t_r$	Rise Time		Q1 Q2		3.1 4	10 10	ns	
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1 Q2		35 38	56 60	ns	
$t_f$	Fall Time		Q1 Q2		1.3 6	10 12	ns	
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	Q1: $V_{DD} = 15\text{ V},$ $I_D = 6\text{ A},$	Q1 Q2		7.3 16	10 22	nC
$Q_{g(TOT)}$	Total Gate Charge			$V_{GS} = 0\text{ V to }4.5\text{ V}$	Q1 Q2		3.1 7	4.3 10
$Q_{gs}$	Gate to Source Charge		Q2: $V_{DD} = 15\text{ V},$ $I_D = 8\text{ A},$	Q1 Q2		1.8 4.1		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			Q1 Q2		1 1.5		nC

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Drain-Source Diode Characteristics</b>							
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 6\text{ A}$ (Note 2)	Q1		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 8\text{ A}$ (Note 2)	Q2		0.8	1.2	
$t_{rr}$	Reverse Recovery Time	Q1 $I_F = 6\text{ A}, di/dt = 100\text{ A/s}$	Q1		13	24	ns
			Q2		21	34	
$Q_{rr}$	Reverse Recovery Charge	Q2 $I_F = 8\text{ A}, di/dt = 100\text{ A/s}$	Q1		2.3	10	nC
			Q2		5.6	12	

Notes:

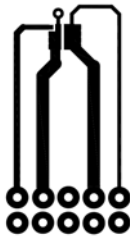
1.  $R_{\theta JA}$  is determined with the device mounted on a 1in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



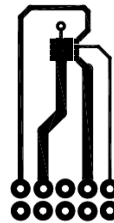
a. 65 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 55 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



c. 180 °C/W when mounted on a minimum pad of 2 oz copper



d. 145 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

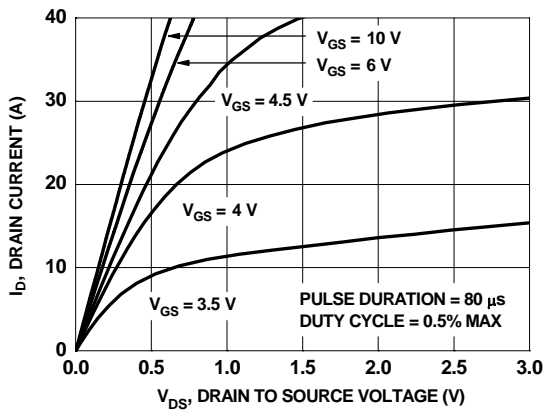


Figure 1. On Region Characteristics

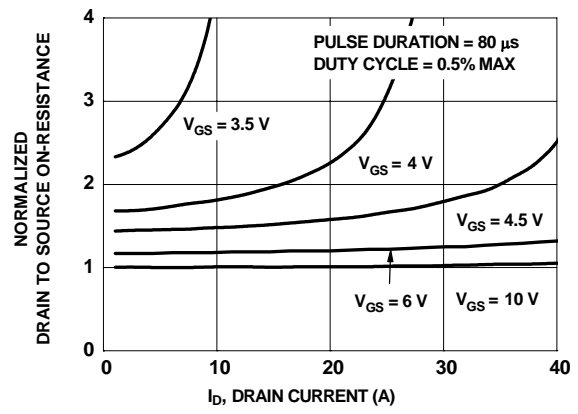


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

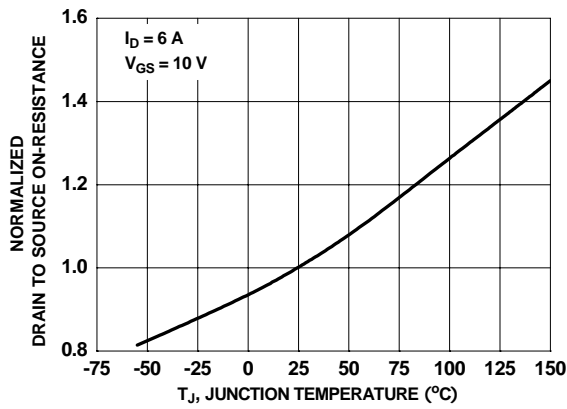


Figure 3. Normalized On Resistance vs Junction Temperature

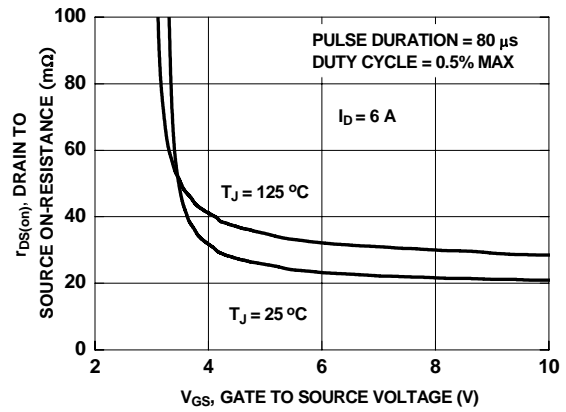


Figure 4. On-Resistance vs Gate to Source Voltage

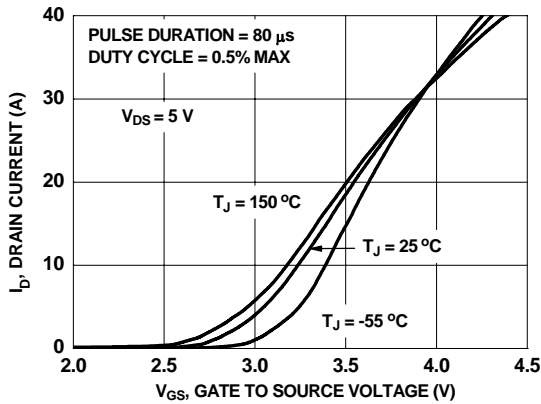


Figure 5. Transfer Characteristics

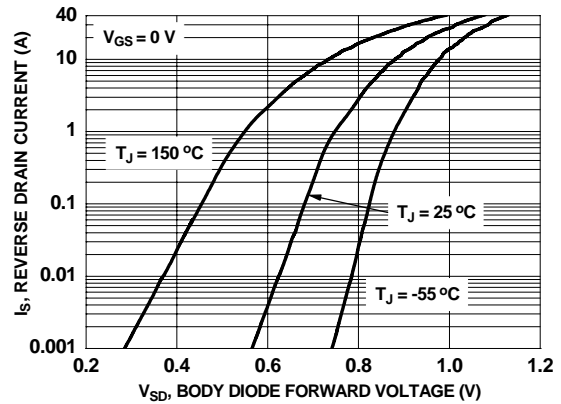
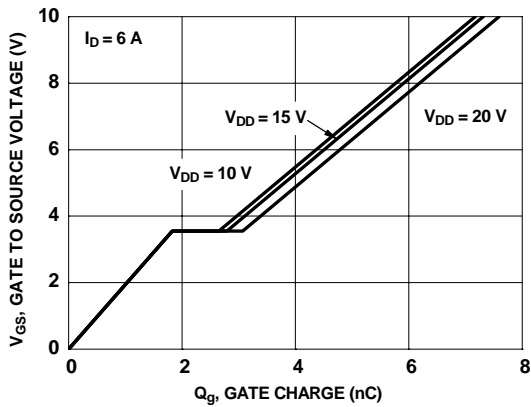
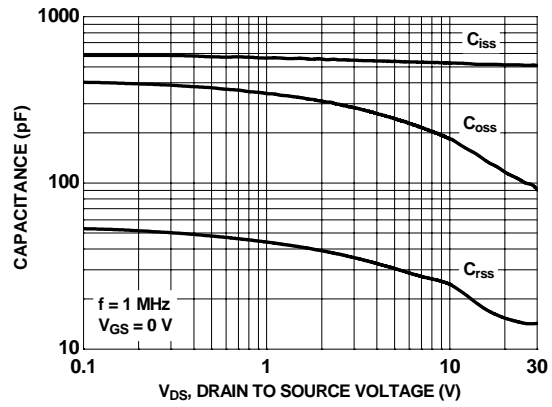


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

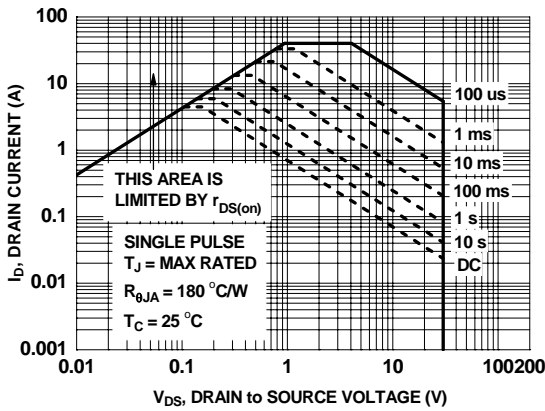
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



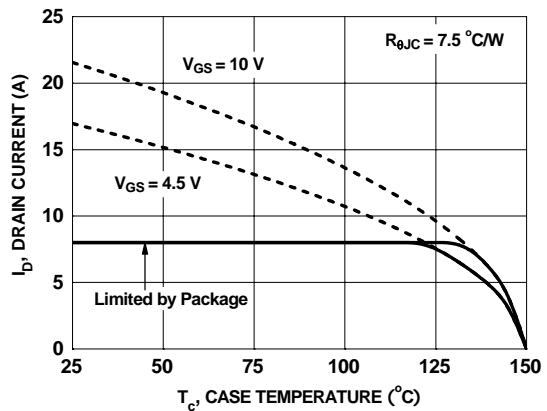
**Figure 7. Gate Charge Characteristics**



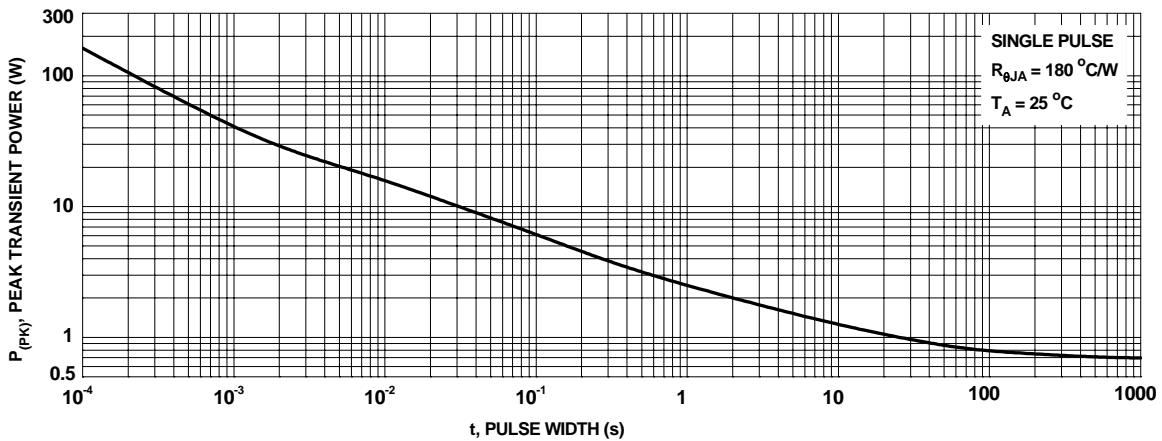
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Forward Bias Safe Operating Area**

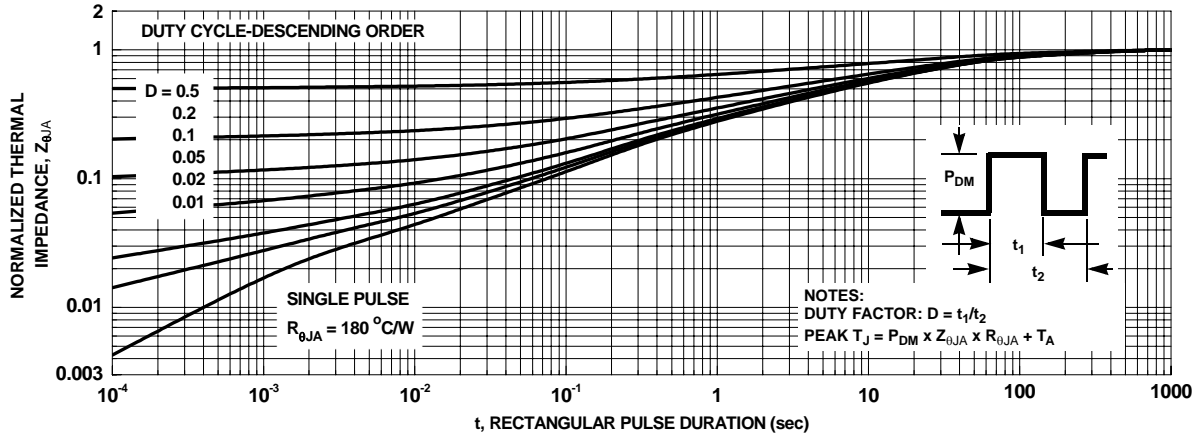


**Figure 10. Maximum Continuous Drain Current vs Case Temperature**



**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**

**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

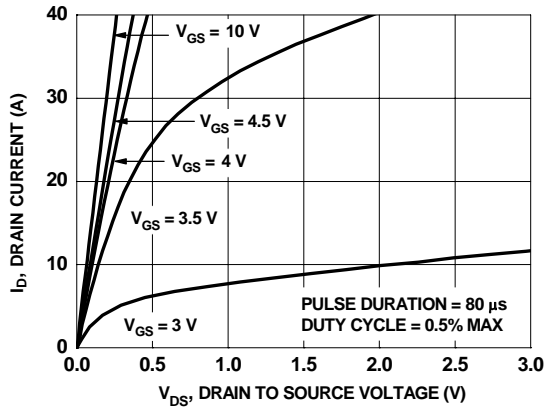


Figure 13. On-Region Characteristics

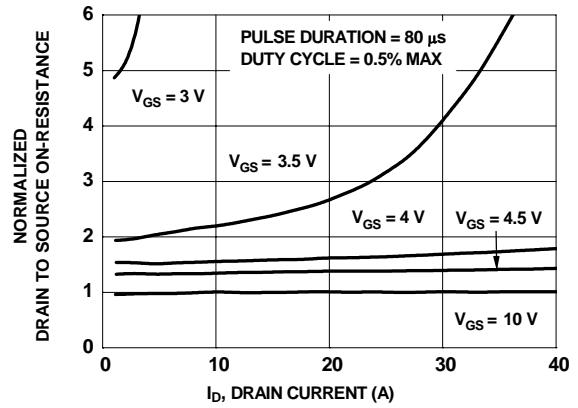


Figure 14. Normalized on-Resistance vs Drain Current and Gate Voltage

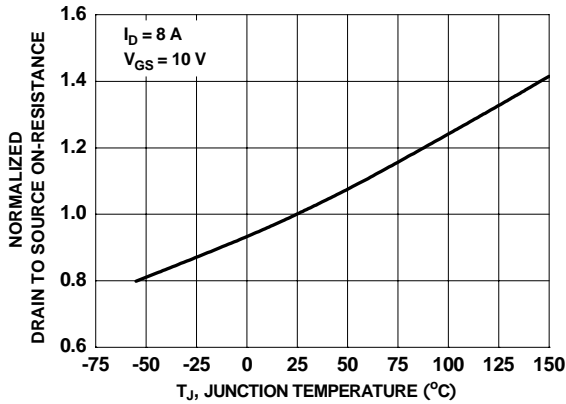


Figure 15. Normalized On-Resistance vs Junction Temperature

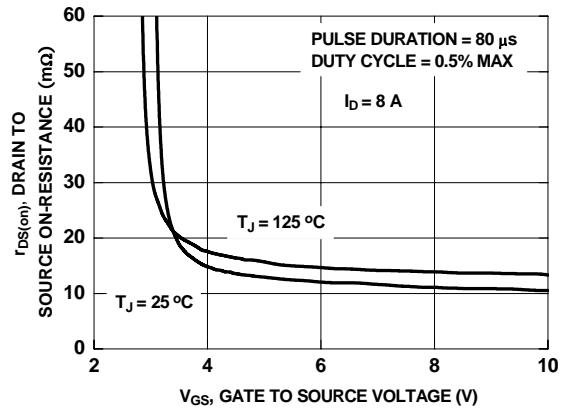


Figure 16. On-Resistance vs Gate to Source Voltage

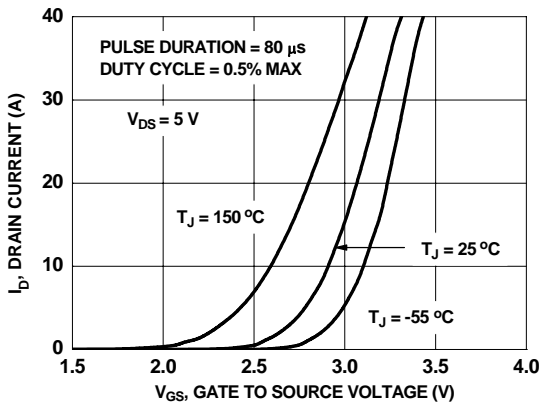


Figure 17. Transfer Characteristics

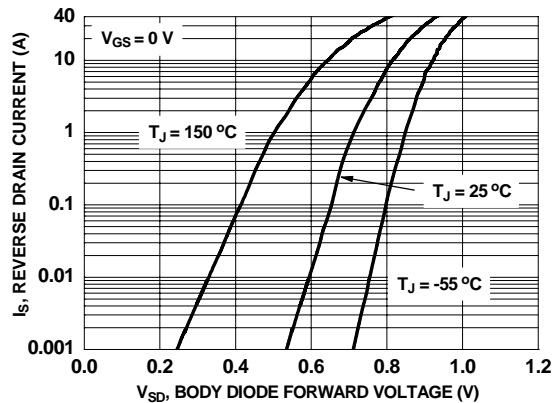
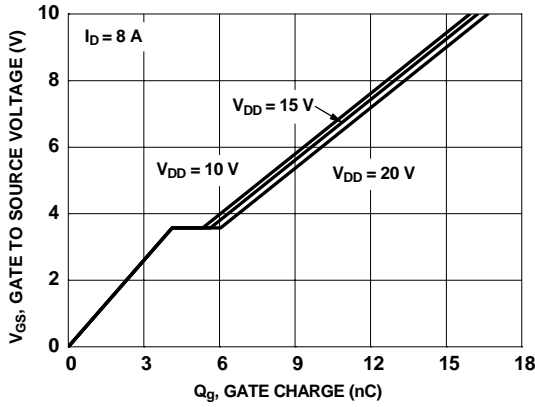


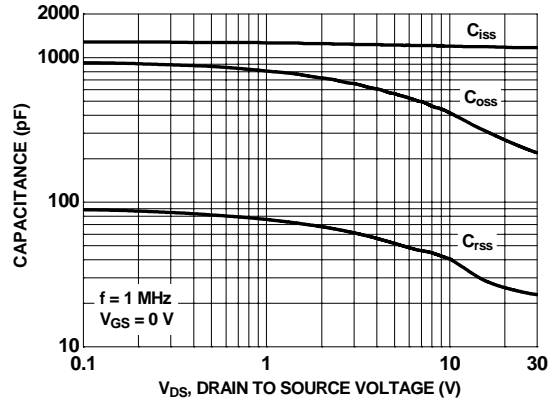
Figure 18. Source to Drain Diode Forward Voltage vs Source Current



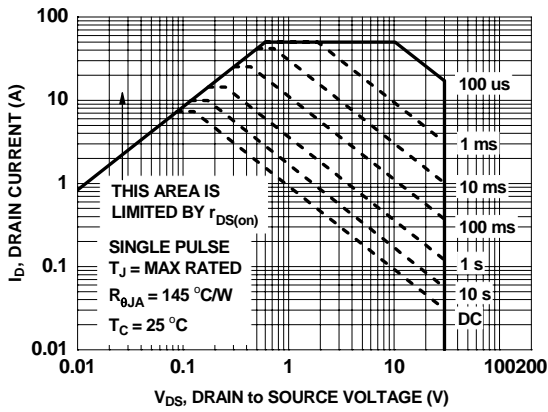
**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



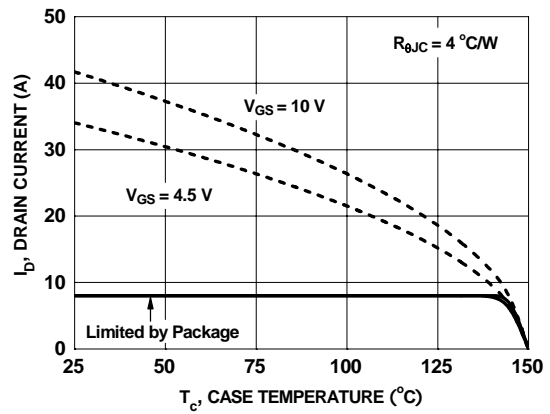
**Figure 19. Gate Charge Characteristics**



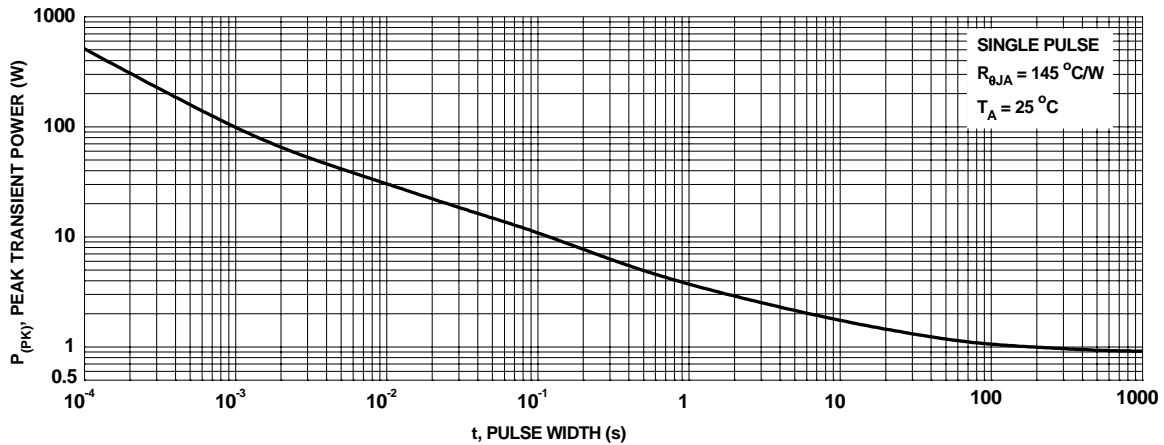
**Figure 20. Capacitance vs Drain to Source Voltage**



**Figure 21. Forward Bias Safe Operating Area**

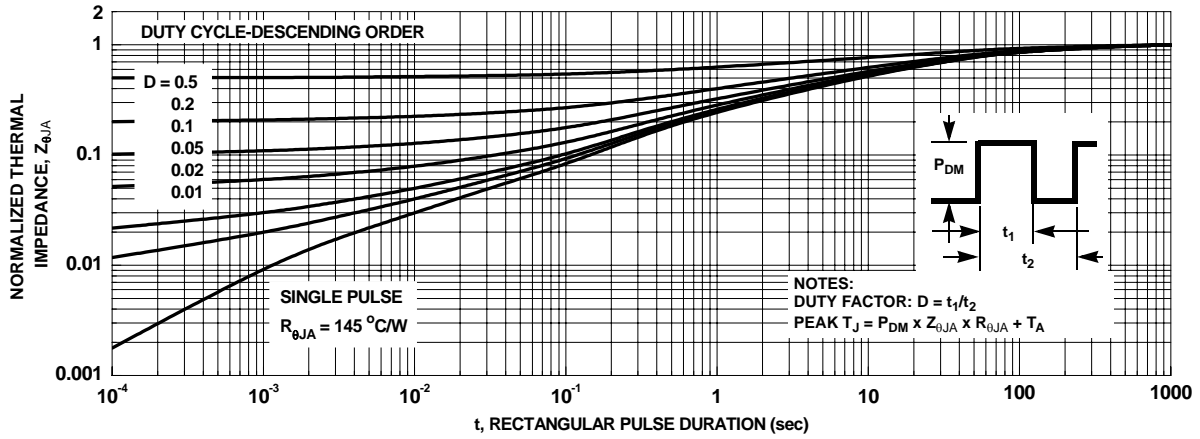


**Figure 22. Maximum Continuous Drain Current vs Case Temperature**



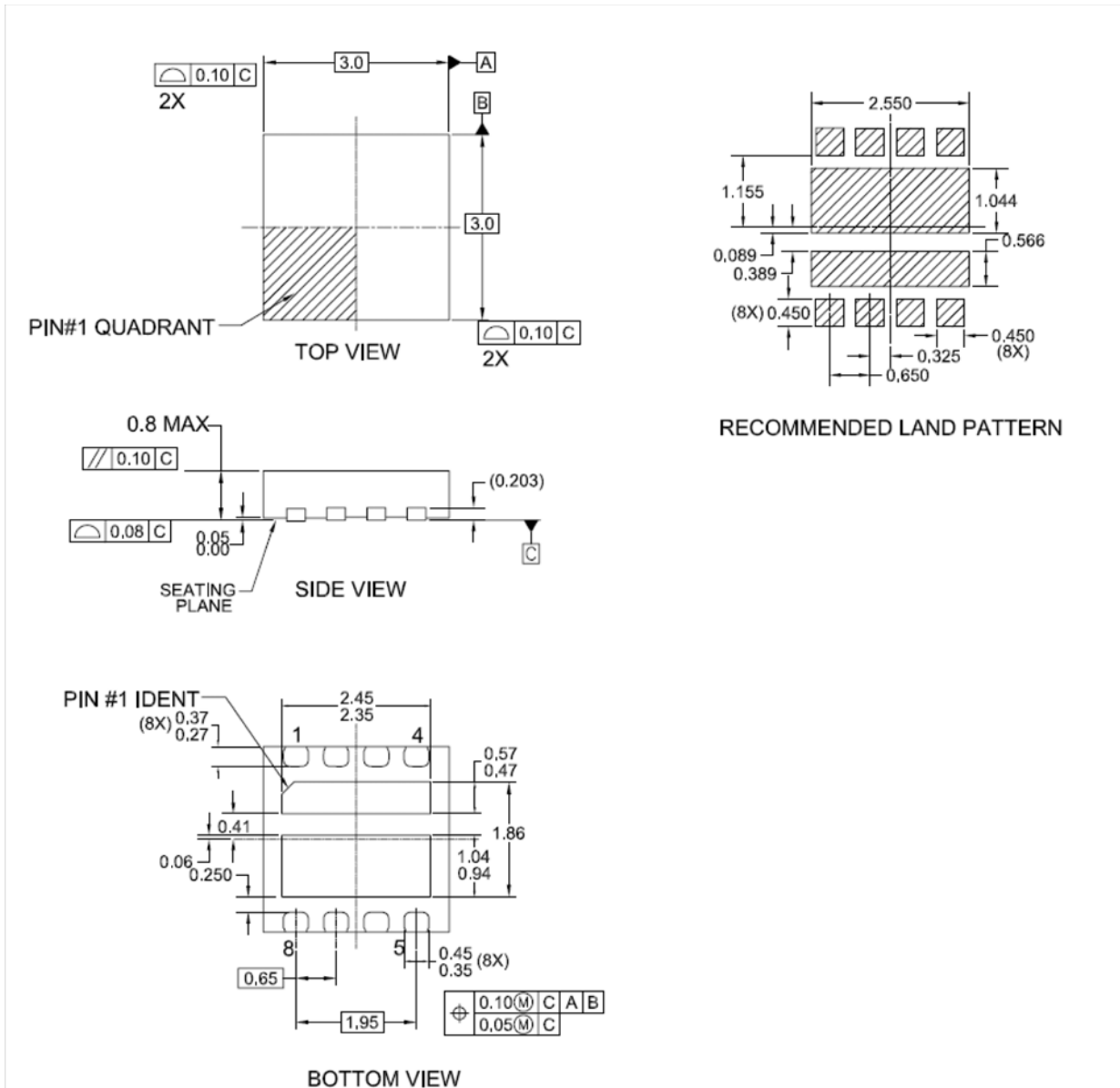
**Figure 22. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 23. Junction-to-Ambient Transient Thermal Response Curve**







## Dimensional Outline and Pad Layout





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**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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